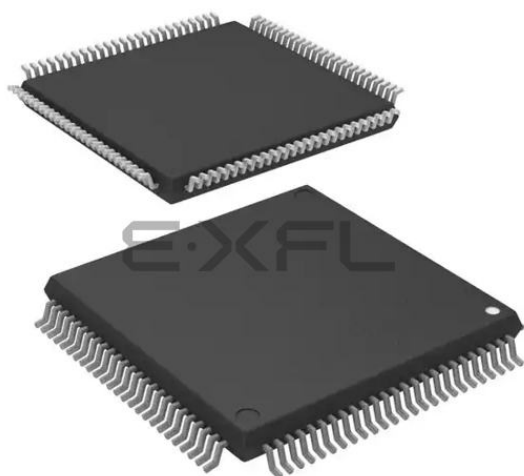




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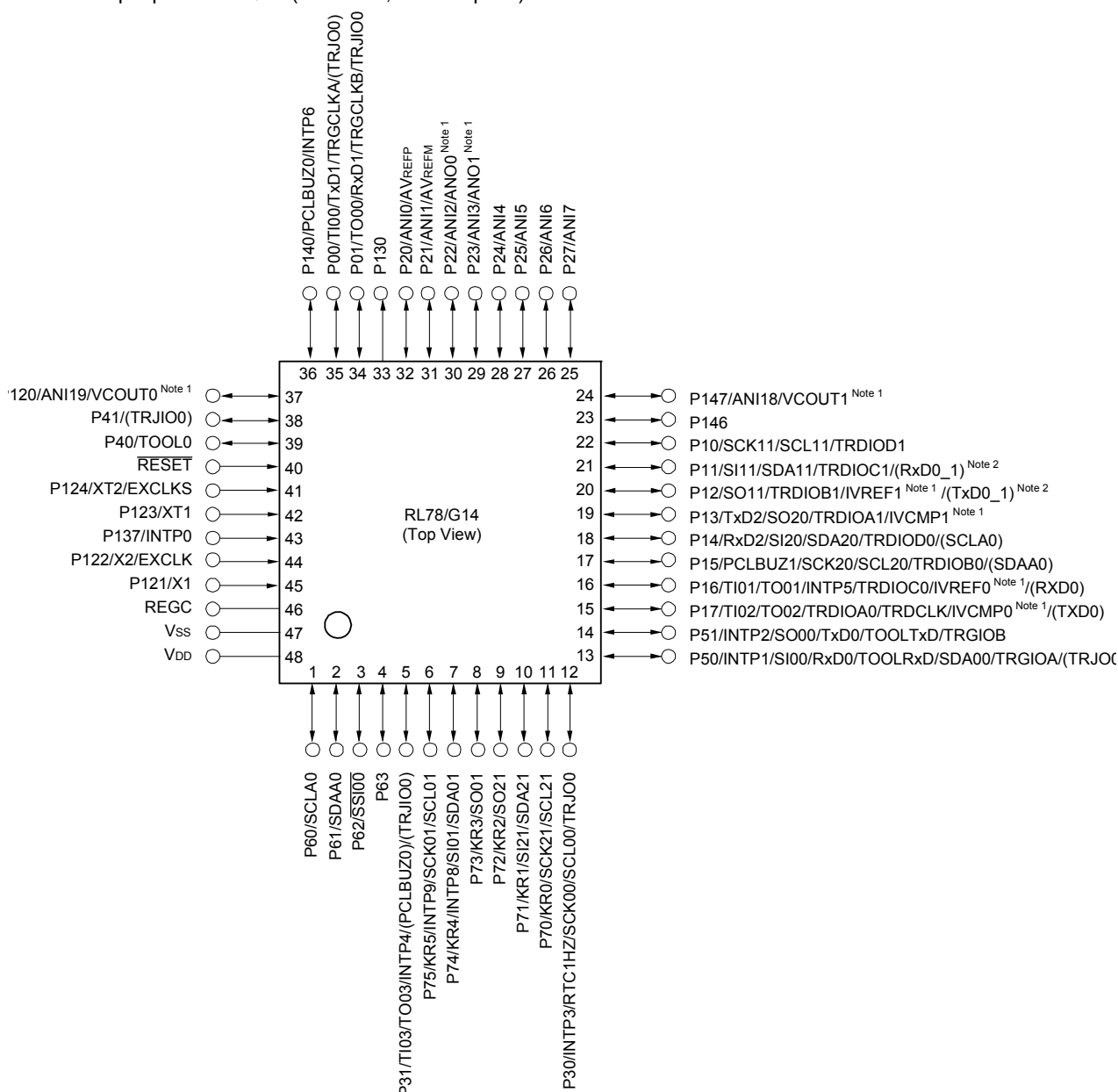
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104pjafb-30

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

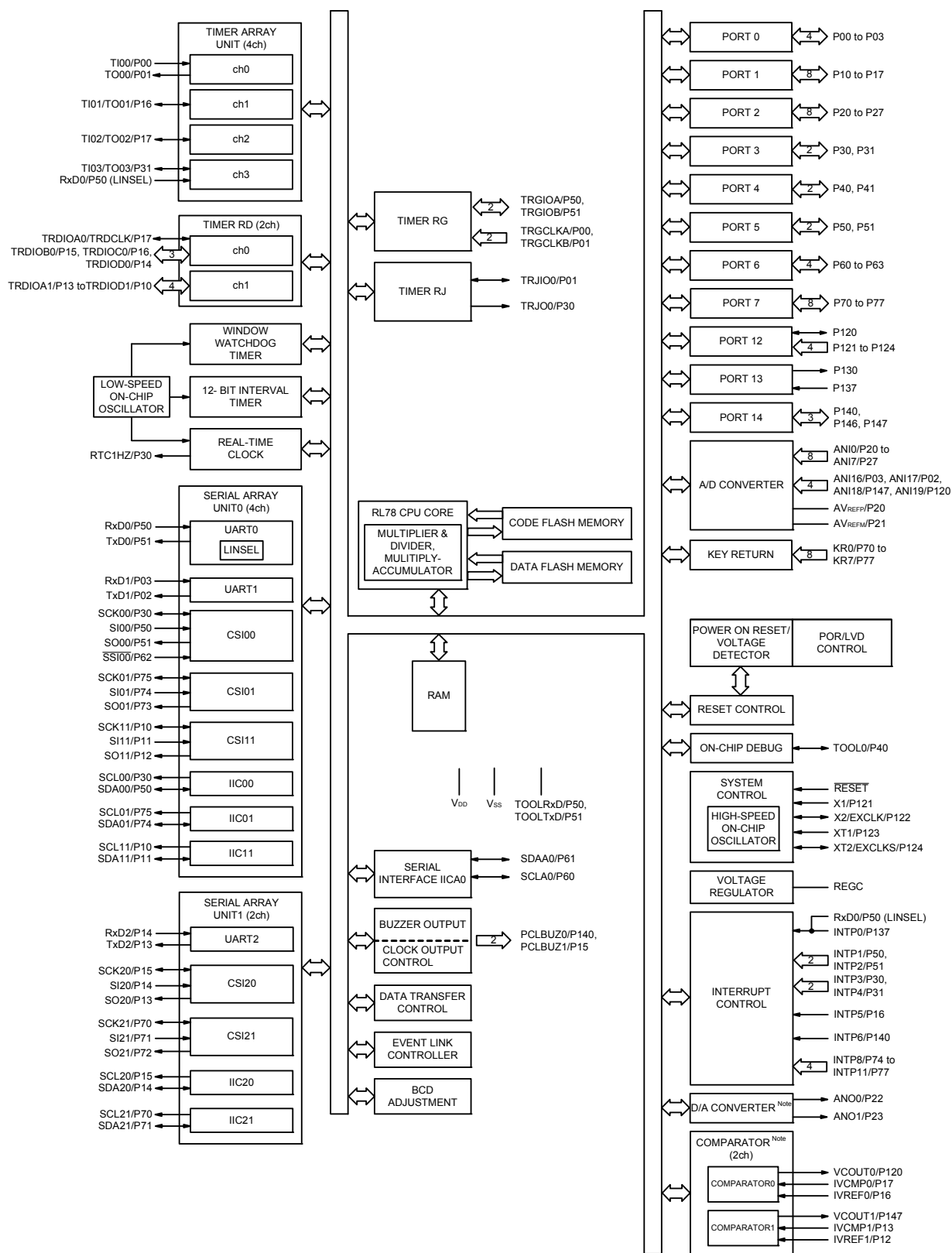
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

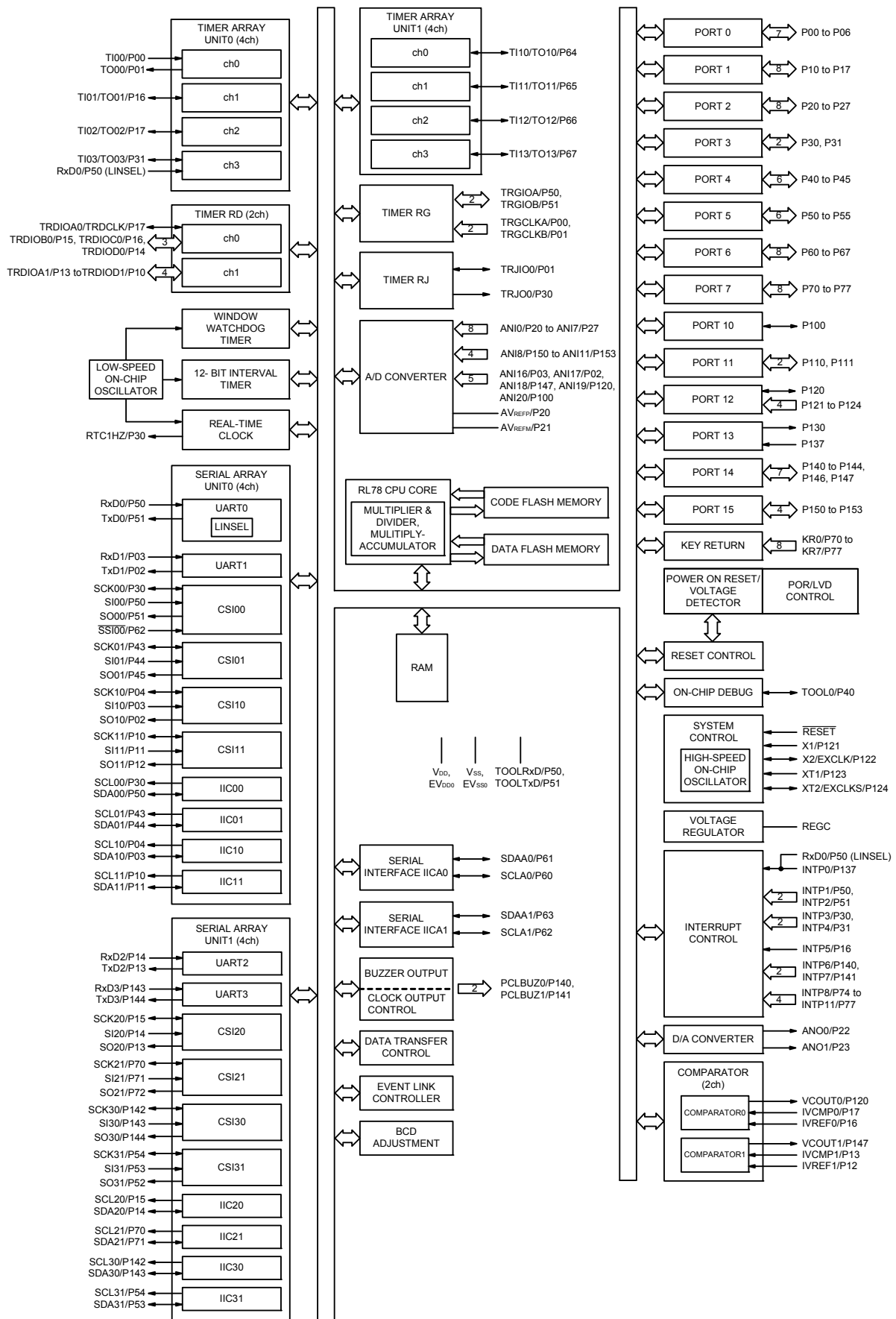
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.5.7 52-pin products



Note Mounted on the 96 KB or more code flash memory products.

1.5.9 80-pin products



Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

[48-pin, 64-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		48-pin	64-pin
		R5F104Gx (x = K, L)	R5F104Lx (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	44	58
	CMOS I/O	34	48
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels	
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

(Note is listed on the next page.)

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

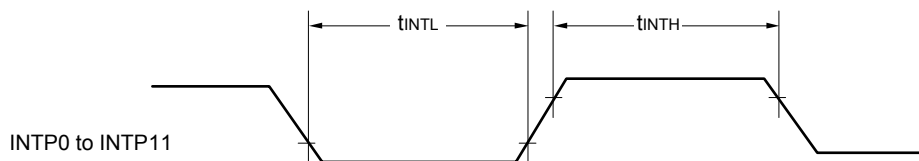
(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

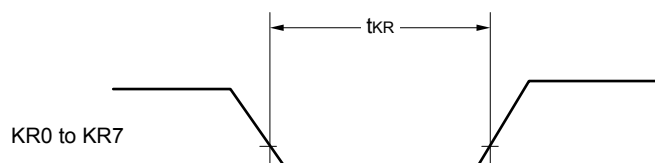
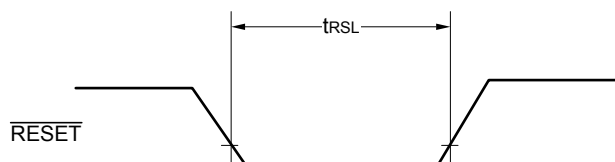
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	3.32	mA			
					VDD = 3.0 V		0.93	3.32				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	2.63				
					VDD = 3.0 V		0.5	2.63				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	2.60				
					VDD = 3.0 V		0.72	2.60				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	2.03				
					VDD = 3.0 V		0.42	2.03				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	1.50				
					VDD = 3.0 V		0.39	1.50				
			LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		270	800	μA			
					VDD = 2.0 V		270	800				
			LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		450	755	μA			
					VDD = 2.0 V		450	755				
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	1.69	mA			
					Resonator connection		0.41	1.91				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31		1.69		
						Resonator connection		0.41		1.91		
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21		0.94		
						Resonator connection		0.26		1.02		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	0.94				
					Resonator connection		0.26	1.02				
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA		
						Resonator connection		150	660			
			fMX = 8 MHz Note 3, VDD = 2.0 V		Square wave input		110	610				
					Resonator connection		150	660				
			Subsystem clock oper- ation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31		μA			
					Resonator connection		0.50					
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.38	0.76				
					Resonator connection		0.57	0.95				
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47	3.59				
					Resonator connection		0.70	3.78				
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80	6.20				
					Resonator connection		1.00	6.39				
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65	10.56				
					Resonator connection		1.84	10.75				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19		μA
					TA = +25°C					0.30	0.59	
					TA = +50°C					0.41	3.42	
					TA = +70°C					0.80	6.03	
					TA = +85°C					1.53	10.39	

(Notes and Remarks are listed on the next page.)

Interrupt Request Input Timing



Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

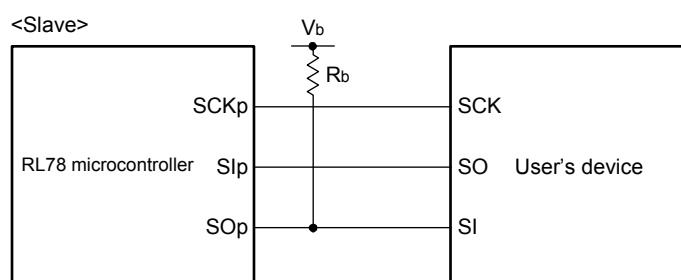
Note 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 2.** Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD0} \geq V_b$.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remark 1.** R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fSCL	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	tLOW	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	tHIGH	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	610		610		610		ns

2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		VLVD1	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		VLVD2	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		VLVD3	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		VLVD4	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		VLVD5	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		VLVD6	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		VLVD7	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		VLVD8	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		VLVD9	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		VLVD10	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		VLVD11	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		VLVD12	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		VLVD13	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ EVDD0 ≤ 5.5 V		-60.0	mA
	IOH2	Per pin for P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ VDD ≤ 5.5 V		-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
 <Example> Where n = 80% and IOH = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	4.86	mA
					VDD = 3.0 V		0.79	4.86	
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	4.17	
					VDD = 3.0 V		0.49	4.17	
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.82	
					VDD = 3.0 V		0.62	3.82	
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	3.25	
					VDD = 3.0 V		0.4	3.25	
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	2.28	
					VDD = 3.0 V		0.38	2.28	
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	2.65	mA
					Resonator connection		0.40	2.77	
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30	2.65	
					Resonator connection		0.40	2.77	
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	1.36	
					Resonator connection		0.25	1.46	
	IDD3 Note 6	STOP mode Note 8	Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA
					Resonator connection		0.47	0.85	
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66	
					Resonator connection		0.53	0.85	
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35	
					Resonator connection		0.56	2.54	
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08	
					Resonator connection		0.80	4.27	
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09	
					Resonator connection		1.74	8.28	
				fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		6.00	51.00	
					Resonator connection		6.00	51.00	
				TA = -40°C			0.19	0.57	μA
				TA = +25°C			0.25	0.57	
				TA = +50°C			0.33	2.26	
				TA = +70°C			0.52	3.99	
				TA = +85°C			1.46	8.00	
				TA = +105°C			5.50	50.00	

(Notes and Remarks are listed on the next page.)

3.4 AC Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
		Subsystem clock (fSUB) operation		2.4 V ≤ VDD ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
External system clock frequency	fEX	2.7 V ≤ VDD ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ VDD ≤ 2.7 V			1.0		16.0	MHz
	fEXS				32		35	kHz
External system clock input high-level width, low-level width	tEXH,	2.7 V ≤ VDD ≤ 5.5 V			24			ns
	tEXL	2.4 V ≤ VDD ≤ 2.7 V			30			ns
	tEXHS, tEXLS				13.7			μs
Ti00 to Ti03, Ti10 to Ti13 input high-level width, low-level width	tTIH, tTIL				1/fMCK + 10 Note			ns
Timer RJ input cycle	fc	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	100			ns
				2.4 V ≤ EVDD0 < 2.7 V	300			ns
Timer RJ input high-level width, low-level width	tTJIH, tTJIL	TRJIO		2.7 V ≤ EVDD0 ≤ 5.5 V	40			ns
				2.4 V ≤ EVDD0 < 2.7 V	120			ns

Note The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$
 $2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

Note 5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq E_{VDD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ E_{VDD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		400 Note 1	kHz
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		400 Note 1	kHz
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$		100 Note 1	kHz
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		100 Note 1	kHz
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	1200		ns
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$	4600		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	4650		ns
Hold time when SCLr = "H"	t _{HIGH}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	620		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 50\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	500		ns
		$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.8\text{ k}\Omega$	2700		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$, $\text{Cb} = 100\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	1830		ns

3.6.6 LVD circuit characteristics

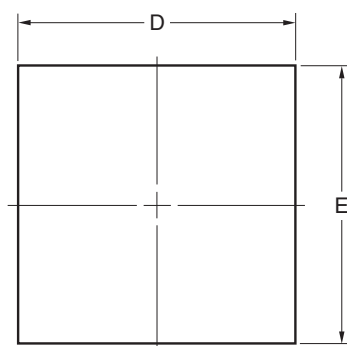
(1) Reset Mode and Interrupt Mode

($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

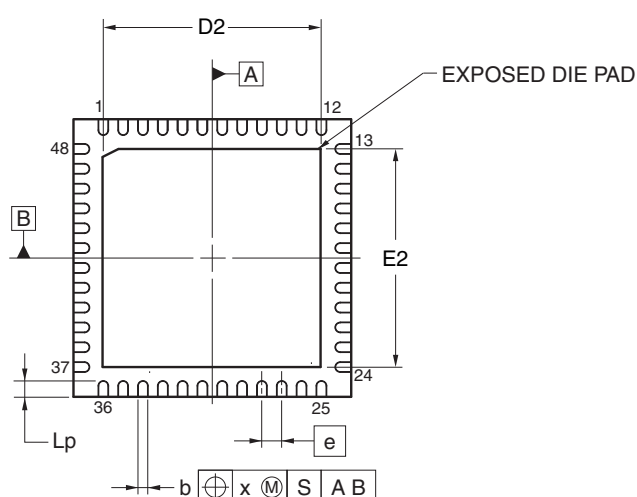
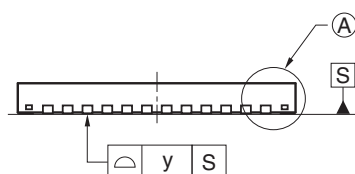
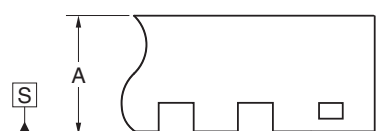
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.90	4.06	4.22	V
			Falling edge	3.83	3.98	4.13	V
		VLVD1	Rising edge	3.60	3.75	3.90	V
			Falling edge	3.53	3.67	3.81	V
		VLVD2	Rising edge	3.01	3.13	3.25	V
			Falling edge	2.94	3.06	3.18	V
		VLVD3	Rising edge	2.90	3.02	3.14	V
			Falling edge	2.85	2.96	3.07	V
		VLVD4	Rising edge	2.81	2.92	3.03	V
			Falling edge	2.75	2.86	2.97	V
		VLVD5	Rising edge	2.70	2.81	2.92	V
			Falling edge	2.64	2.75	2.86	V
		VLVD6	Rising edge	2.61	2.71	2.81	V
			Falling edge	2.55	2.65	2.75	V
		VLVD7	Rising edge	2.51	2.61	2.71	V
			Falling edge	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA,
 R5F104GHANA, R5F104GJANA
 R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA,
 R5F104GHDNA, R5F104GJDNA
 R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,
 R5F104GHGNA, R5F104GJGNA
 R5F104GKANA, R5F104GLANA
 R5F104GKGNA, R5F104GLGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

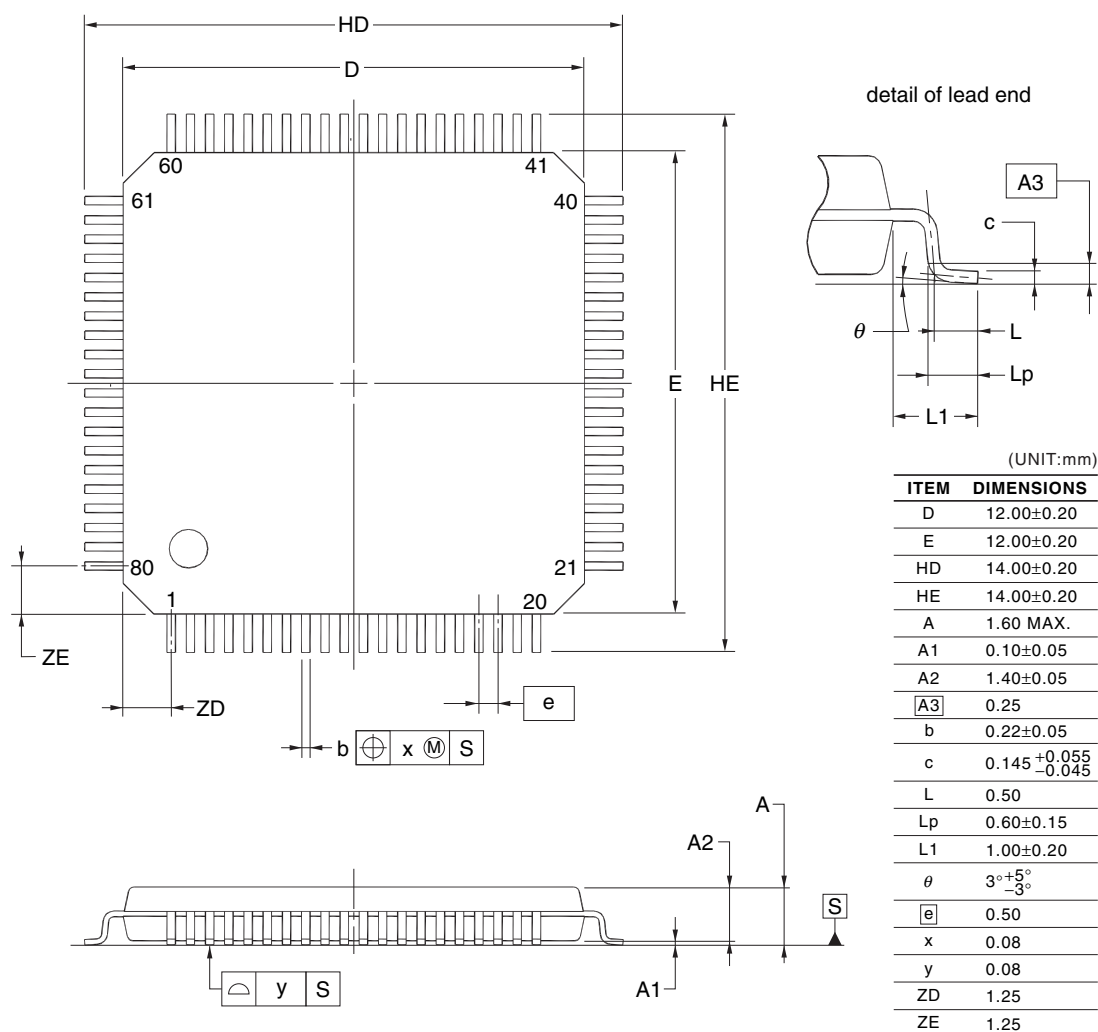
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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4.9 80-pin products

R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
 R5F104MDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
 R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.