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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f104pkafb-30

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Pin count	Package	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0 R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 R5F104GKAFB#30, R5F104GLAFB#30 R5F104GKAFB#50, R5F104GLAFB#50
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0 R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104CHGFB#V0, R5F104GJGFB#V0 R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104CHGFB#X0, R5F104GJGFB#X0 R5F104GKGB#30, R5F104GLGB#30 R5F104GKGB#50, R5F104GLGB#50
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0 R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0 R5F104GKANA#U0, R5F104GLANA#U0 R5F104GKANA#W0, R5F104GLANA#W0
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0 R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0 R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0 R5F104GKGNA#U0, R5F104GLGNA#U0 R5F104GKGNA#W0, R5F104GLGNA#W0
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHFAFA#V0, R5F104JJFAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHFAFA#X0, R5F104JJFAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

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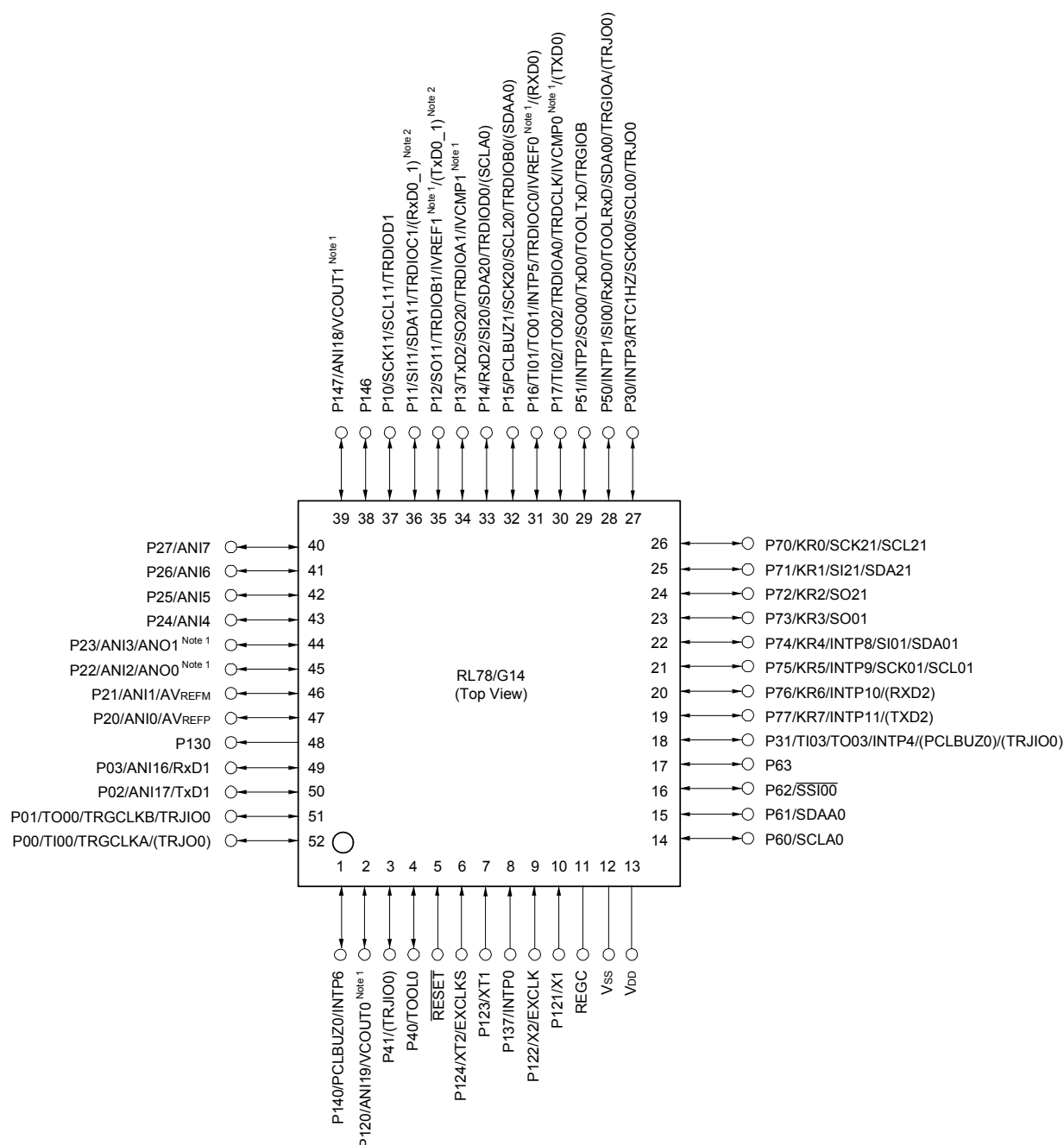
Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAF#V0, R5F104LHAF#V0, R5F104LJAF#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAF#X0, R5F104LHAF#X0, R5F104LJAF#X0 R5F104LKAF#30, R5F104LLAF#30 R5F104LKAF#50, R5F104LLAF#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDF#V0, R5F104LHDF#V0, R5F104LJDF#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDF#X0, R5F104LHDF#X0, R5F104LJDF#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCA#U0, R5F104LDA#U0, R5F104LEA#U0, R5F104LFA#U0, R5F104LGA#U0, R5F104LHA#U0, R5F104LJA#U0 R5F104LCA#W0, R5F104LDA#W0, R5F104LEA#W0, R5F104LFA#W0, R5F104LGA#W0, R5F104LHA#W0, R5F104LJA#W0 R5F104LKA#U0, R5F104LLA#U0 R5F104LKA#W0, R5F104LLA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFLGA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFLGA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
		D	R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0
		G	R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

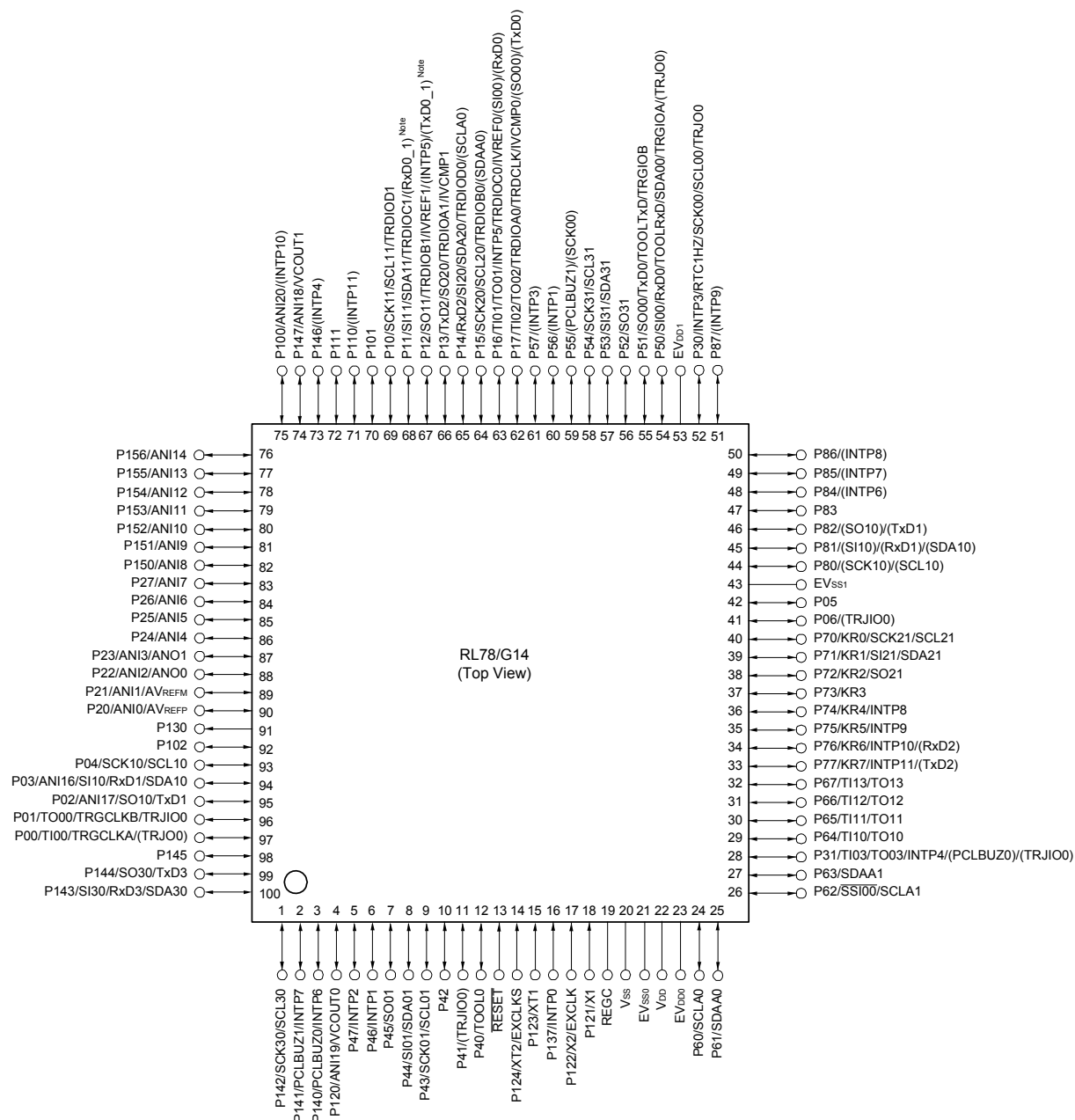
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

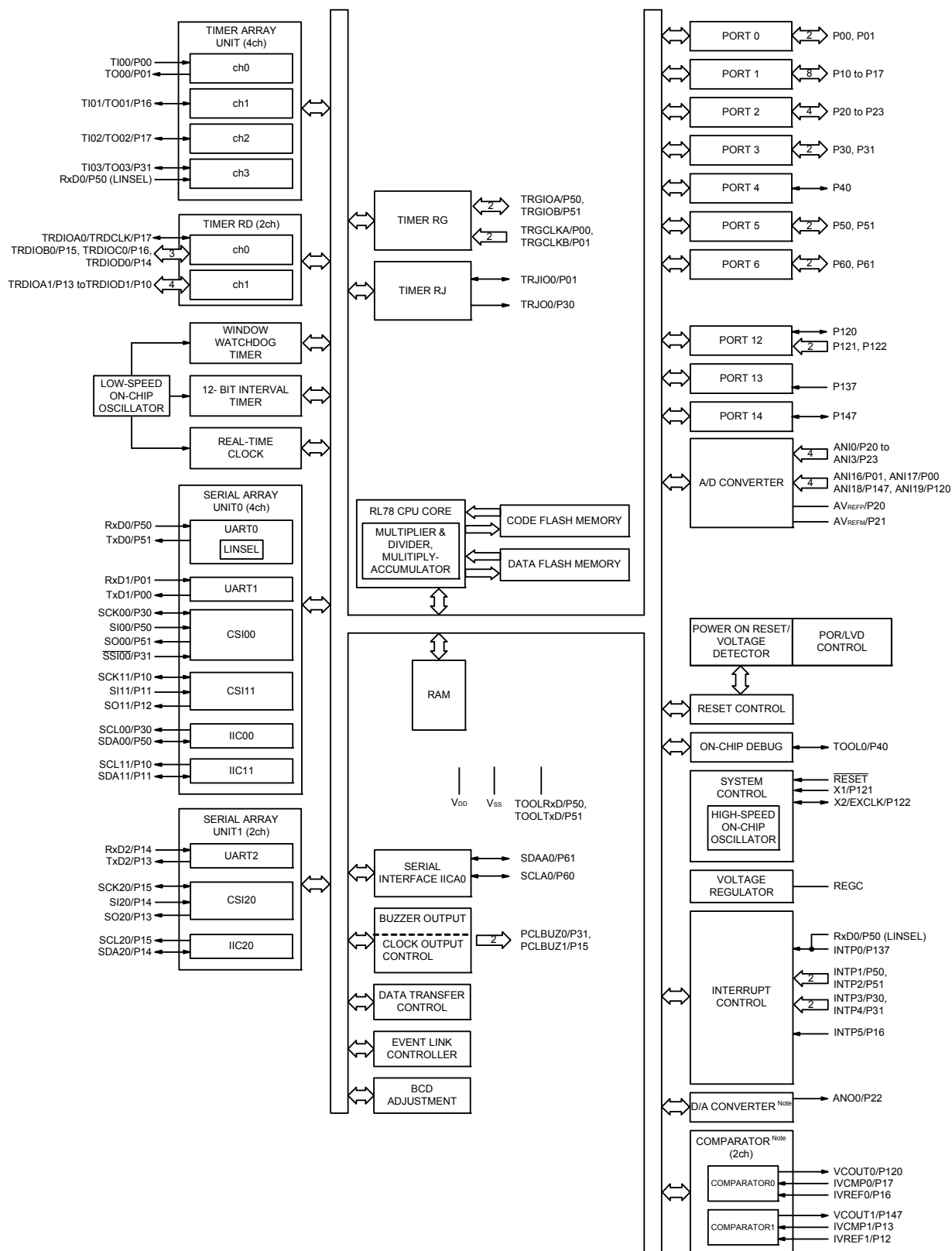
1.3.10 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)



1.5 Block Diagram

1.5.1 30-pin products



Note Mounted on the 96 KB or more code flash memory products.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _I REGC	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3 Note 2	V
Analog input voltage	V _{AI1}	ANI16 to ANI20	-0.3 to EV _{DD0} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5		V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7		V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
			1.6 V ≤ EVDD0 < 1.8 V, IOH1 = -1.0 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA	VDD - 0.5		V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 20.0 mA		1.3	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.3 mA		0.4	V
	VOL2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.93	3.32	mA			
					VDD = 3.0 V		0.93	3.32				
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.5	2.63				
					VDD = 3.0 V		0.5	2.63				
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.72	2.60				
					VDD = 3.0 V		0.72	2.60				
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.42	2.03				
					VDD = 3.0 V		0.42	2.03				
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.39	1.50				
					VDD = 3.0 V		0.39	1.50				
				LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		270		800	μA	
						VDD = 2.0 V		270		800		
				LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		450		755	μA	
						VDD = 2.0 V		450		755		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	1.69	mA			
					Resonator connection		0.41	1.91				
					fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31		1.69		
						Resonator connection		0.41		1.91		
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21		0.94		
						Resonator connection		0.26		1.02		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	0.94				
					Resonator connection		0.26	1.02				
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA		
						Resonator connection		150	660			
					fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input		110	610			
						Resonator connection		150	660			
				Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.31		μA		
						Resonator connection		0.50				
			fSUB = 32.768 kHz Note 5, TA = +25°C		Square wave input		0.38	0.76				
					Resonator connection		0.57	0.95				
			fSUB = 32.768 kHz Note 5, TA = +50°C		Square wave input		0.47	3.59				
					Resonator connection		0.70	3.78				
			fSUB = 32.768 kHz Note 5, TA = +70°C		Square wave input		0.80	6.20				
					Resonator connection		1.00	6.39				
			fSUB = 32.768 kHz Note 5, TA = +85°C		Square wave input		1.65	10.56				
					Resonator connection		1.84	10.75				
			IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19		μA
					TA = +25°C					0.30	0.59	
					TA = +50°C					0.41	3.42	
					TA = +70°C					0.80	6.03	
					TA = +85°C					1.53	10.39	

(Notes and Remarks are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	Note 1		Note 1		Note 1	bps
									Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	Note 2		Note 2		Note 2	Mbps
									bps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	Note 3		Note 3		Note 3	Mbps
									bps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

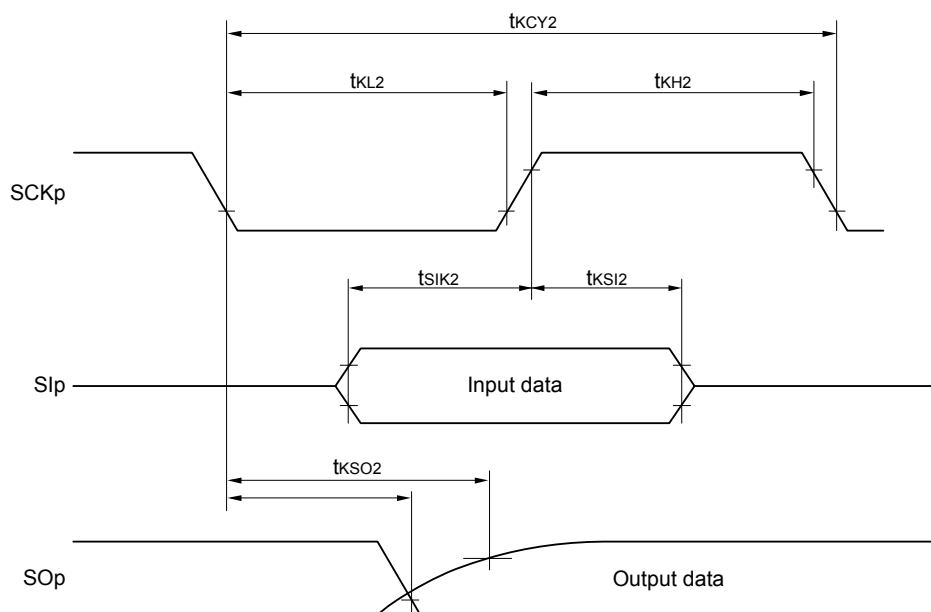
Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

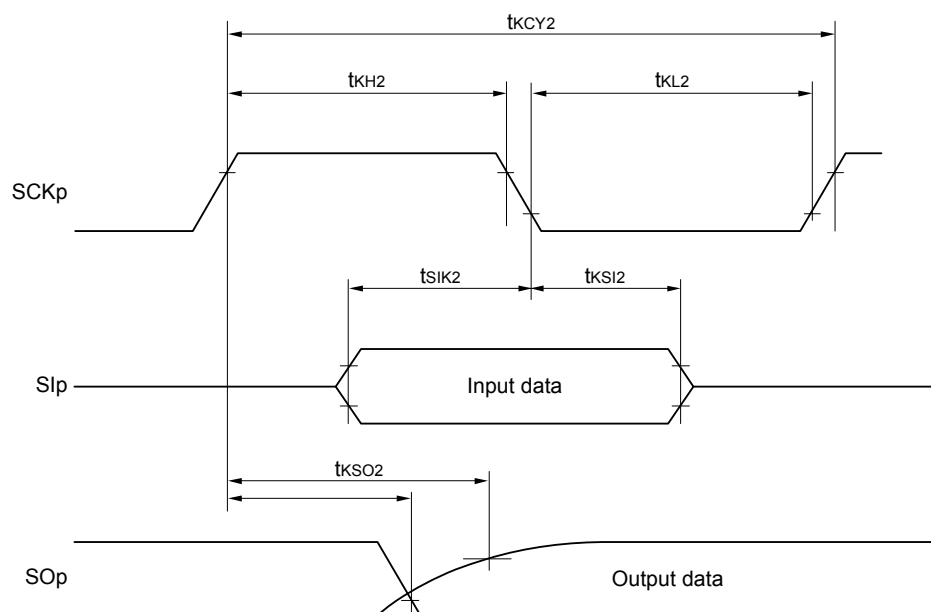
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI14		Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI20		Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage		Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4		1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E _{zs}	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Full-scale error Notes 1, 2	E _{fs}	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4			±2.0	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI14		0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} Note 5			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TPMS25} Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 5. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) Interrupt & Reset Mode**(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVDA0	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	VLVDA1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	VLVDB1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	VLVDC1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDC3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.7 Power supply voltage rising slope characteristics**(TA = -40 to +85°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	4.86	mA	
					VDD = 3.0 V		0.79	4.86		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	4.17		
					VDD = 3.0 V		0.49	4.17		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	3.82		
					VDD = 3.0 V		0.62	3.82		
				fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	3.25		
					VDD = 3.0 V		0.4	3.25		
				fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	2.28		
					VDD = 3.0 V		0.38	2.28		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	2.65	mA	
					Resonator connection		0.40	2.77		
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30	2.65		
					Resonator connection		0.40	2.77		
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	1.36		
					Resonator connection		0.25	1.46		
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	1.36		
					Resonator connection		0.25	1.46		
		Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA		
				Resonator connection		0.47	0.85			
			fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.66			
				Resonator connection		0.53	0.85			
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.37	2.35			
				Resonator connection		0.56	2.54			
			fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.61	4.08			
				Resonator connection		0.80	4.27			
			fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09			
				Resonator connection		1.74	8.28			
			fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		6.00	51.00			
				Resonator connection		6.00	51.00			
	IDD3 Note 6	STOP mode Note 8	TA = -40°C					0.19	0.57	μA
			TA = +25°C					0.25	0.57	
			TA = +50°C					0.33	2.26	
			TA = +70°C					0.52	3.99	
			TA = +85°C					1.46	8.00	
			TA = +105°C					5.50	50.00	

(Notes and Remarks are listed on the next page.)

(4) Peripheral Functions (Common to all products)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fIL = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	
		DTC operation			3.10		

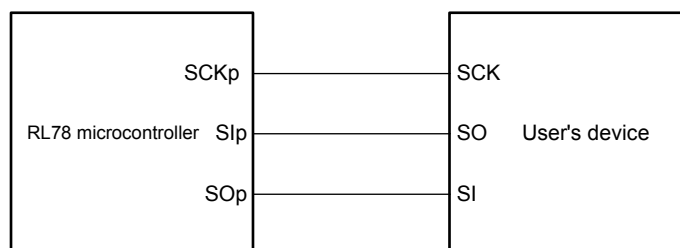
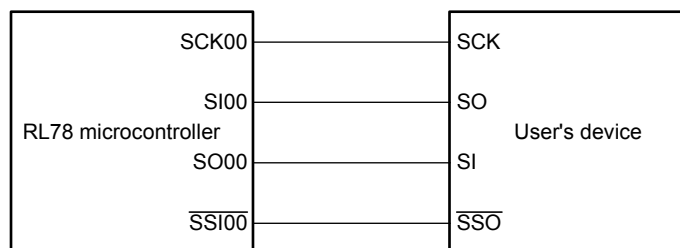
Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{\text{SSI00}}$ setup time	t_{SSIK}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
$\overline{\text{SSI00}}$ hold time	t_{kSSI}	DAPmn = 0	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 240$		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/f_{\text{MCK}} + 400$		ns
		DAPmn = 1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	240		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	400		ns

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)
CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))


Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V,

Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

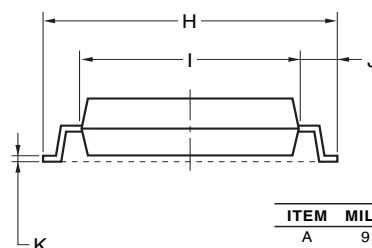
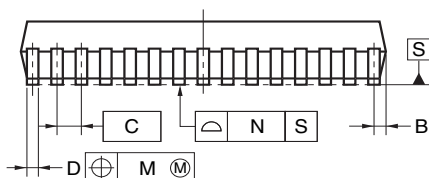
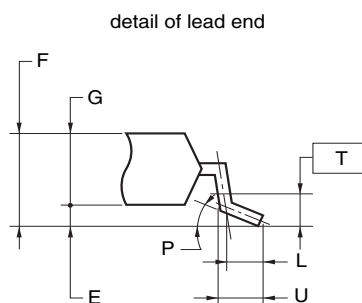
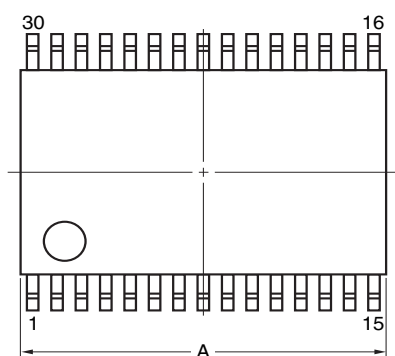
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
 R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
 R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

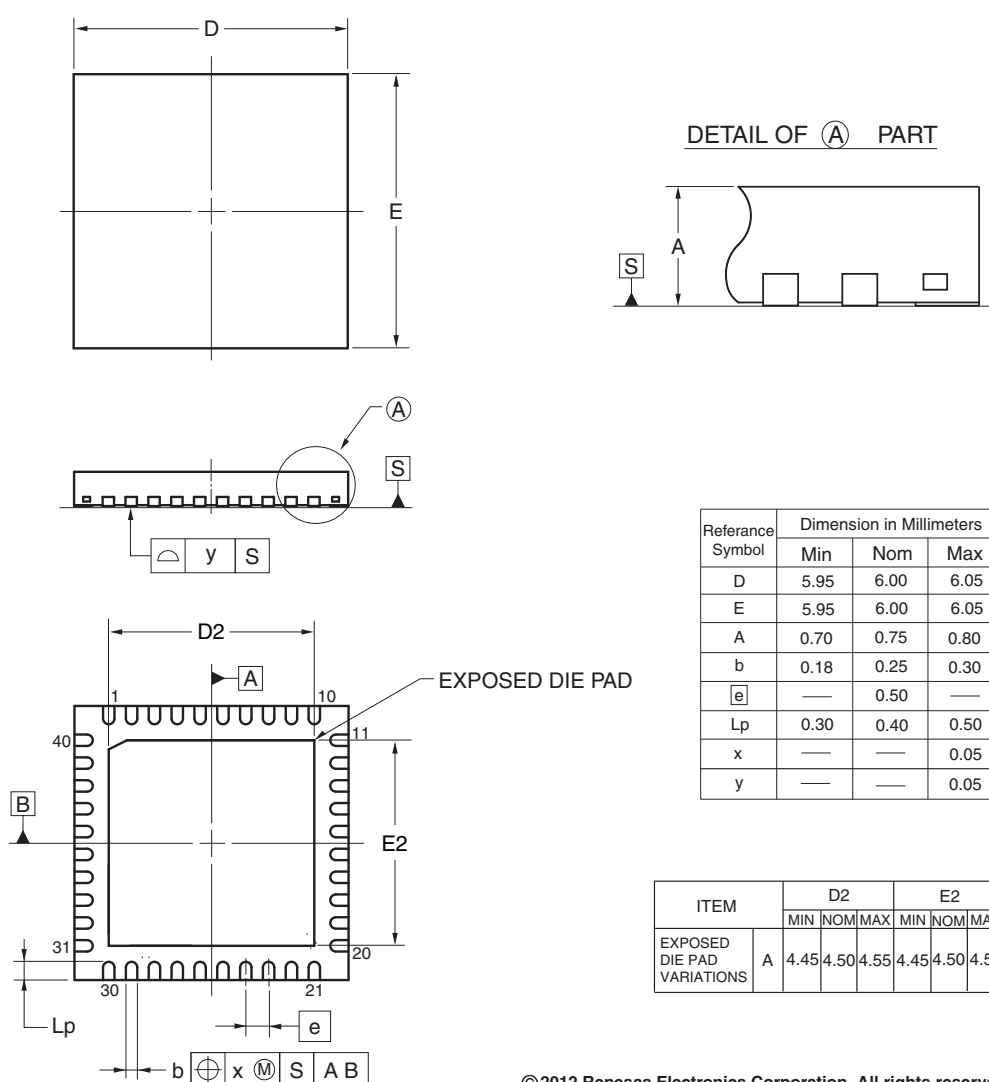
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

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4.4 40-pin products

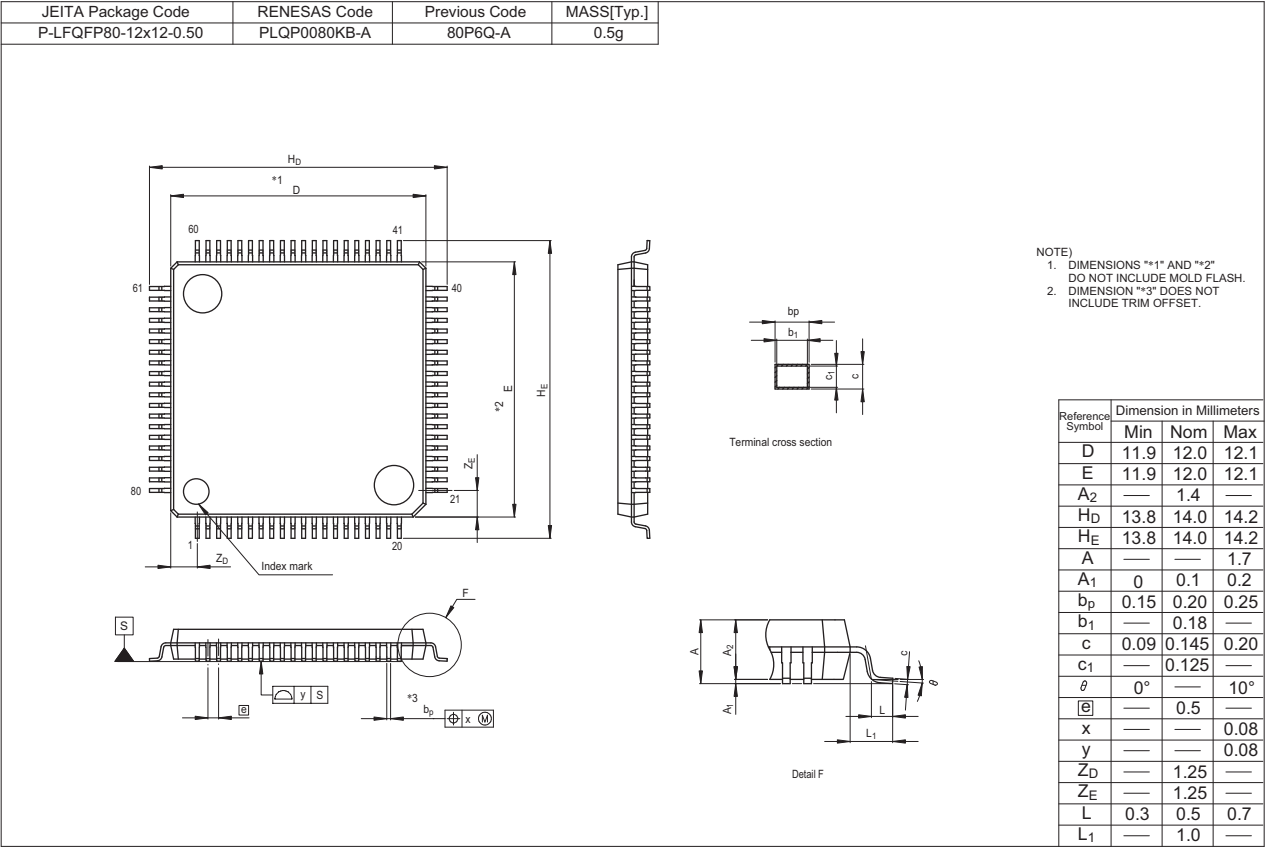
R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA,
 R5F104EHANA
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 R5F104EHDNA
 R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA,
 R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



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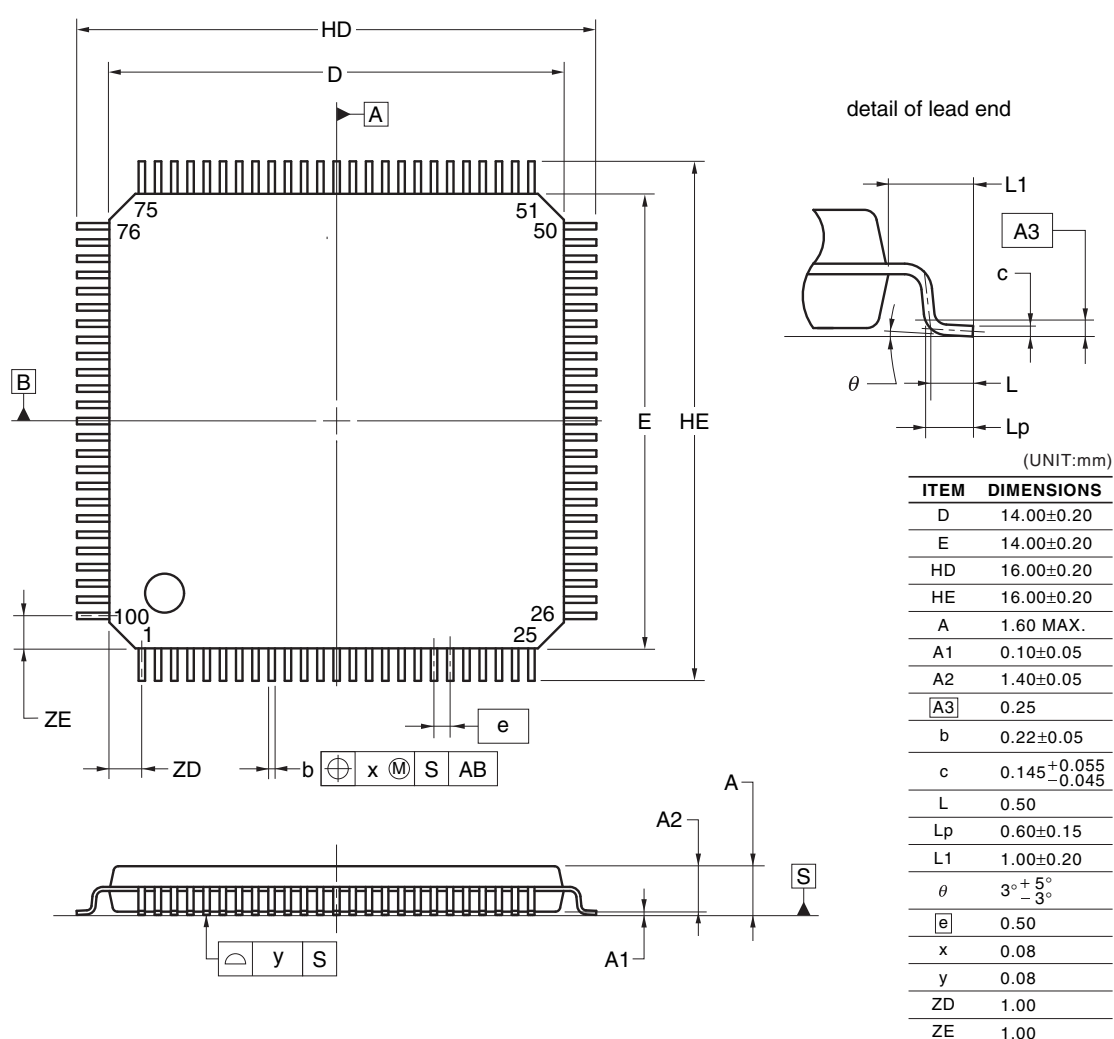
R5F104MKAFB, R5F104MLAFB
R5F104MKGFB, R5F104MLGFB



4.10 100-pin products

R5F104PFAFB, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB
 R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFB
 R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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