



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211a1dsp-u0

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/1A Group and Table 1.2 outlines the Functions and Specifications for R8C/1B Group.

Table 1.1 Functions and Specifications for R8C/1A Group

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	See Table 1.3 Product Information for R8C/1A Group
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits $\times$ 1 channel, timer Z: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits $\times$ 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Clock synchronous serial interface	1 channel I ² C bus Interface ⁽¹⁾ Clock synchronous serial I/O with chip select (SSU)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 11 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock oscillation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electric Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz)
	Current consumption	Typ. 9 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz, A/D converter stopped) Typ. 5 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz, A/D converter stopped) Typ. 35 μ A ($VCC = 3.0$ V, wait mode, peripheral clock off) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C
		-40 to 85°C (D version)
		-20 to 105°C (Y version) ⁽²⁾
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

NOTE:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Please contact Renesas Technology sales offices for the Y version.

1.4 Product Information

Table 1.3 lists Product Information for R8C/1A Group and Table 1.4 lists Product Information for R8C/1B Group.

Table 1.3 Product Information for R8C/1A Group

Current of October 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F211A1SP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F211A2SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DD	4 Kbytes	384 bytes	PRDP0020BA-A	
R5F211A2DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2NP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	
R5F211A1XXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	Factory programming product ⁽¹⁾
R5F211A2XXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3XXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4XXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DXXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DXXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1XXXDD	4 Kbytes	384 bytes	PRDP0020BA-A	Factory programming product ⁽¹⁾
R5F211A2XXXDD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3XXXDD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4XXXDD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2XXXNP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3XXXNP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4XXXNP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

NOTE:

1. The user ROM is programmed before shipment.

Table 1.4 Product Information for R8C/1B Group

Current of October 2006

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F211B1SP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F211B2SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	
R5F211B2DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	
R5F211B2DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3DD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	
R5F211B1XXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	Factory programming product ⁽¹⁾
R5F211B2XXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3XXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4XXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DXXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	
R5F211B2DXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DXXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1XXXDD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Factory programming product ⁽¹⁾
R5F211B2XXXDD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3XXXDD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4XXXDD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2XXXNP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3XXXNP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4XXXNP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

NOTE:

1. The user ROM is programmed before shipment.

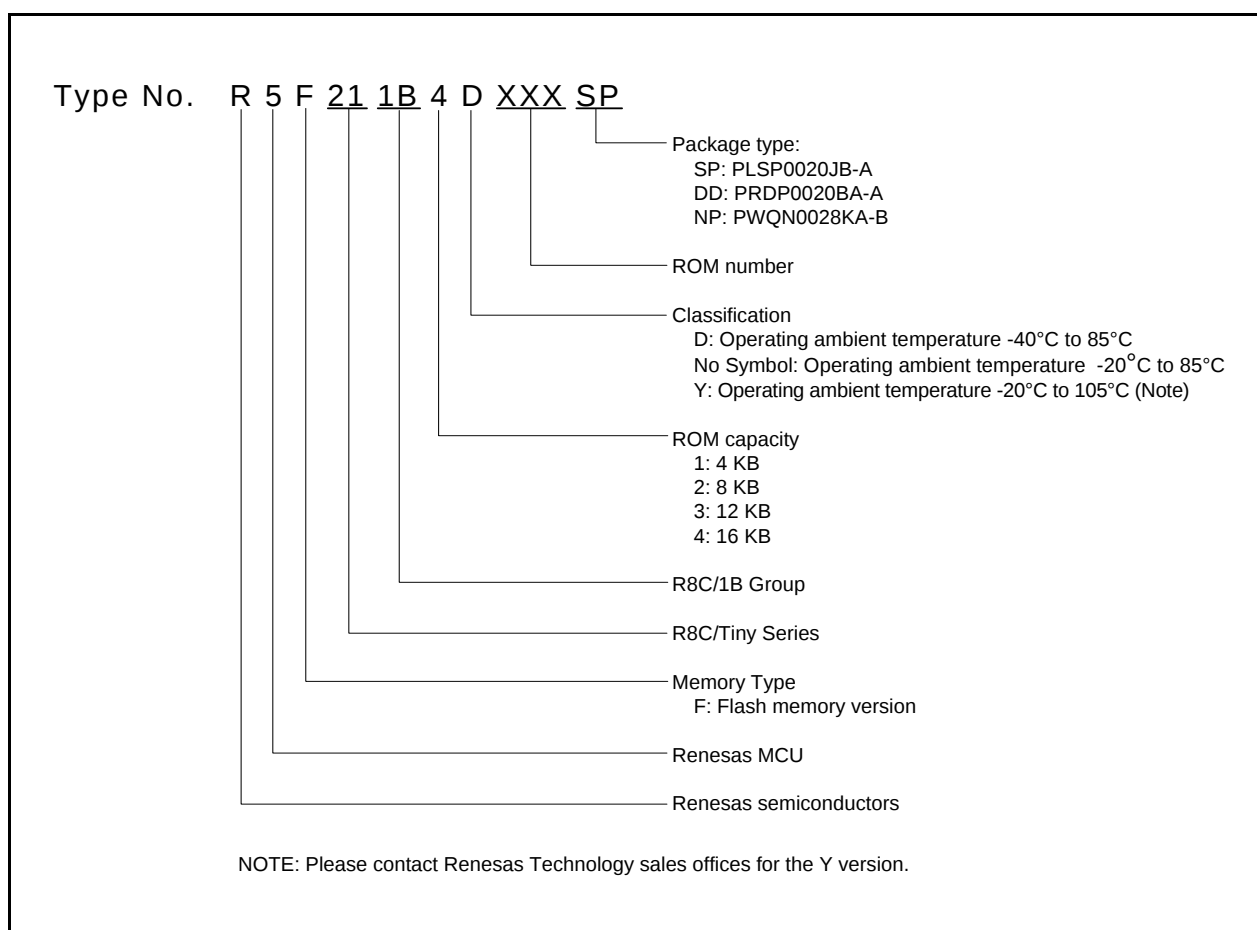


Figure 1.3 Type Number, Memory Size, and Package of R8C/1B Group

Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B Package

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C bus Interface	A/D Converter
1	NC							
2	XOUT	P4_7						
3	VSS/AVSS							
4	NC							
5	NC							
6	XIN	P4_6						
7	NC							
8	VCC/AVCC							
9	MODE							
10		P4_5	$\overline{\text{INT0}}$		RXD1			
11		P1_7	$\overline{\text{INT10}}$	CNTR00				
12		P1_6			CLK0	SSI01		
13		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0			
14		P1_4			TXD0			
15	NC							
16		P1_3	$\overline{\text{KI3}}$	TZOUT				AN11
17		P1_2	$\overline{\text{KI2}}$	CMP0_2				AN10
18	NC							
19	NC							
20	VREF	P4_2						
21	NC							
22		P1_1	$\overline{\text{KI1}}$	CMP0_1				AN9
23		P1_0	$\overline{\text{KI0}}$	CMP0_0				AN8
24		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		SSI00		
25		P3_4		CMP1_1		$\overline{\text{SCS}}$	SDA	
26		P3_5		CMP1_2		SSCK	SCL	
27		P3_7		$\overline{\text{CNTR0}}$	TXD1	SSO		
28	$\overline{\text{RESET}}$							

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/1B Group

Figure 3.2 is a Memory Map of R8C/1B Group. The R8C/1B Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

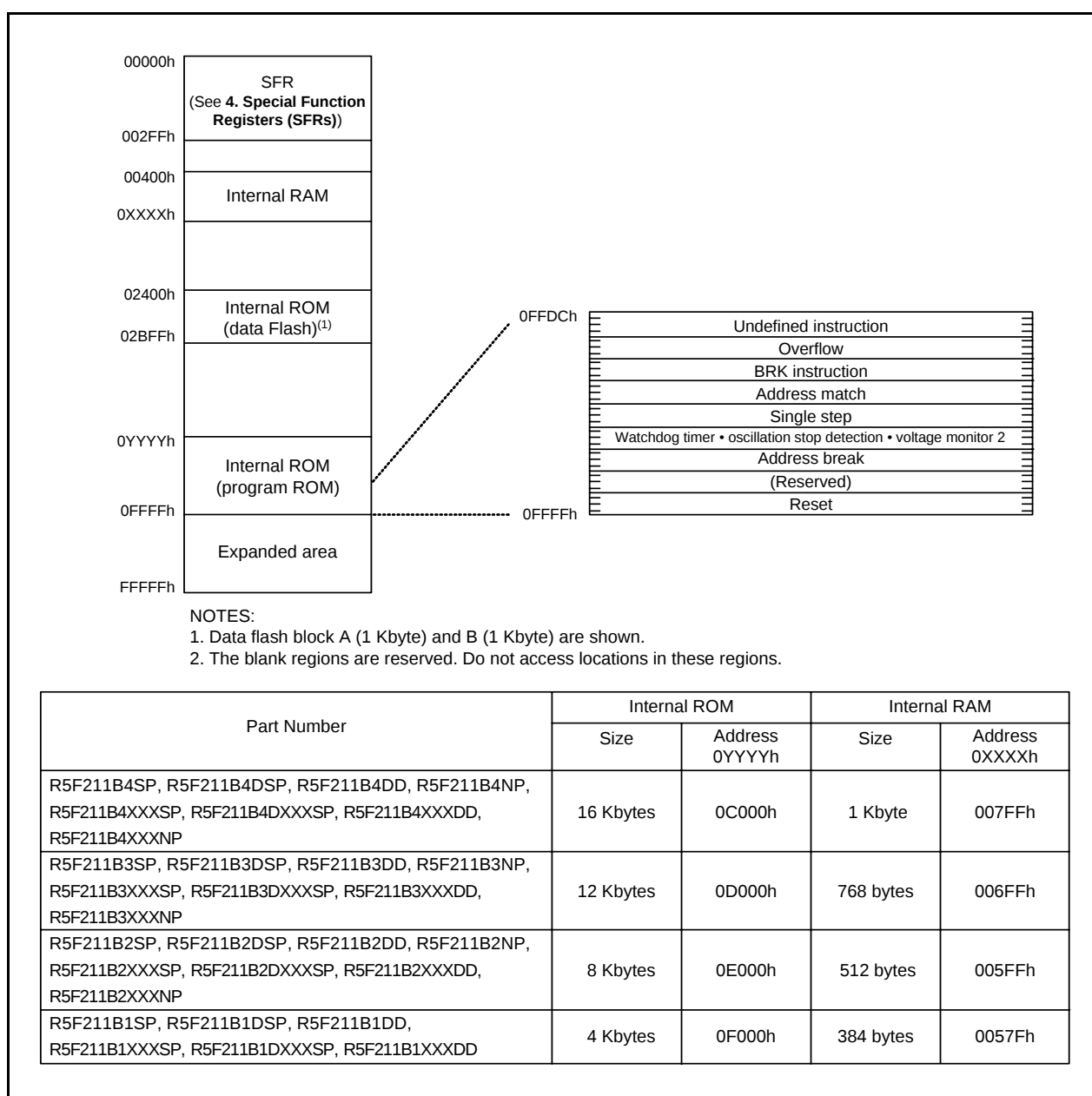


Figure 3.2 Memory Map of R8C/1B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OSD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 01000000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽²⁾	VW1C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh			
0090h	Timer C Register	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h			
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Ch	Capture, Compare 0 Register	TM0	0000h ⁽²⁾
009Dh	Compare 1 Register	TM1	FFFFh ⁽³⁾
009Eh			FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Generator	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			XXh
00A9h	UART1 Transmit/Receive Mode Register	U1MR	00h
00AAh	UART1 Bit Rate Generator	U1BRG	XXh
00ABh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h	UART Transmit/Receive Control Register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1 ⁽⁴⁾	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2 ⁽⁴⁾	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register ⁽⁴⁾	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register ⁽⁴⁾	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register ⁽⁴⁾	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register ⁽⁴⁾	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register ⁽⁴⁾	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register ⁽⁴⁾	SSRDR / ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In input capture mode.
3. In output compare mode.
4. Selected by the IICSEL bit in the PMR register.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{ref} = V_{CC}$	—	—	10	Bits
—	Absolute accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	—	—	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$	—	—	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = V_{CC}$	10	—	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	3.3	—	—	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$	2.8	—	—	μs
V_{ref}	Reference voltage			2.7	—	V_{CC}	V
V_{IA}	Analog input voltage ⁽⁴⁾			0	—	AV_{CC}	V
—	A/D operating clock frequency ⁽²⁾	Without sample and hold		0.25	—	10	MHz
		With sample and hold		1	—	10	MHz

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -20$ to $85 \text{ }^{\circ}\text{C}$ / -40 to $85 \text{ }^{\circ}\text{C}$, unless otherwise specified.
2. If f_1 exceeds 10 MHz , divide f_1 and ensure the A/D operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AV_{CC} is less than 4.2 V , divide f_1 and ensure the A/D operating clock frequency (ϕ_{AD}) is $f_1/2$ or below.
4. When the analog input voltage is over the reference voltage, the A/D conversion result will be $3FFh$ in 10-bit mode and FFh in 8-bit mode.

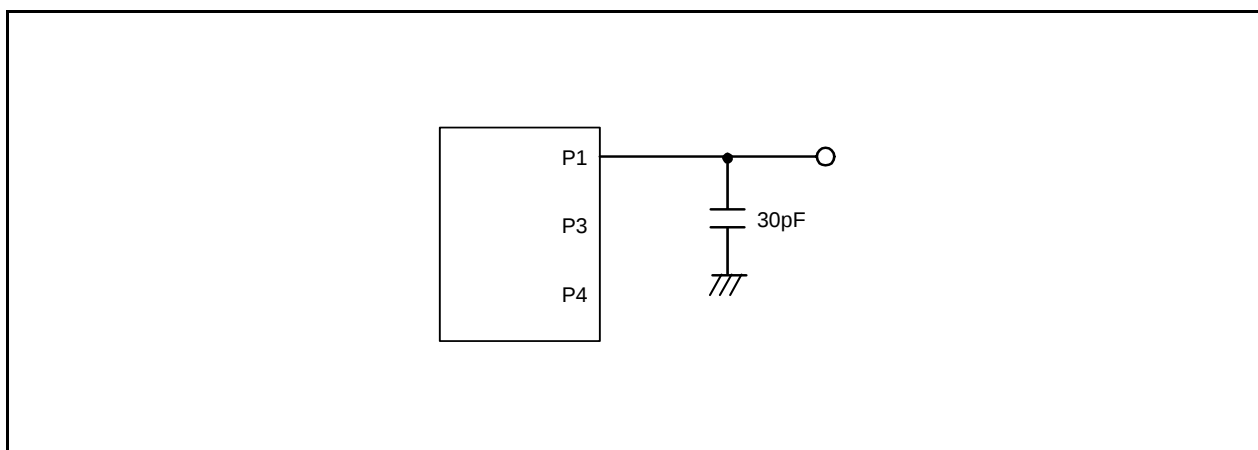
**Figure 5.1 Port P1, P3, and P4 Measurement Circuit**

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	—	—	V _{det1}	V
t _w (V _{por2} -V _{det1})	Supply voltage rising time when power-on reset is deasserted ⁽¹⁾	-20°C ≤ Topr ≤ 85°C, t _w (por2) ≥ 0s ⁽³⁾	—	—	100	ms

NOTES:

1. This condition is not applicable when using with V_{cc} ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds 10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. t_w(por2) is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	—	—	0.1	V
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, t _w (por1) ≥ 10 s ⁽²⁾	—	—	100	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, t _w (por1) ≥ 30 s ⁽²⁾	—	—	100	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, t _w (por1) ≥ 10 s ⁽²⁾	—	—	1	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, t _w (por1) ≥ 1 s ⁽²⁾	—	—	0.5	ms

NOTES:

1. When not using voltage monitor 1, use with V_{cc} ≥ 2.7 V.
2. t_w(por1) is the time to hold the external power below effective voltage (V_{por1}).

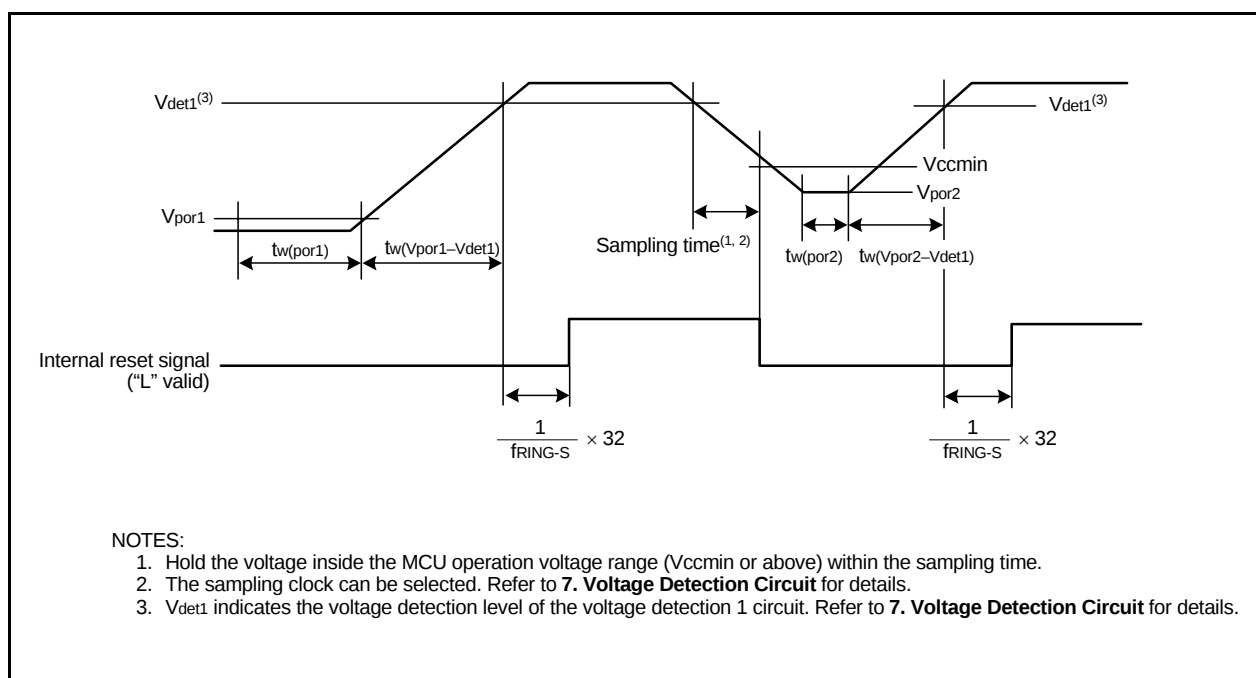
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency when the reset is deasserted	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	8	—	MHz
—	High-speed on-chip oscillator frequency temperature • supply voltage dependence ⁽²⁾	0 to +60 $^{\circ}\text{C}$ /5 V $\pm$ 5 % ⁽³⁾	7.76	—	8.24	MHz
		-20 to +85 $^{\circ}\text{C}$ /2.7 to 5.5 V ⁽³⁾	7.68	—	8.32	MHz
		-40 to +85 $^{\circ}\text{C}$ /2.7 to 5.5 V ⁽³⁾	7.44	—	8.32	MHz

NOTES:

1. The measurement condition is $V_{CC} = 5.0 \text{ V}$ and $T_{opr} = 25 \text{ }^{\circ}\text{C}$.
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on ⁽²⁾		1	—	2000	μs
$t_{d(R-S)}$	STOP exit time ⁽³⁾		—	—	150	μs

NOTES:

1. The measurement condition is $V_{CC} = 2.7$ to 5.5 V and $T_{opr} = 25 \text{ }^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	SCS setup time	Slave		1tcyc+50	–	–	ns
t _{LAG}	SCS hold time	Slave		1tcyc+50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time			–	–	1.5tcyc+100	ns
t _{OR}	SSI slave out open time			–	–	1.5tcyc+100	ns

NOTES:

1. V_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Ta = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Table 5.13 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} +600(2)	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{CYC} +300(2)	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{CYC} +300(2)	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{CYC} (2)	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} (2)	—	—	ns
t _{STAH}	Start condition input hold time		3t _{CYC} (2)	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} (2)	—	—	ns
t _{STOS}	Stop condition input setup time		3t _{CYC} (2)	—	—	ns
t _{SDAS}	Data input setup time		1t _{CYC} +20(2)	—	—	ns
t _{SDAH}	Data input hold time		0	—	—	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V and T_a = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

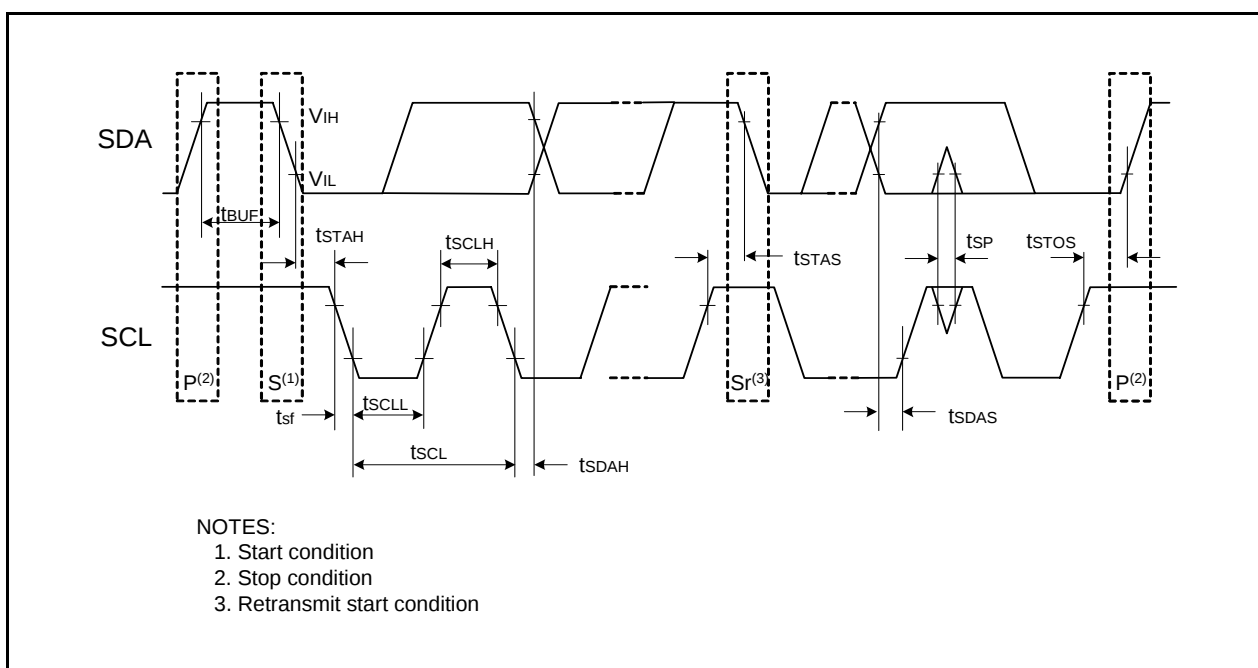
**Figure 5.7** I/O Timing of I²C bus Interface

Table 5.14 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except X _{OUT}	I _{OH} = -5 mA		V _{CC} - 2.0	—	V _{CC}	V
			I _{OH} = -200 μA		V _{CC} - 0.3	—	V _{CC}	V
		X _{OUT}	Drive capacity HIGH	I _{OH} = -1 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -500 μA	V _{CC} - 2.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_3, X _{OUT}	I _{OL} = 5 mA		—	—	2.0	V
			I _{OL} = 200 μA		—	—	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	I _{OL} = 15 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 5 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 200 μA	—	—	0.45	V
		X _{OUT}	Drive capacity HIGH	I _{OL} = 1 mA	—	—	2.0	V
			Drive capacity LOW	I _{OL} = 500 μA	—	—	2.0	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0			0.2	—	1.0	V
		RESET			0.2	—	2.2	V
I _{IH}	Input "H" current		V _I = 5 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN			—	1.0	—	MΩ
f _{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM hold voltage		During stop mode		2.0	—	—	V

NOTE:

- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.

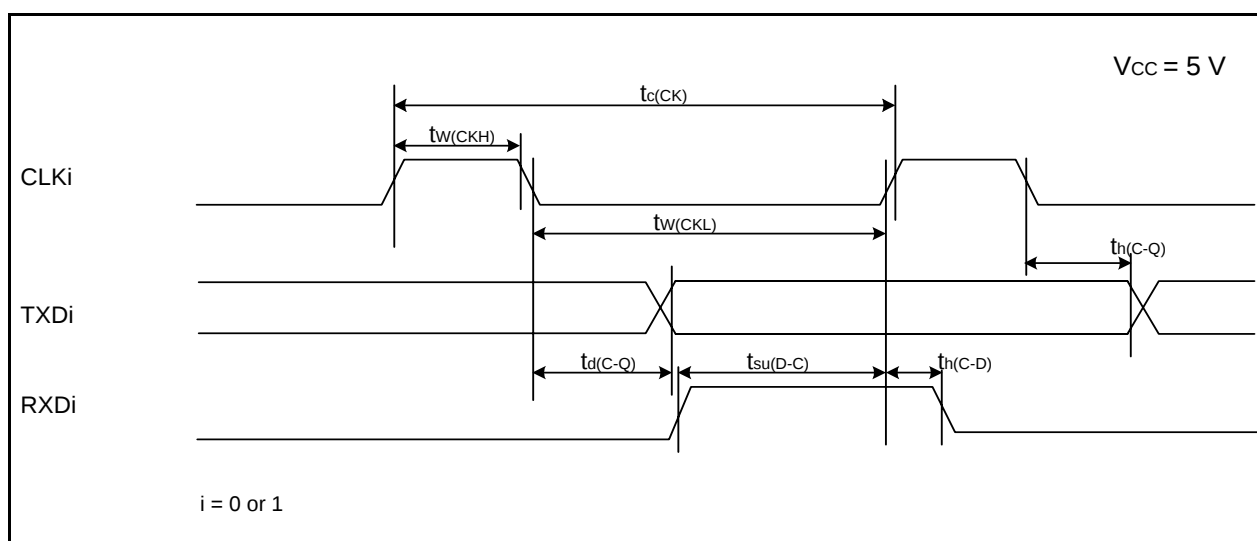
Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss, A/D converter is stopped	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8	14	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
		Medium-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	110	300	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	–	40	80	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	–	38	76	μA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	–	0.8	3.0	μA

Table 5.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

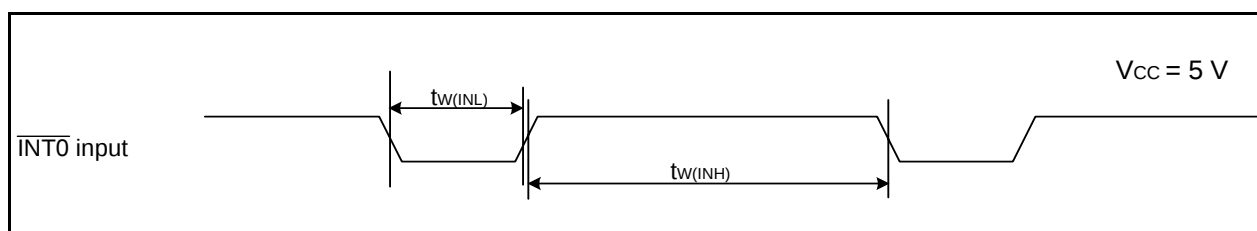
i = 0 or 1

**Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.20 External Interrupt $\overline{INT0}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	250 ⁽²⁾	—	ns

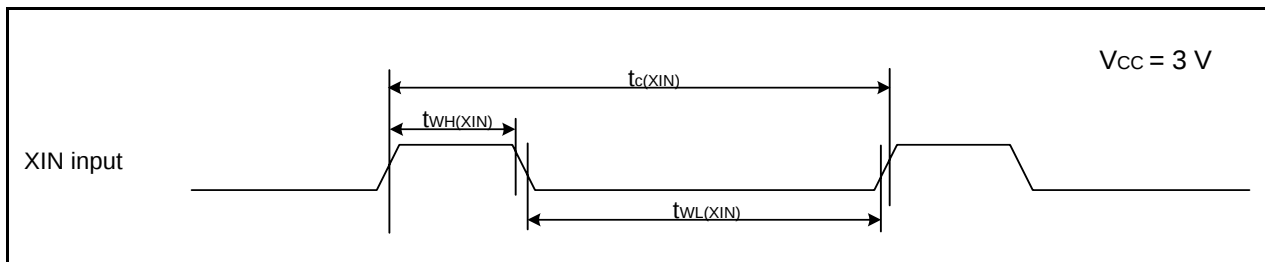
NOTES:

- When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

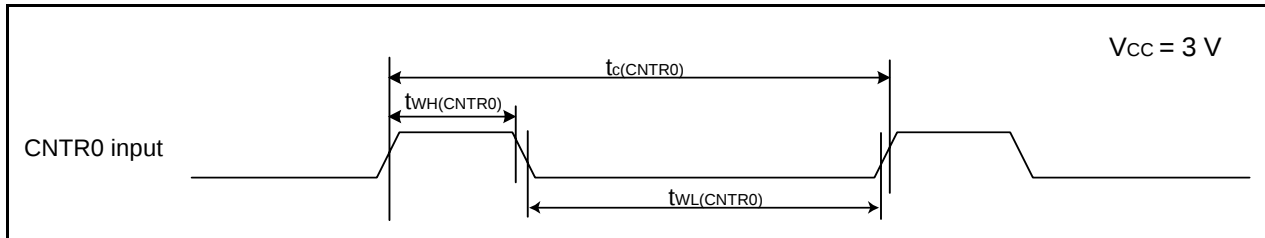
**Figure 5.12 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 5 V**

Timing requirements (Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_a = 25\text{ }^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]**Table 5.23 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	—	ns
$t_{WH(XIN)}$	XIN input "H" width	40	—	ns
$t_{WL(XIN)}$	XIN input "L" width	40	—	ns

**Figure 5.13 XIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.24 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input**

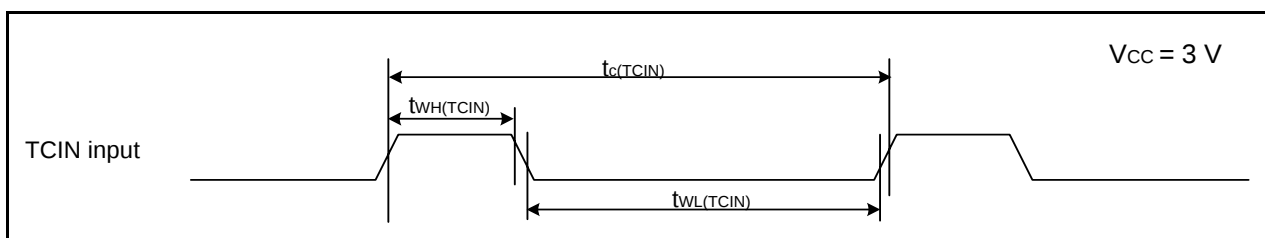
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	300	—	ns
$t_{WH(CNTR0)}$	CNTR0 input "H" width	120	—	ns
$t_{WL(CNTR0)}$	CNTR0 input "L" width	120	—	ns

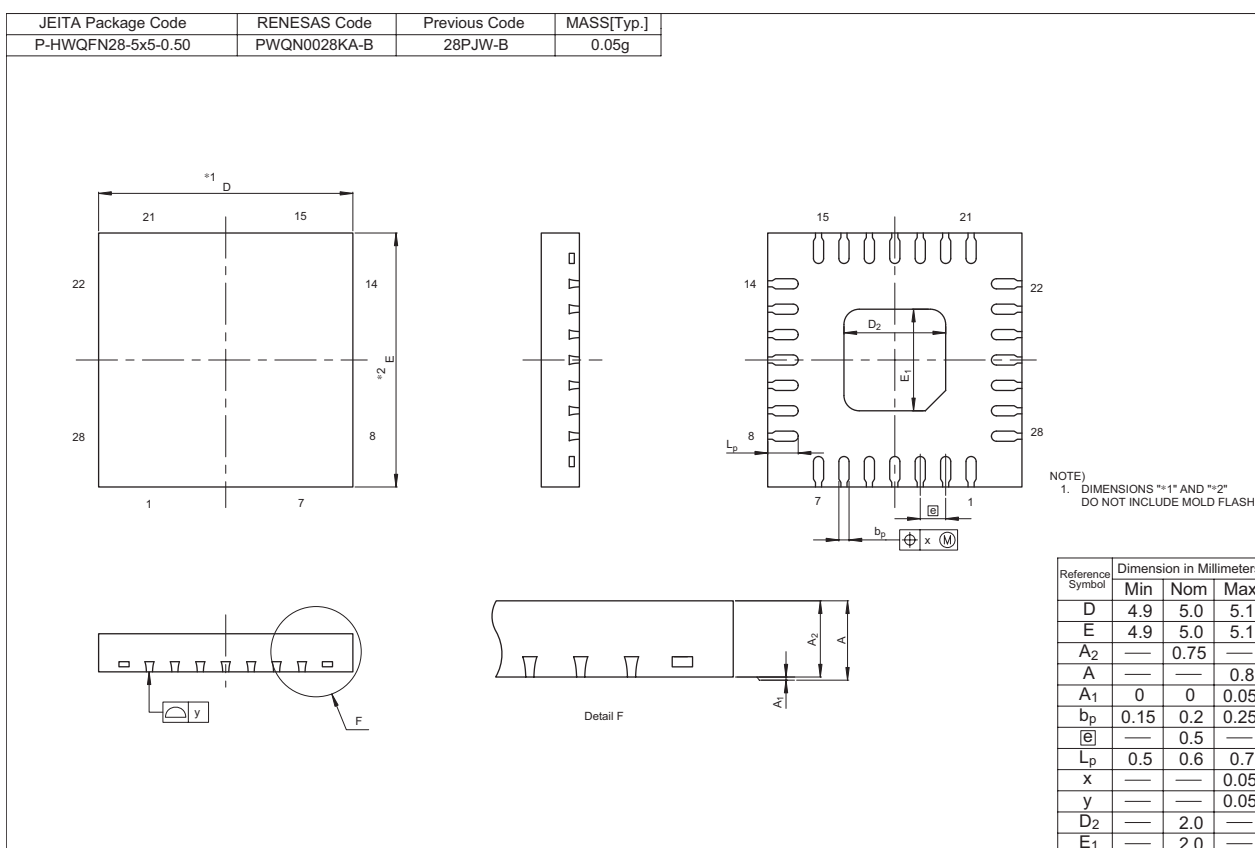
**Figure 5.14 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.25 TCIN Input, $\overline{INT3}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	1,200 ⁽¹⁾	—	ns
$t_{WH(TCIN)}$	TCIN input "H" width	600 ⁽²⁾	—	ns
$t_{WL(TCIN)}$	TCIN input "L" width	600 ⁽²⁾	—	ns

NOTES:

1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency x 1.5) or above.

**Figure 5.15 TCIN Input, $\overline{INT3}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$**



REVISION HISTORY

R8C/1A Group, R8C/1B Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 01, 2005	18	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.3 A/D Converter Characteristics; V _{ref} and V _{IA} : Standard value, NOTE4 revised
		22	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; NOTES3 and 5 revised, NOTE8 deleted
		23	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTES1 and 3 revised
		25	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised
		26	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; "High-Speed On-Chip Oscillator ..." → "High-Speed On-Chip Oscillator Frequency ..." revised, NOTE2 added
		33	Table 5.15 Electrical Characteristics (2) [V _{cc} = 5V]; NOTE1 deleted
		37	Table 5.22 Electrical Characteristics (4) [V _{cc} = 3V]; NOTE1 deleted
1.10	Dec 16, 2005	–	Products of PWQN0028KA-B package included
		5, 6	Table 1.3, Table 1.4 revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; NOTE 8 added, T _{opr} → Ambient temperature
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTE 9 added, T _{opr} → Ambient temperature
		28	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; NOTE 3 added
		29	Table 5.12; t _{SA} and t _{OR} revised, NOTE: 1. V _{CC} = 2.2 to → 2.7 to
		33	Table 5.13; NOTE: 1. V _{CC} = 2.2 to → 2.7 to
		35, 39	Table 5.15, Table 5.22; The title revised, Condition of Stop Mode added
1.20	Mar 31, 2006	37, 41	Table 5.19, Table 5.26; t _d (C-Q) and t _{su} (D-C) revised
		42, 43	Package Dimensions revised
1.20	Mar 31, 2006	5, 6	Table 1.3, Table 1.4; Type No. added, deleted
		16, 17	Figure 3.1, Figure 3.2; Part Number added, deleted
		24, 25	Table 5.4, Table 5.5; Conditions: V _{CC} = 5.0 V at T _{opr} = 25 °C deleted,
1.30	Oct 03, 2006	all pages	Y version added Factory programming product added