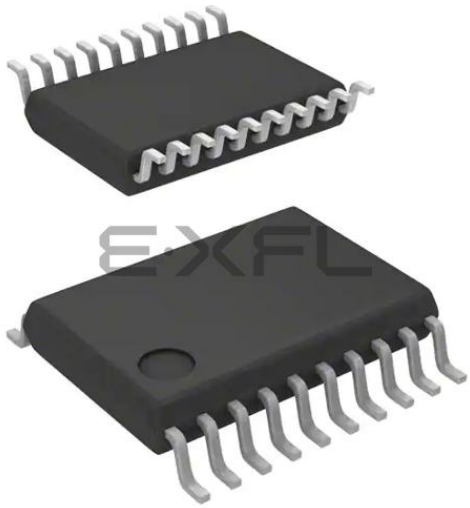

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211a3dsp-u0

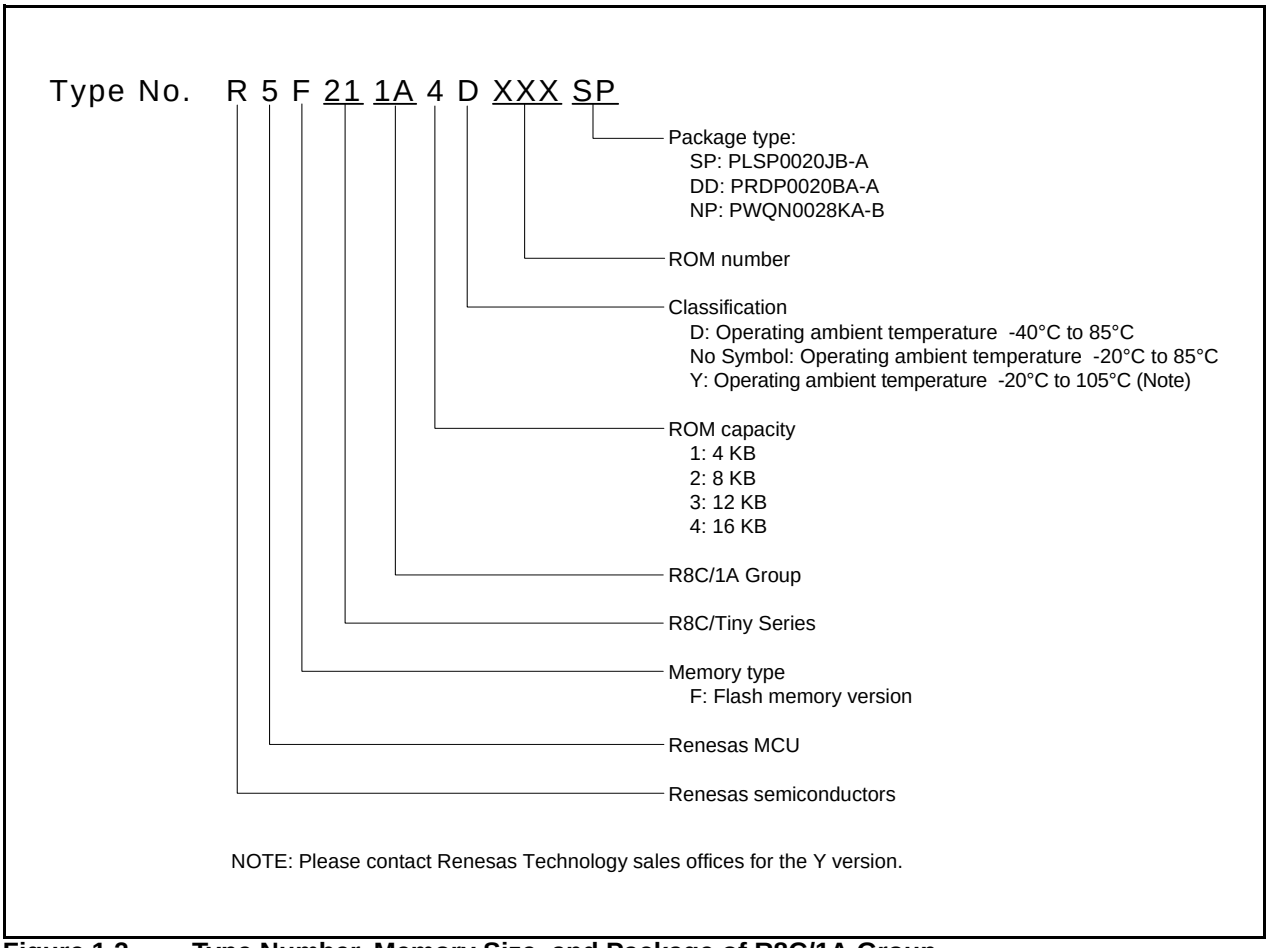


Figure 1.2 Type Number, Memory Size, and Package of R8C/1A Group

1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A Packages and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B Package.

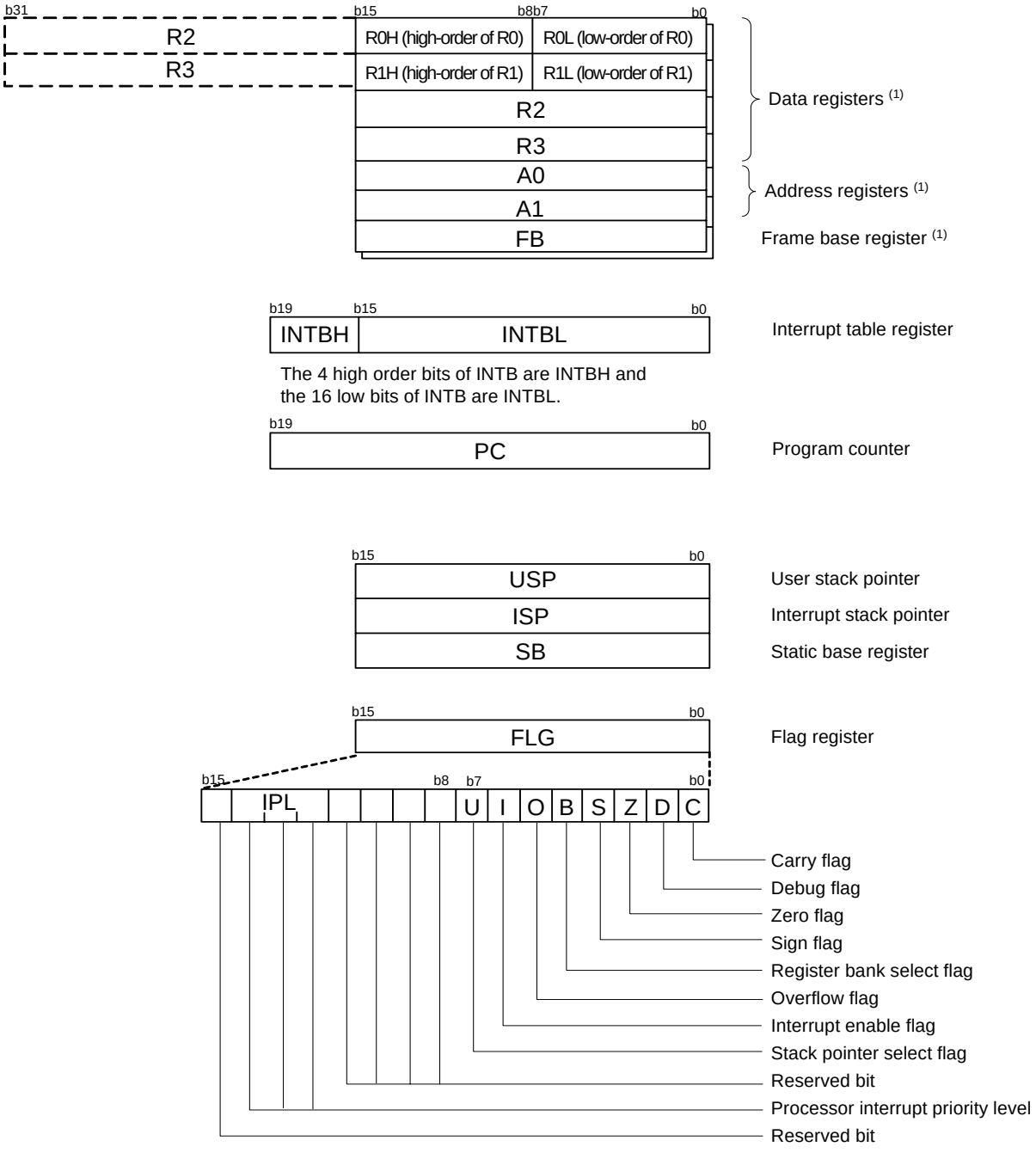
Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Power supply for the A/D converter Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main Clock Input	XIN	I	These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
Main Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	INT interrupt input pins
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	O	Timer C output pins
Serial Interface	CLK0	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
Clock synchronous serial I/O with chip select (SSU)	SSI00, SSI01	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
I^2C bus Interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter
A/D Converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O Port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_3 also function as LED drive ports.
Input Port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

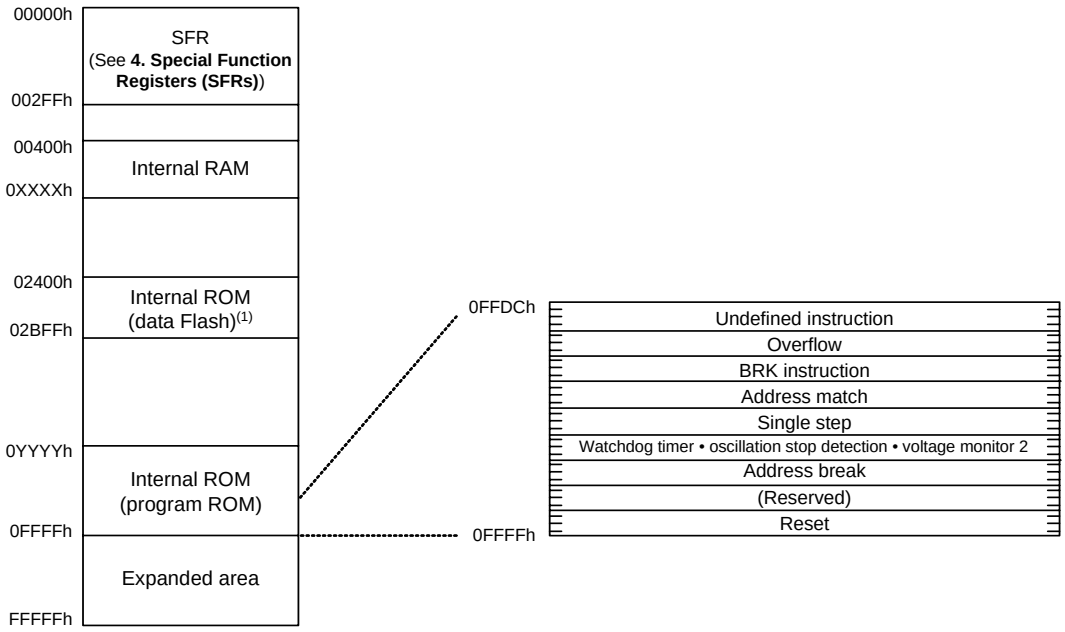


NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Register

3.2 R8C/1B Group

Figure 3.2 is a Memory Map of R8C/1B Group. The R8C/1B Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F211B4SP, R5F211B4DSP, R5F211B4DD, R5F211B4NP, R5F211B4XXXSP, R5F211B4DXXXSP, R5F211B4XXXDD, R5F211B4XXXNP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F211B3SP, R5F211B3DSP, R5F211B3DD, R5F211B3NP, R5F211B3XXXSP, R5F211B3DXXXSP, R5F211B3XXXDD, R5F211B3XXXNP	12 Kbytes	0D000h	768 bytes	006FFh
R5F211B2SP, R5F211B2DSP, R5F211B2DD, R5F211B2NP, R5F211B2XXXSP, R5F211B2DXXXSP, R5F211B2XXXDD, R5F211B2XXXNP	8 Kbytes	0E000h	512 bytes	005FFh
R5F211B1SP, R5F211B1DSP, R5F211B1DD, R5F211B1XXXSP, R5F211B1DXXXSP, R5F211B1XXXDD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.2 Memory Map of R8C/1B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	$\overline{\text{INT0}}$ Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register [2]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register [5]	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh			
0090h	Timer C Register	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h			
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Ch	Capture, Compare 0 Register	TM0	0000h(2)
009Dh			FFFFh(3)
009Eh	Compare 1 Register	TM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Generator	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Generator	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h	UART Transmit/Receive Control Register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1(4)	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2(4)	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register(4)	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register(4)	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register(4)	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register(4)	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register(4)	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register(4)	SSRDR / ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. In input capture mode.
3. In output compare mode.
4. Selected by the IICSEL bit in the PMR register.

5. Electrical Characteristics

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = -20°C to 105°C).

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	–	5.5	V
AV_{CC}	Analog supply voltage			–	V_{CC}	–	V
V_{SS}	Supply voltage			–	0	–	V
AV_{SS}	Analog supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	30	mA
			Drive capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average output “L” current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	15	mA
			Drive capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 Main clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	HRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			HRA01 = 1 High-speed on-chip oscillator clock selected	–	8	–	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = V_{CC}	–	–	10	Bits
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = V_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	Vcc	V
V_{IA}	Analog input voltage(4)			0	–	AVcc	V
–	A/D operating clock frequency(2)	Without sample and hold		0.25	–	10	MHz
		With sample and hold		1	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is f1/2 or below.
4. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

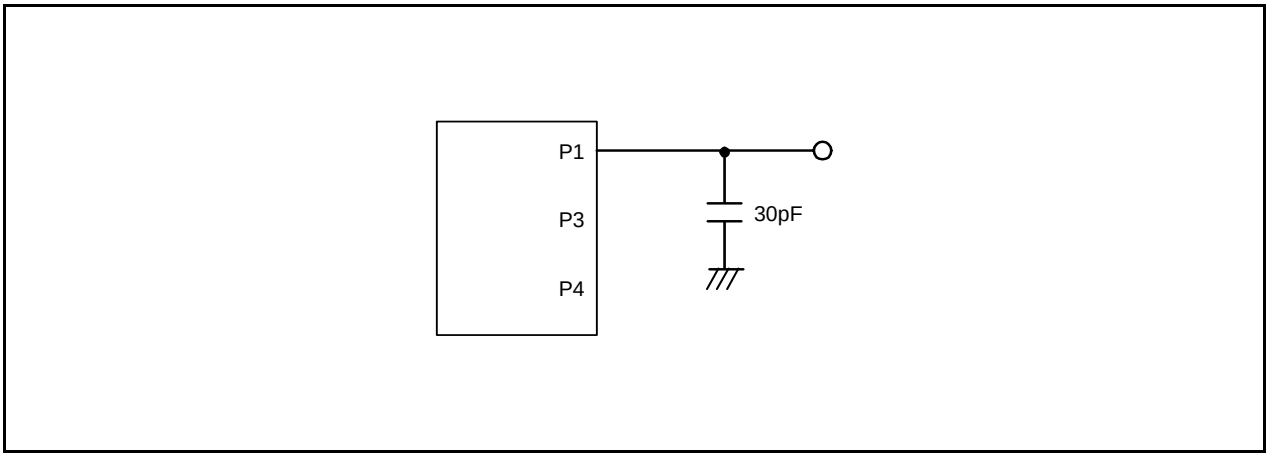


Figure 5.1 Port P1, P3, and P4 Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/1A Group	100(3)	–	–	times
		R8C/1B Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(8)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time Delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85 °C / –40 to 85 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

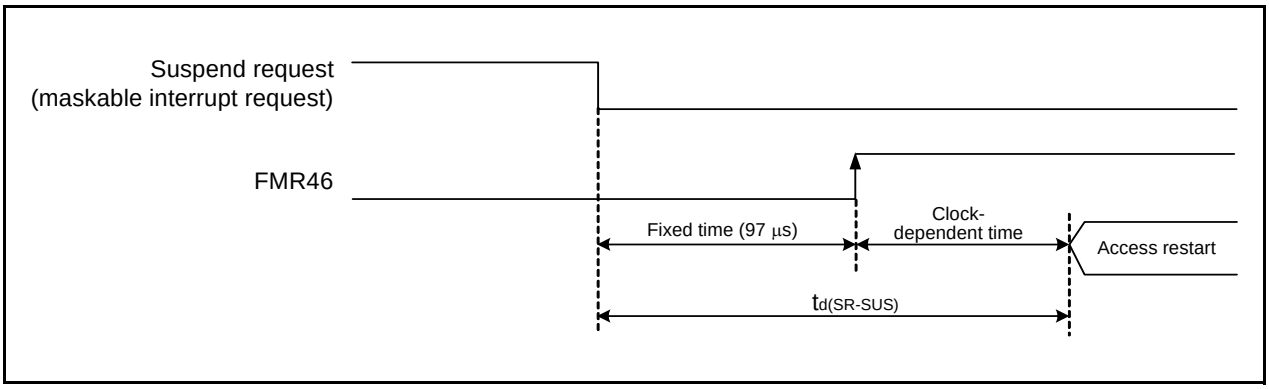


Figure 5.2 Transition Time to Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3)		2.70	2.85	3.00	V
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Ensure that $V_{det2} > V_{det1}$.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.00	3.30	3.60	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Ensure that $V_{det2} > V_{det1}$.

Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency when the reset is deasserted	V_{CC} = 5.0 V, T_{opr} = 25 °C	–	8	–	MHz
–	High-speed on-chip oscillator frequency temperature • supply voltage dependence(2)	0 to +60 °C/5 V ± 5 %(3)	7.76	–	8.24	MHz
		-20 to +85 °C/2.7 to 5.5 V(3)	7.68	–	8.32	MHz
		-40 to +85 °C/2.7 to 5.5 V(3)	7.44	–	8.32	MHz

NOTES:
1. The measurement condition is V_{CC} = 5.0 V and T_{opr} = 25 °C.
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

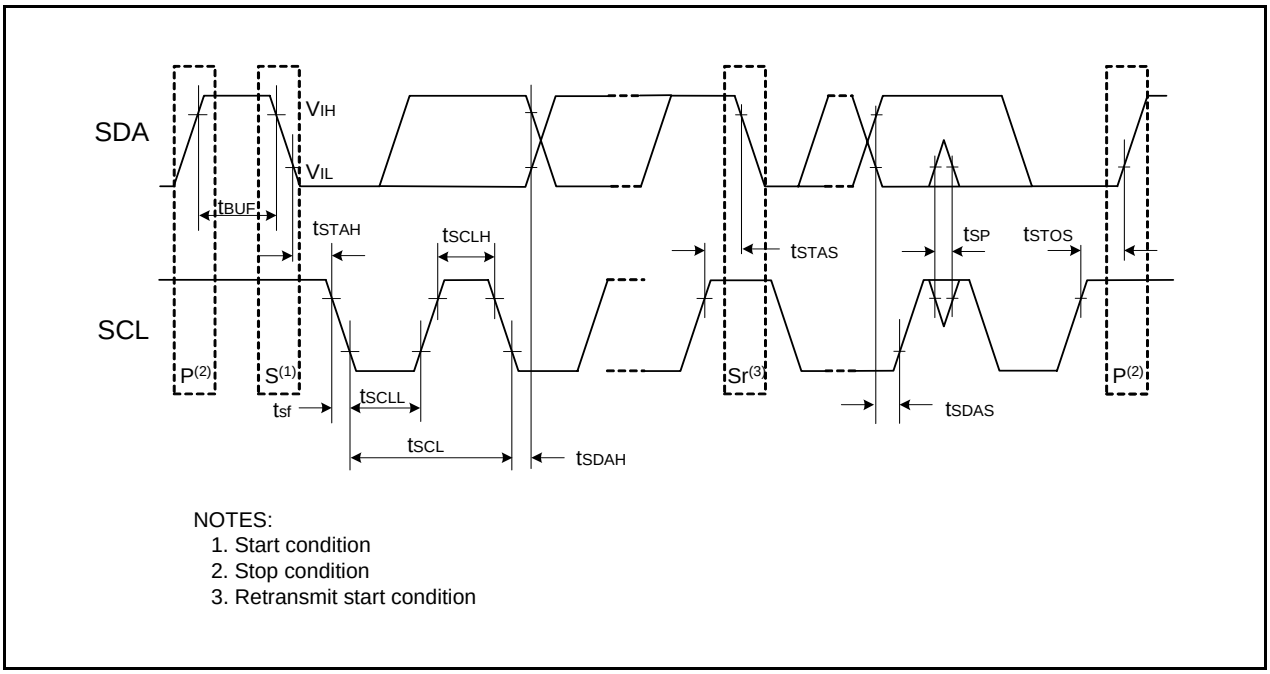
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC}+50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC}+50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1.5t_{CYC}+100	ns
t_{OR}	SSI slave out open time			–	–	1.5t_{CYC}+100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Ta = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Table 5.13 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}+600^{(2)}$	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}+300^{(2)}$	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}+300^{(2)}$	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}^{(2)}$	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}^{(2)}$	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STOS}	Stop condition input setup time		$3t_{CYC}^{(2)}$	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC}+20^{(2)}$	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V and Ta = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}, A/D converter is stopped	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8	14	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
		Medium-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	110	300	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	–	40	80	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	–	38	76	µA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	–	0.8	3.0	µA

Table 5.21 Electrical Characteristics (3) [Vcc = 3V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except X_{OUT}	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 µA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 1 mA		–	–	0.5	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0			0.2	–	0.8	V
		$\overline{RESET}$			0.2	–	1.8	V
I_{IH}	Input “H” current		VI = 3 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN) = 10 MHz, unless otherwise specified.

Timing requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Ta = 25 °C) [Vcc = 3 V]

Table 5.23 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

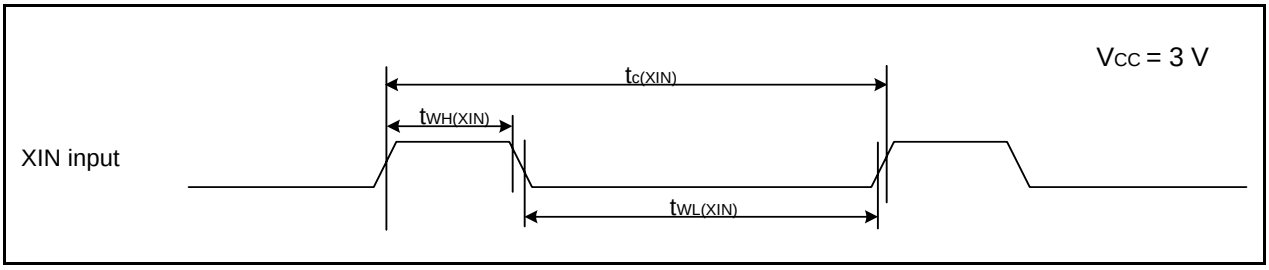


Figure 5.13 XIN Input Timing Diagram when Vcc = 3 V

Table 5.24 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	120	–	ns

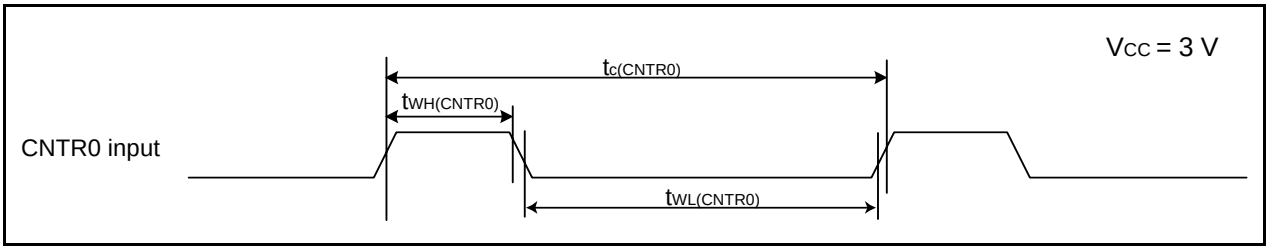


Figure 5.14 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 3 V

Table 5.25 TCIN Input, $\overline{\text{INT3}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	600(2)	–	ns

NOTES:
1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency x 1.5) or above.

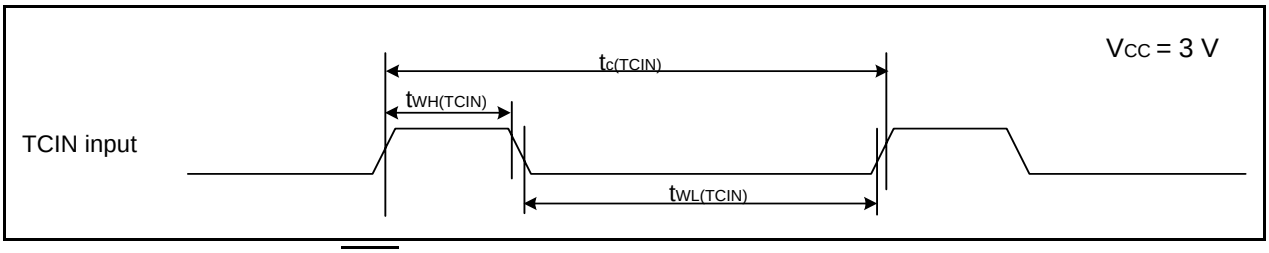


Figure 5.15 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

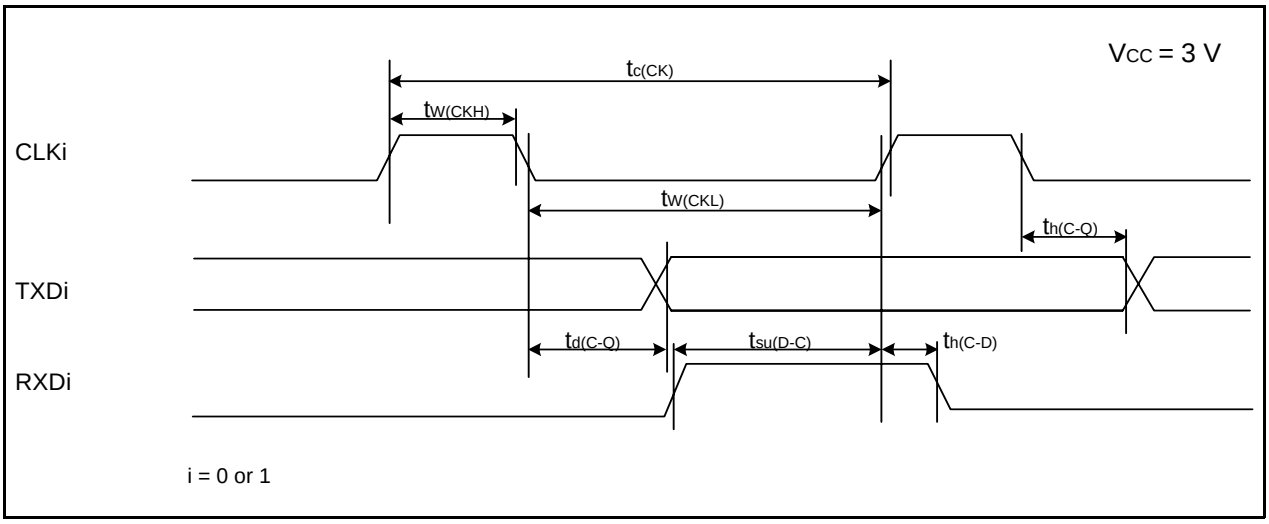


Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater

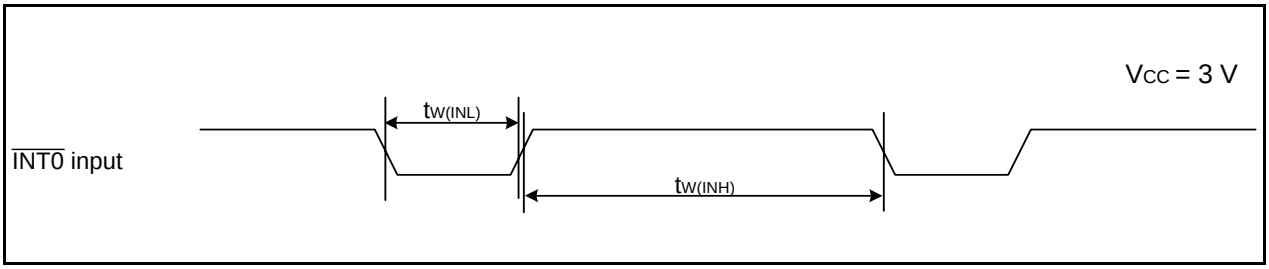


Figure 5.17 External Interrupt $\overline{INT0}$ Input Timing Diagram when VCC = 3 V

REVISION HISTORY	R8C/1A Group, R8C/1B Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 01, 2005	18	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.3 A/D Converter Characteristics; V_{ref} and V_{IA}: Standard value, NOTE4 revised
		22	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; NOTES3 and 5 revised, NOTE8 deleted
		23	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTES1 and 3 revised
		25	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised
		26	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; "High-Speed On-Chip Oscillator ..." → "High-Speed On-Chip Oscillator Frequency ..." revised, NOTE2 added
		33	Table 5.15 Electrical Characteristics (2) [Vcc = 5V]; NOTE1 deleted
		37	Table 5.22 Electrical Characteristics (4) [Vcc = 3V]; NOTE1 deleted
1.10	Dec 16, 2005	–	Products of PWQN0028KA-B package included
		5, 6	Table 1.3, Table 1.4 revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; NOTE 8 added, Topr → Ambient temperature
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTE 9 added, Topr → Ambient temperature
		28	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; NOTE 3 added
		29	Table 5.12; tSA and tOR revised, NOTE: 1. VCC = 2.2 to → 2.7 to
		33	Table 5.13; NOTE: 1. VCC = 2.2 to → 2.7 to
		35, 39	Table 5.15, Table 5.22; The title revised, Condition of Stop Mode added
		37, 41	Table 5.19, Table 5.26; td(C-Q) and tsu(D-C) revised
		42, 43	Package Dimensions revised
1.20	Mar 31, 2006	5, 6	Table 1.3, Table 1.4; Type No. added, deleted
		16, 17	Figure 3.1, Figure 3.2; Part Number added, deleted
		24, 25	Table 5.4, Table 5.5; Conditions: VCC = 5.0 V at Topr = 25 °C deleted,
1.30	Oct 03, 2006	all pages	Y version added Factory programming product added

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