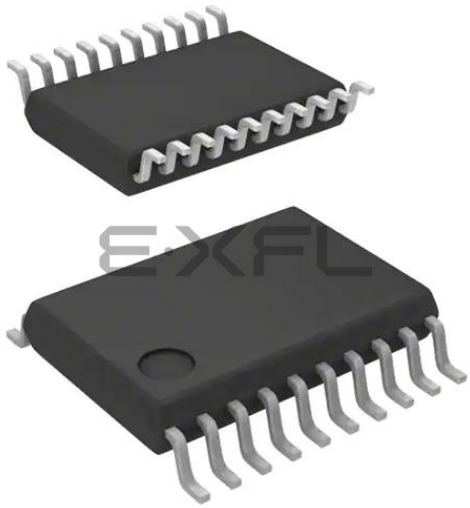

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211b2dsp-u0

1. Overview

These MCUs are fabricated using the high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/1B Group has on-chip data flash ROM (1 KB × 2 blocks).
The difference between the R8C/1A Group and R8C/1B Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), portable equipment, general industrial equipment, audio equipment, etc.

Table 1.2 Functions and Specifications for R8C/1B Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	See **Table 1.4 Product Information for R8C/1B Group**
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Clock synchronous serial interface	1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select (SSU)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 11 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power on reset circuit	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, A/D converter stopped) Typ. 5 mA (VCC = 3.0 V, f(XIN) = 10 MHz, A/D converter stopped) Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version) -20 to 105°C (Y version) (2)
Package		20-pin molded-plastic LSSOP 20-pin molded-plastic SDIP 28-pin molded-plastic HWQFN

NOTE:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Please contact Renesas Technology sales offices for the Y version.

1.4 Product Information

Table 1.3 lists Product Information for R8C/1A Group and Table 1.4 lists Product Information for R8C/1B Group.

Table 1.3 Product Information for R8C/1A Group Current of October 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F211A1SP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F211A2SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DD	4 Kbytes	384 bytes	PRDP0020BA-A	
R5F211A2DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2NP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	
R5F211A1XXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	Factory programming product (1)
R5F211A2XXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3XXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4XXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DXXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DXXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1XXXDD	4 Kbytes	384 bytes	PRDP0020BA-A	Factory programming product (1)
R5F211A2XXXDD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3XXXDD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4XXXDD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2XXXNP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3XXXNP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4XXXNP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

NOTE:
1. The user ROM is programmed before shipment.

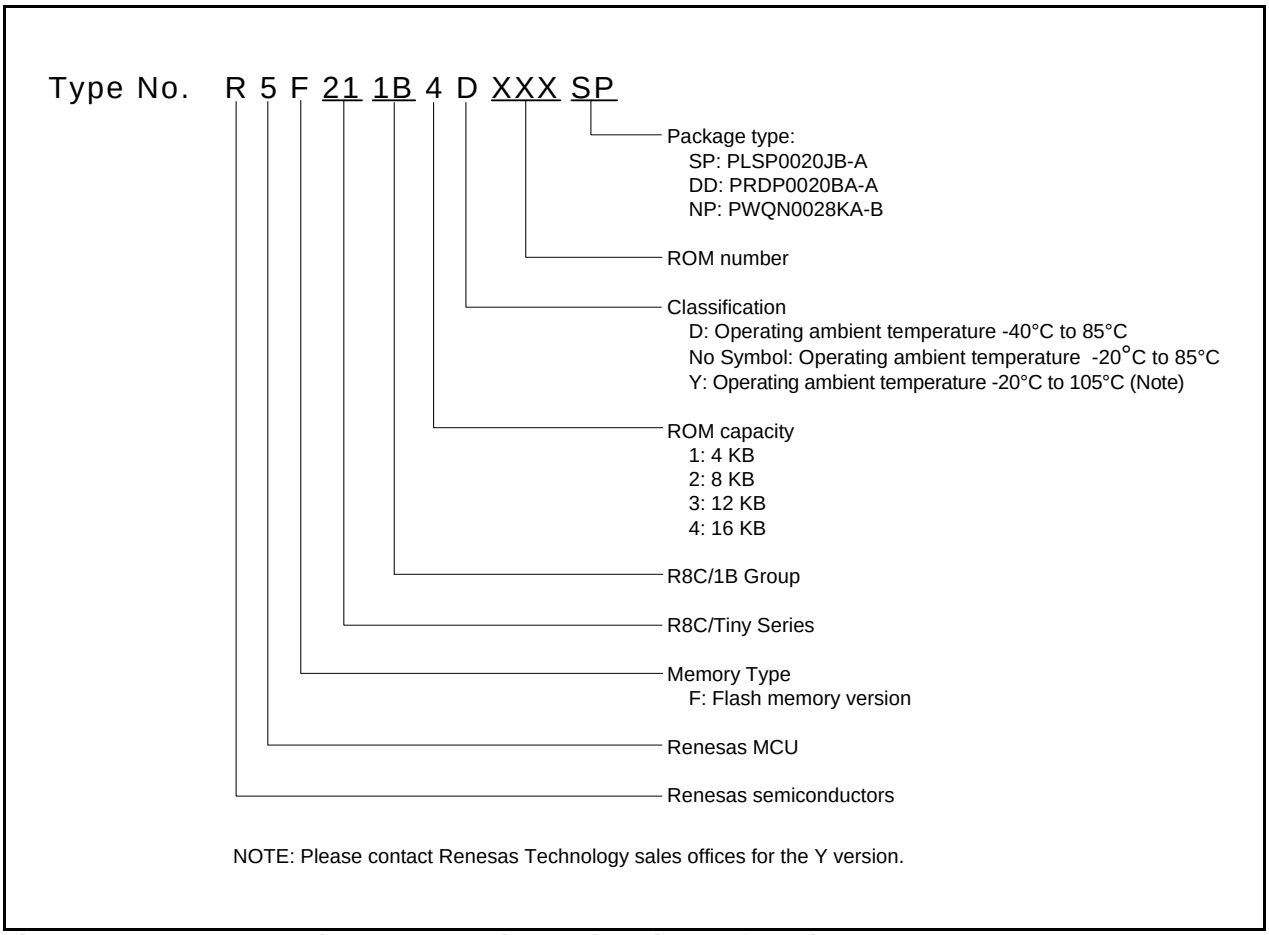


Figure 1.3 Type Number, Memory Size, and Package of R8C/1B Group

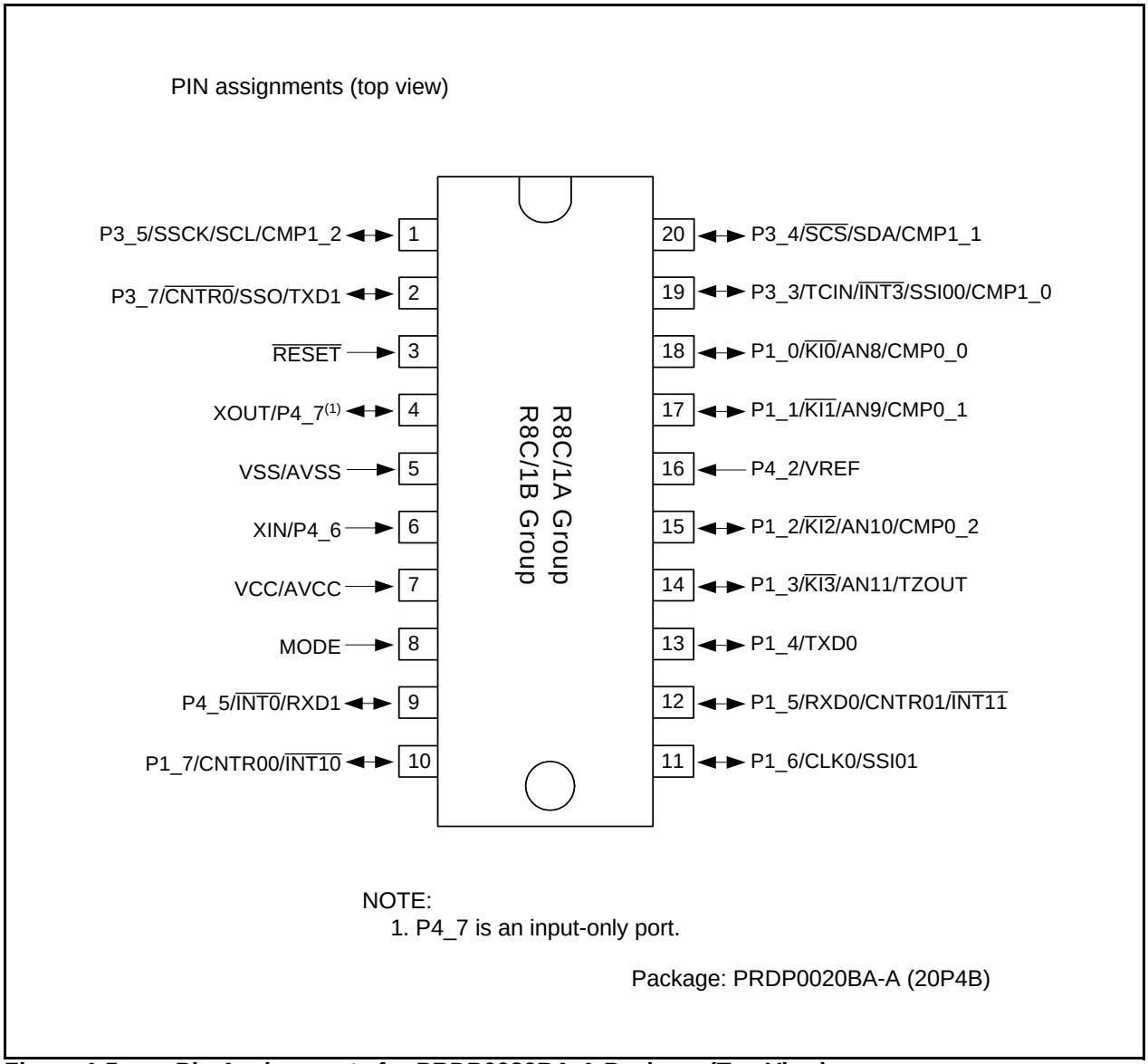


Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)

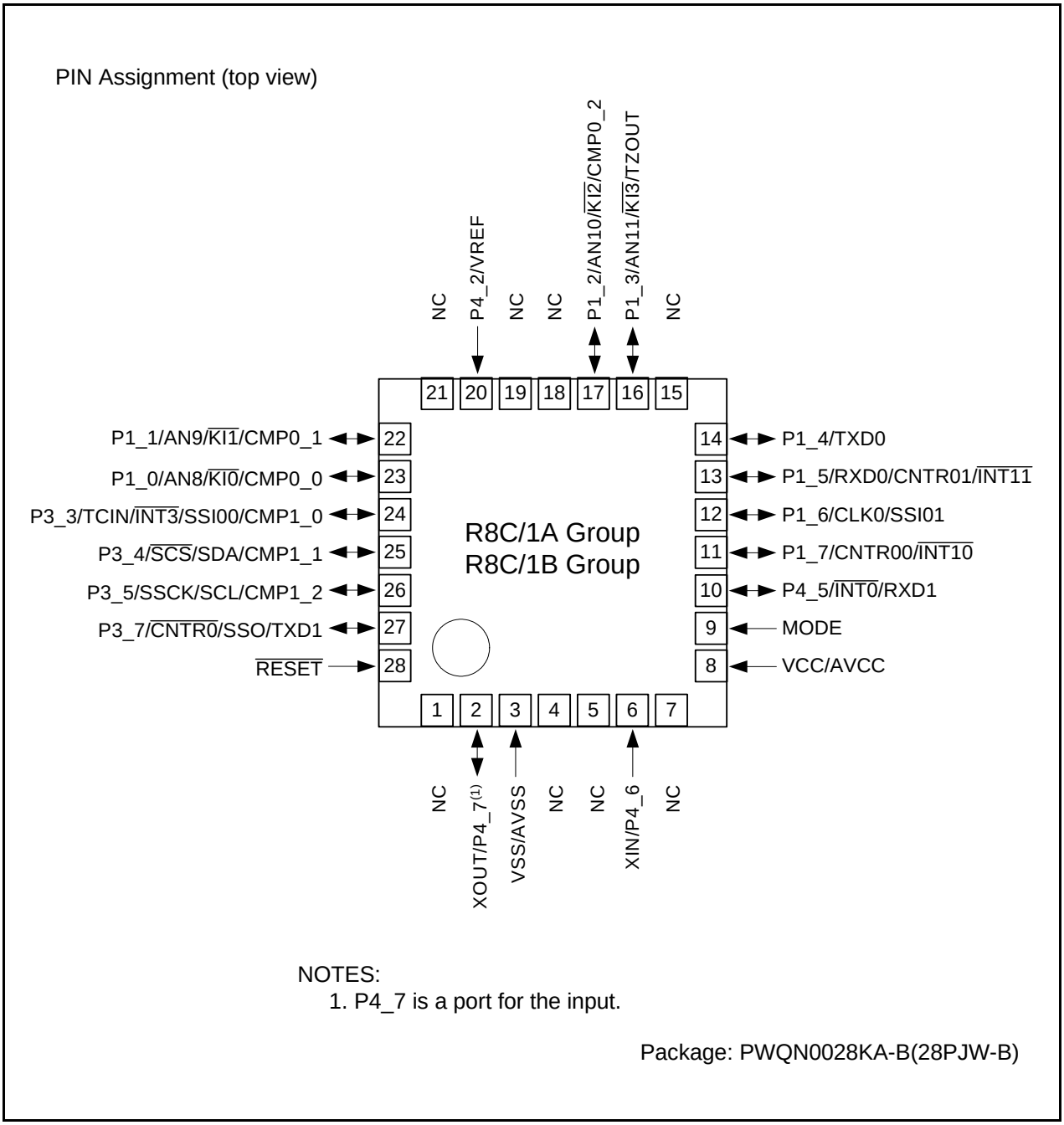


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A Packages and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B Package.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Power supply for the A/D converter Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main Clock Input	XIN	I	These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
Main Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	INT interrupt input pins
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	O	Timer C output pins
Serial Interface	CLK0	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
Clock synchronous serial I/O with chip select (SSU)	SSI00, SSI01	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
I^2C bus Interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter
A/D Converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O Port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_3 also function as LED drive ports.
Input Port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

5. Electrical Characteristics

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = -20°C to 105°C).

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	–	5.5	V
AV_{CC}	Analog supply voltage			–	V_{CC}	–	V
V_{SS}	Supply voltage			–	0	–	V
AV_{SS}	Analog supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	30	mA
			Drive capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average output “L” current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	15	mA
			Drive capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 Main clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 On-chip oscillator clock selected	HRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			HRA01 = 1 High-speed on-chip oscillator clock selected	–	8	–	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = V_{CC}	–	–	10	Bits
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = V_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	Vcc	V
V_{IA}	Analog input voltage(4)			0	–	AVcc	V
–	A/D operating clock frequency(2)	Without sample and hold		0.25	–	10	MHz
		With sample and hold		1	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is f1/2 or below.
4. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

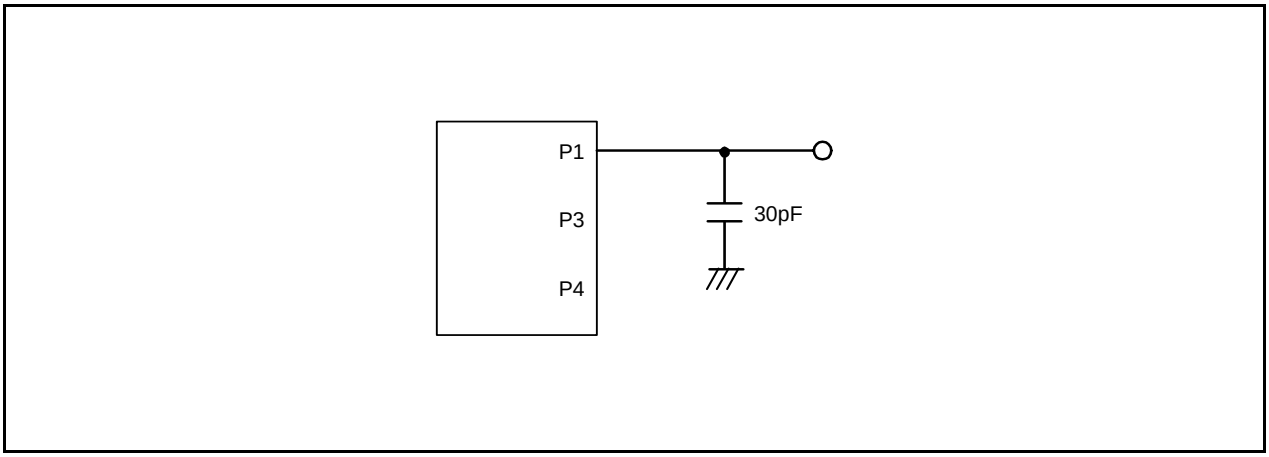


Figure 5.1 Port P1, P3, and P4 Measurement Circuit

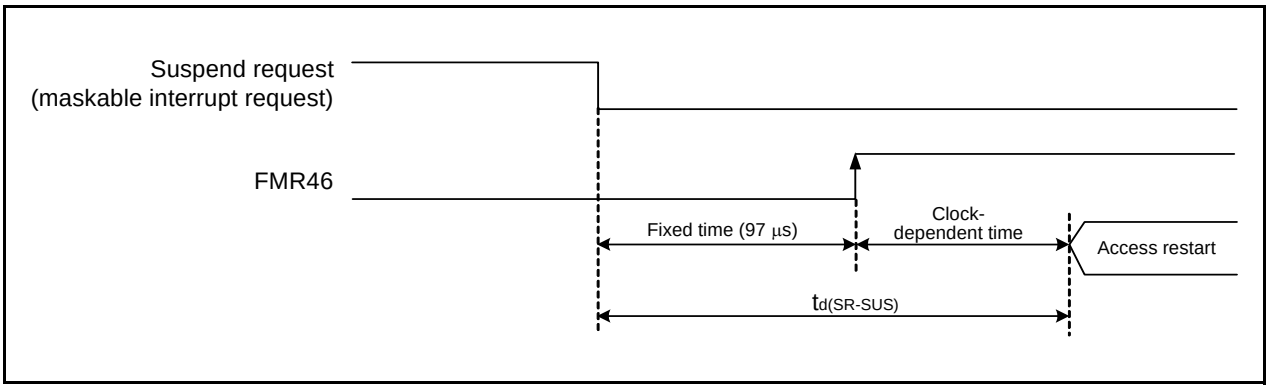


Figure 5.2 Transition Time to Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3)		2.70	2.85	3.00	V
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Ensure that $V_{det2} > V_{det1}$.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.00	3.30	3.60	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Ensure that $V_{det2} > V_{det1}$.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

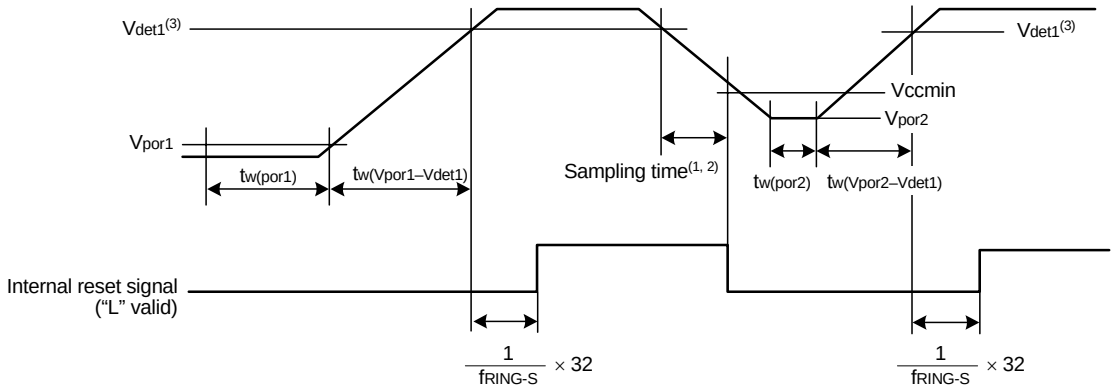
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted(1)	-20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2)	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with Vcc≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency when the reset is deasserted	V_{CC} = 5.0 V, T_{opr} = 25 °C	–	8	–	MHz
–	High-speed on-chip oscillator frequency temperature • supply voltage dependence(2)	0 to +60 °C/5 V ± 5 %(3)	7.76	–	8.24	MHz
		-20 to +85 °C/2.7 to 5.5 V(3)	7.68	–	8.32	MHz
		-40 to +85 °C/2.7 to 5.5 V(3)	7.44	–	8.32	MHz

NOTES:
1. The measurement condition is V_{CC} = 5.0 V and T_{opr} = 25 °C.
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

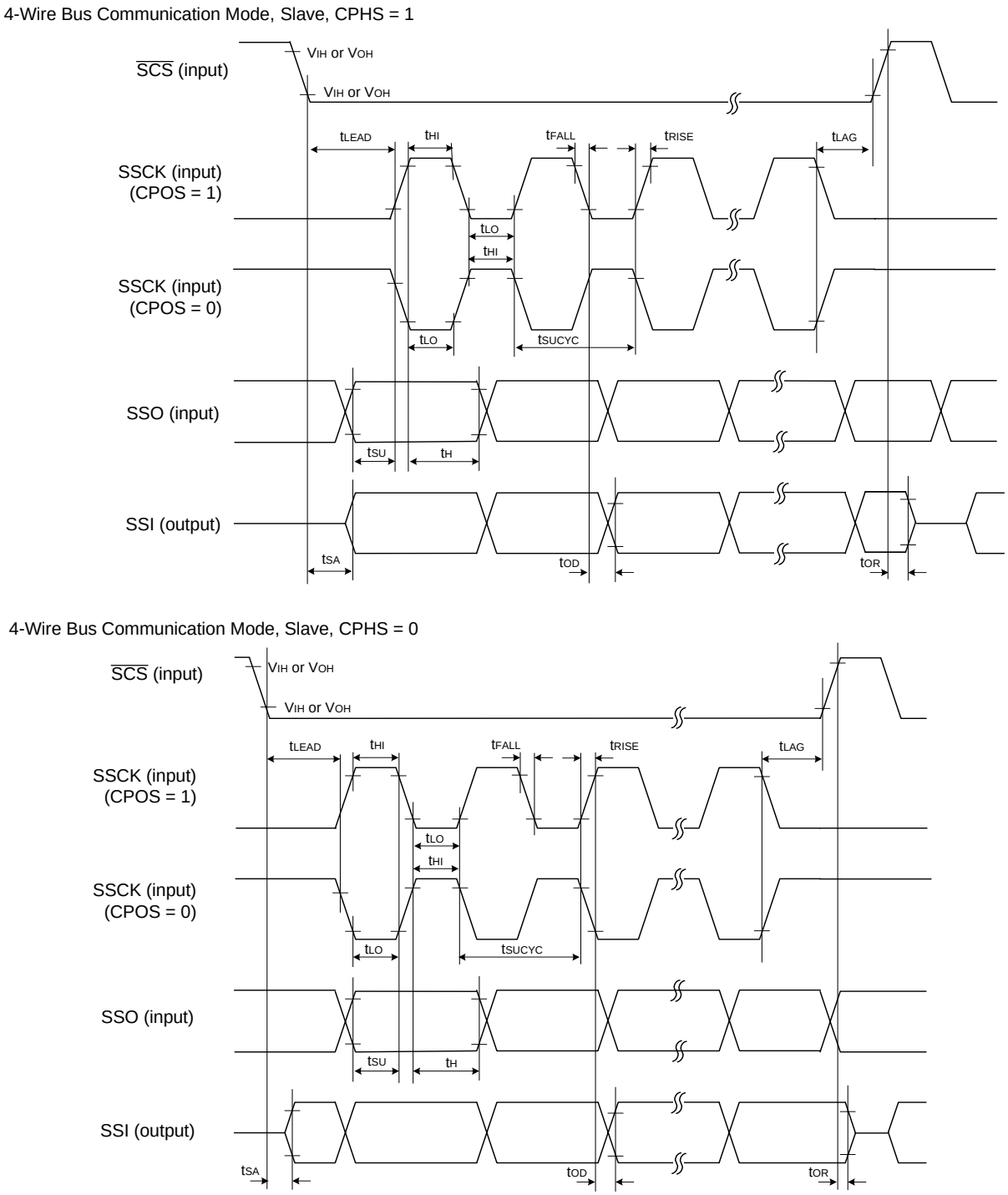
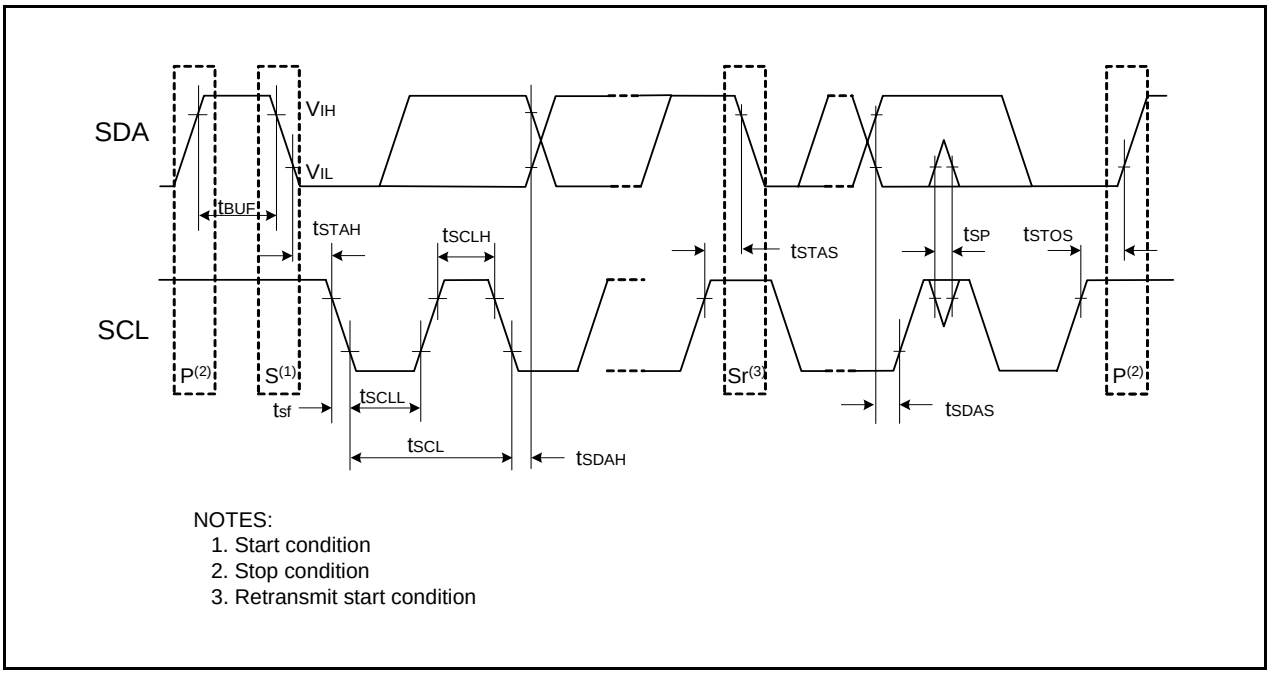


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.13 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}+600^{(2)}$	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}+300^{(2)}$	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}+300^{(2)}$	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}^{(2)}$	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}^{(2)}$	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}^{(2)}$	–	–	ns
t_{STOS}	Stop condition input setup time		$3t_{CYC}^{(2)}$	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC}+20^{(2)}$	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V and Ta = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.14 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except X_{OUT}	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 µA		V_{CC} – 0.3	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 15 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 200 µA	–	–	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0			0.2	–	1.0	V
		$\overline{RESET}$			0.2	–	2.2	V
I_{IH}	Input “H” current		VI = 5 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements
(Unless otherwise specified: Vcc = 5 V, Vss = 0 V at Ta = 25 °C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

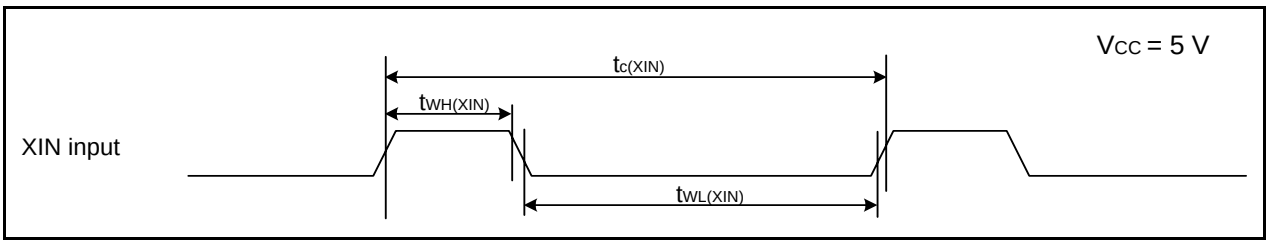


Figure 5.8 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	40	–	ns

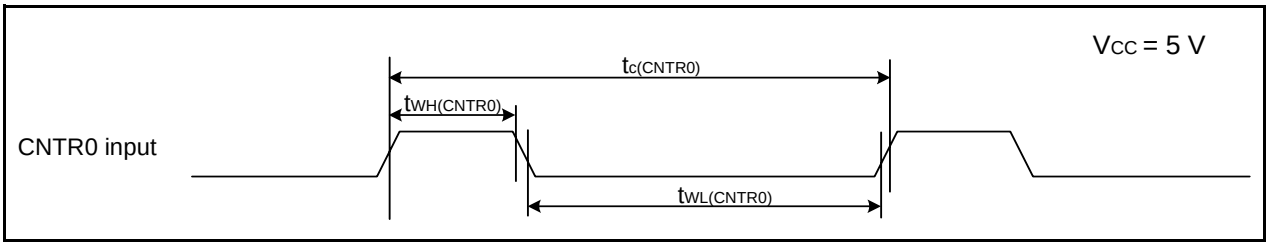


Figure 5.9 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 5 V

Table 5.18 TCIN Input, $\overline{\text{INT3}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400(1)	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	200(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	200(2)	–	ns

NOTES:
1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

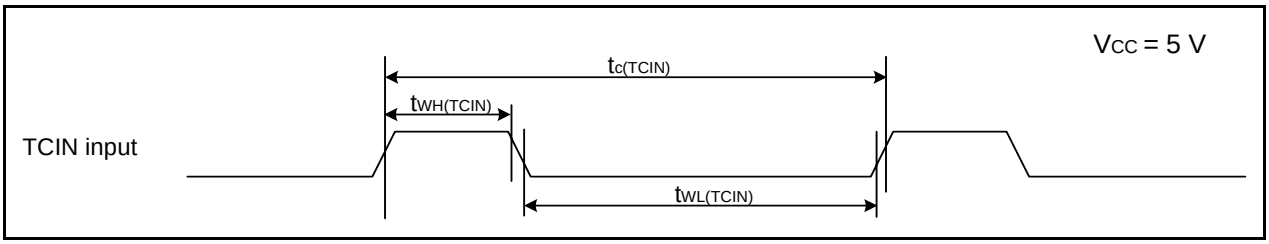


Figure 5.10 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 5 V

Table 5.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

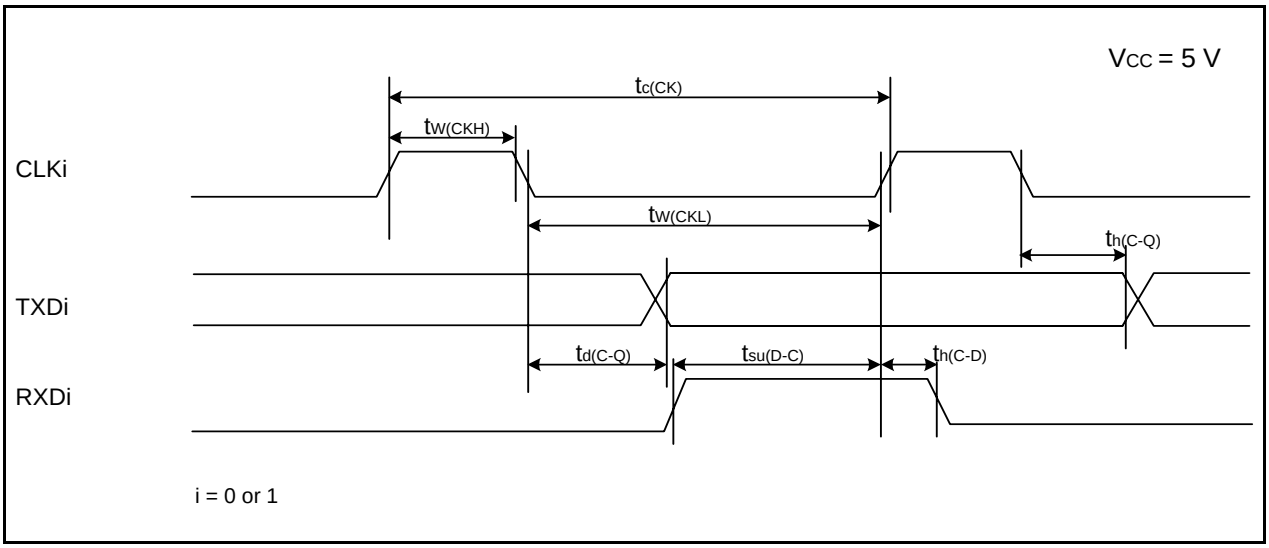


Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.20 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

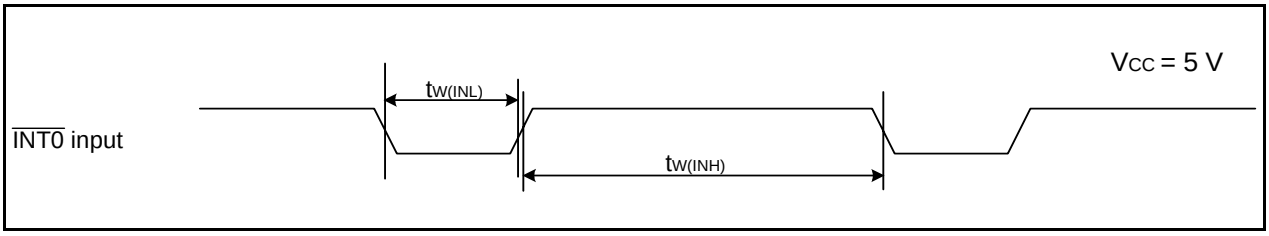
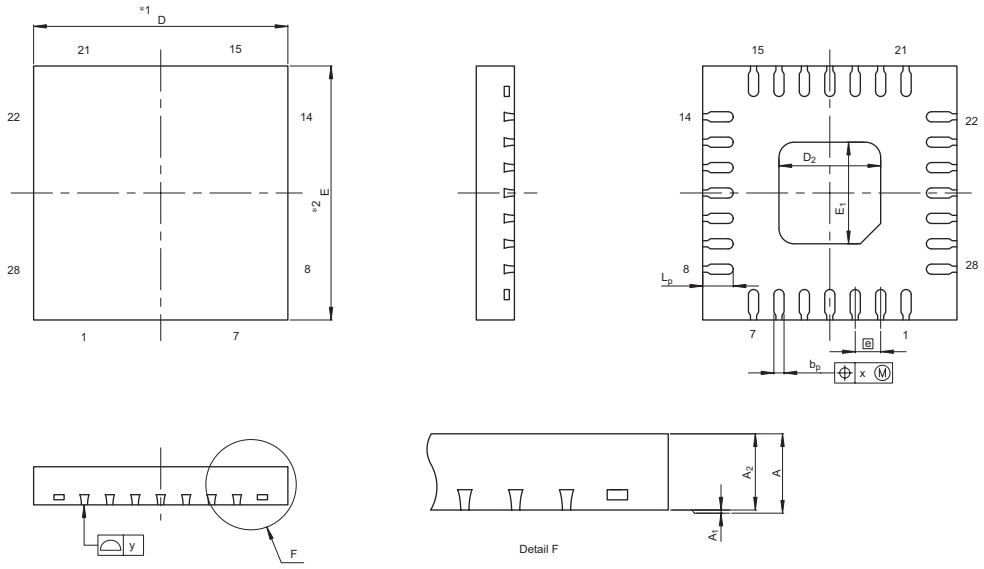


Figure 5.12 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 5 V

Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V_{SS}, A/D converter is stopped	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8	13	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7	12	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
		Medium-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.6	–	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	100	280	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	–	37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	–	35	70	µA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	–	0.7	3.0	µA

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN28-5x5-0.50	PWQN0028KA-B	28PJW-B	0.05g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.9	5.0	5.1
A_2	—	0.75	—
A	—	—	0.8
A_1	0	0	0.05
b_p	0.15	0.2	0.25
e	—	0.5	—
L_p	0.5	0.6	0.7
x	—	—	0.05
y	—	—	0.05
D_2	—	2.0	—
E_1	—	2.0	—