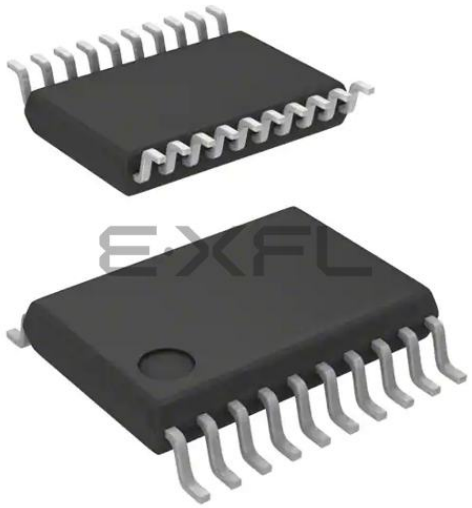
Renesas Electronics America Inc - R5F211B2SP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211b2sp-u0

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1. Overview

These MCUs are fabricated using the high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/1B Group has on-chip data flash ROM (1 KB × 2 blocks).
The difference between the R8C/1A Group and R8C/1B Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), portable equipment, general industrial equipment, audio equipment, etc.

Table 1.2 Functions and Specifications for R8C/1B Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	See **Table 1.4 Product Information for R8C/1B Group**
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Clock synchronous serial interface	1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select (SSU)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 11 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power on reset circuit	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, A/D converter stopped) Typ. 5 mA (VCC = 3.0 V, f(XIN) = 10 MHz, A/D converter stopped) Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version) -20 to 105°C (Y version) (2)
Package		20-pin molded-plastic LSSOP 20-pin molded-plastic SDIP 28-pin molded-plastic HWQFN

NOTE:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

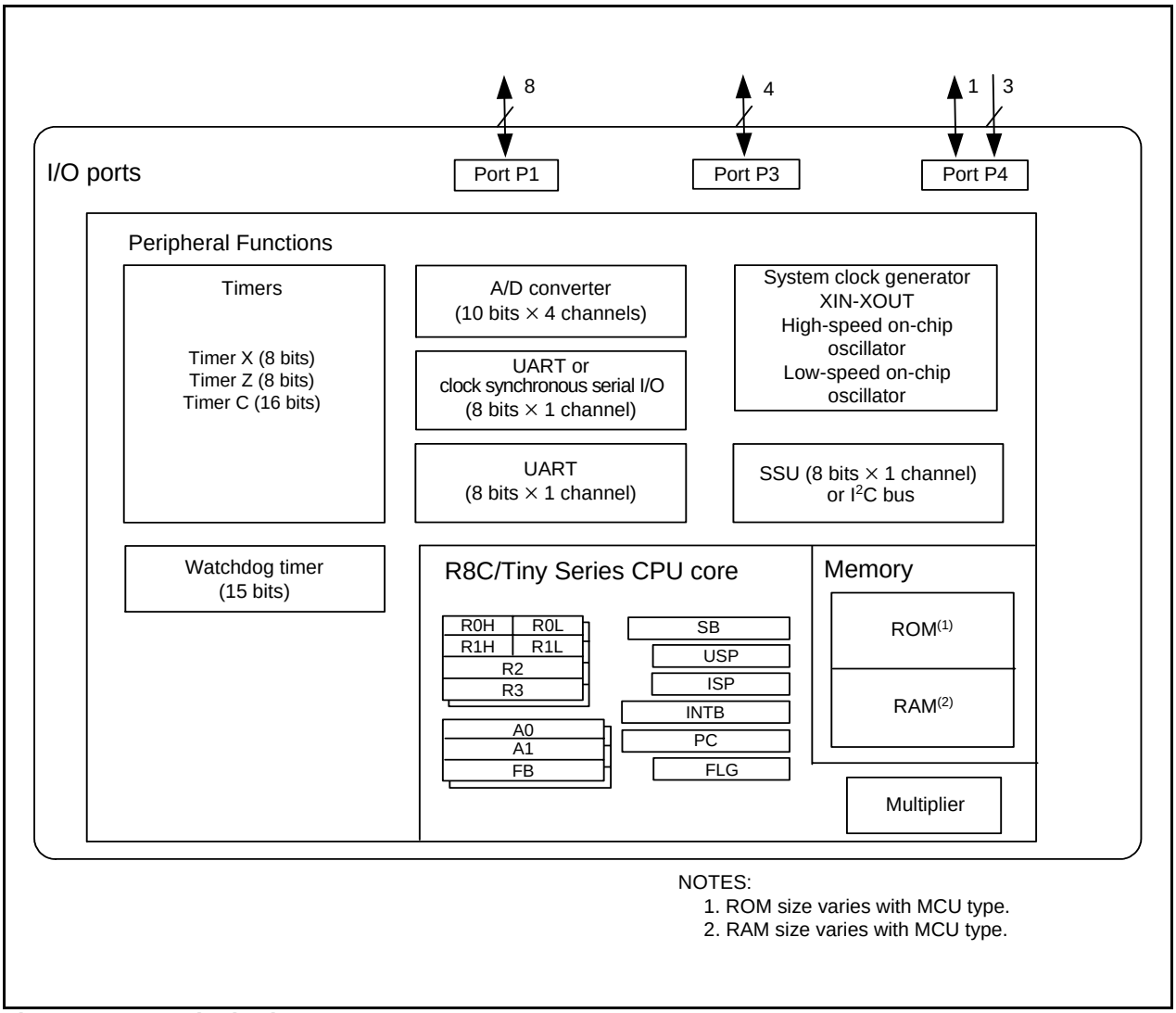


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/1A Group and Table 1.4 lists Product Information for R8C/1B Group.

Table 1.3 Product Information for R8C/1A Group Current of October 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F211A1SP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F211A2SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DD	4 Kbytes	384 bytes	PRDP0020BA-A	
R5F211A2DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2NP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	
R5F211A1XXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	Factory programming product (1)
R5F211A2XXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3XXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4XXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DXXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DXXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1XXXDD	4 Kbytes	384 bytes	PRDP0020BA-A	Factory programming product (1)
R5F211A2XXXDD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3XXXDD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4XXXDD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2XXXNP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3XXXNP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4XXXNP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

NOTE:
1. The user ROM is programmed before shipment.

Table 1.4 Product Information for R8C/1B Group Current of October 2006

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F211B1SP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	
R5F211B2SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F211B2DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	
R5F211B2DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3DD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	
R5F211B1XXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	Factory programming product (1)
R5F211B2XXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3XXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4XXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DXXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F211B2DXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DXXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1XXXDD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Factory programming product (1)
R5F211B2XXXDD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3XXXDD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4XXXDD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2XXXNP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3XXXNP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4XXXNP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

NOTE:
1. The user ROM is programmed before shipment.

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).

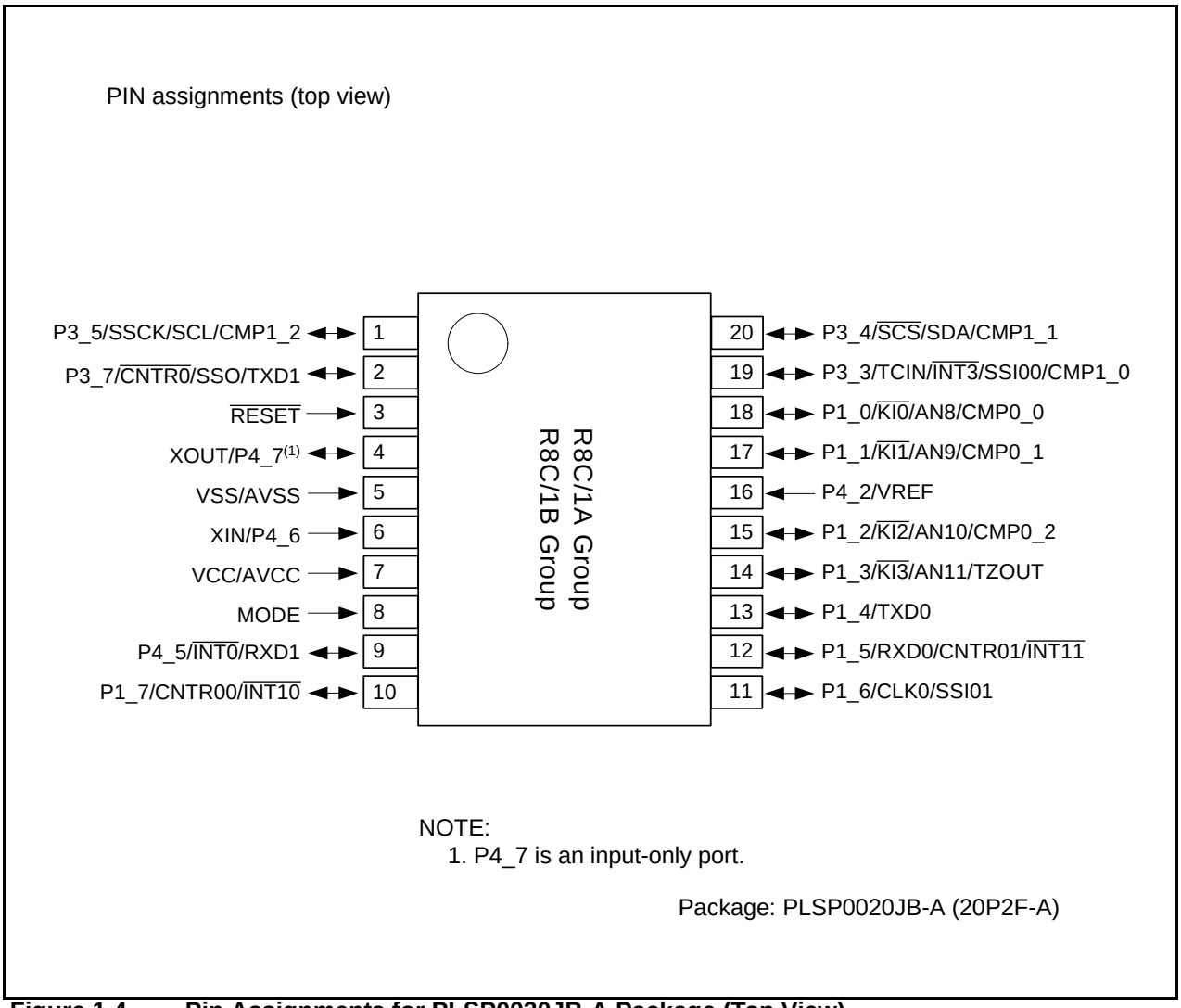


Figure 1.4 Pin Assignments for PLSP0020JB-A Package (Top View)

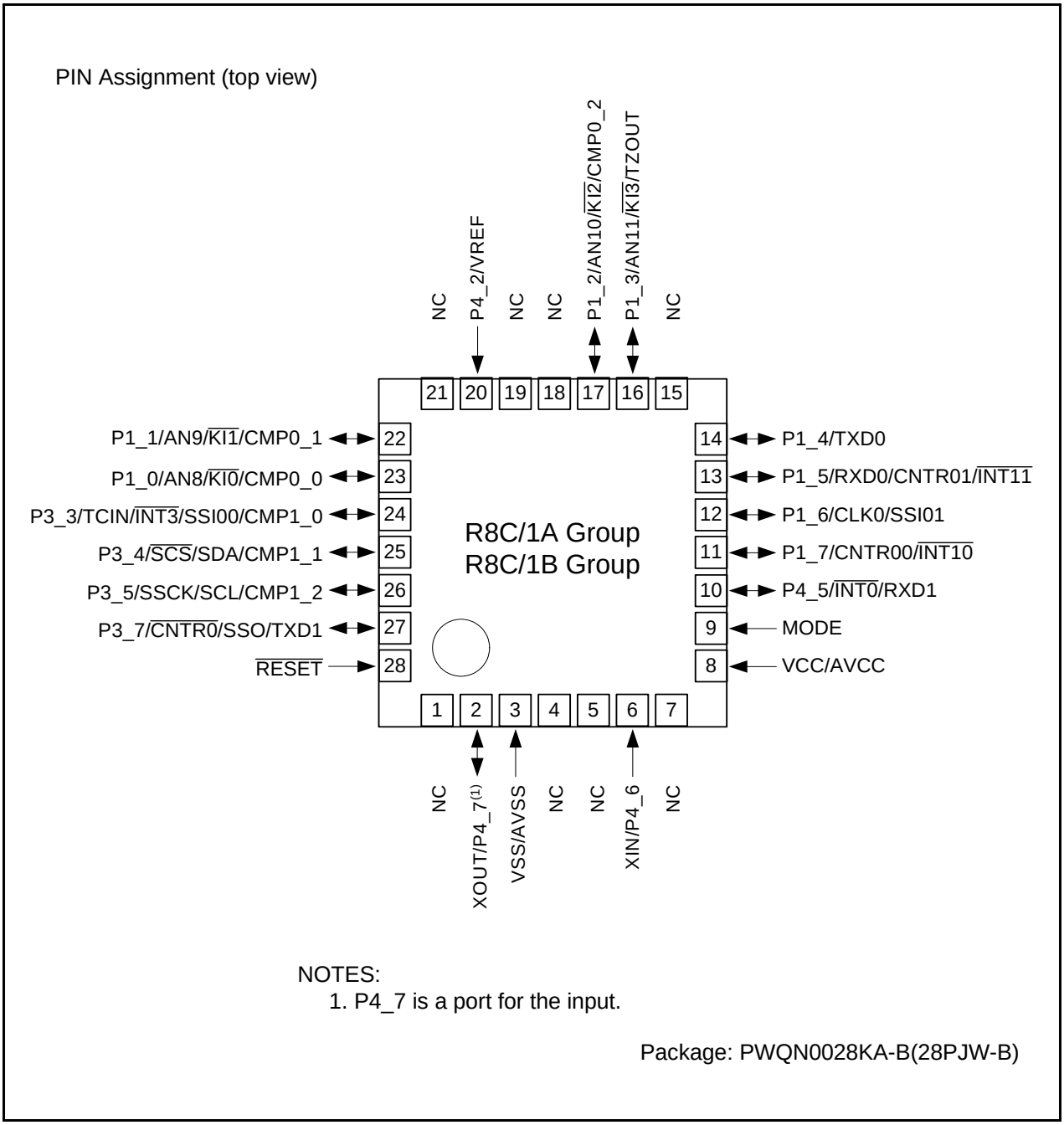
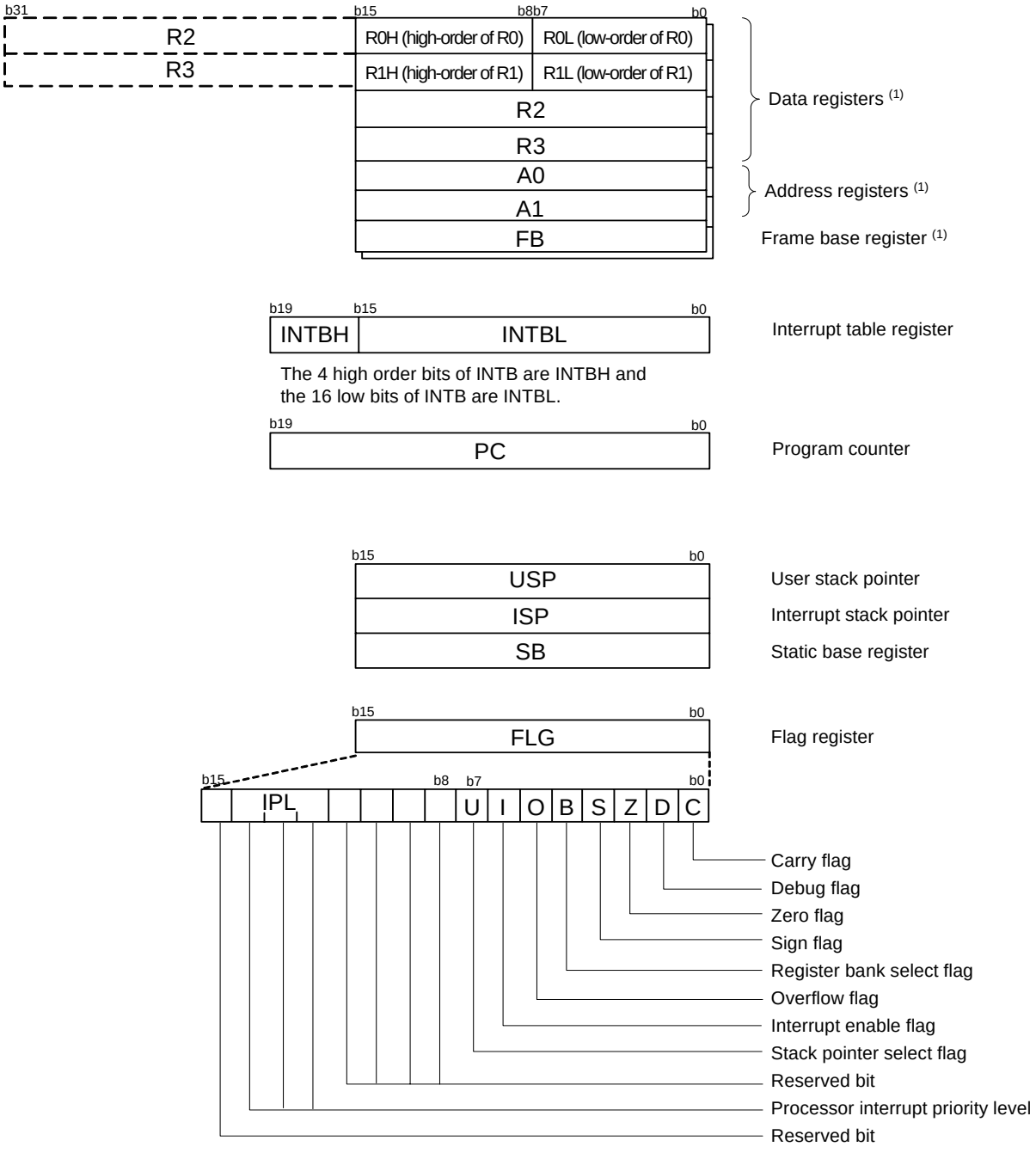


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer and arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	$\overline{\text{INT0}}$ Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register [2]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register [5]	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = V_{CC}	–	–	10	Bits
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 3.3 V(3)	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = V_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = V_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	Vcc	V
V_{IA}	Analog input voltage(4)			0	–	AVcc	V
–	A/D operating clock frequency(2)	Without sample and hold		0.25	–	10	MHz
		With sample and hold		1	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divide f1 and ensure the A/D operating clock frequency (ϕ_{AD}) is f1/2 or below.
4. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

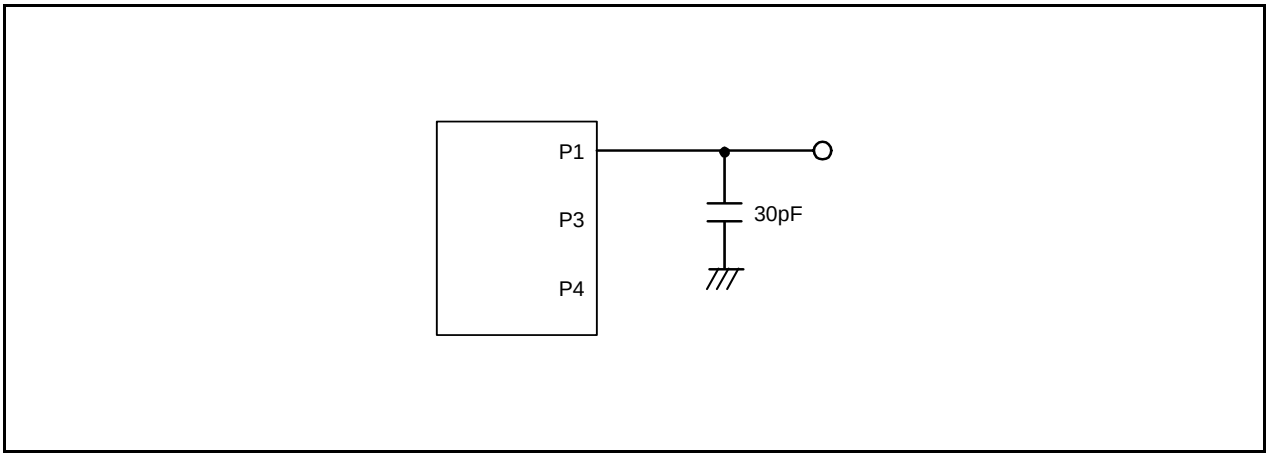


Figure 5.1 Port P1, P3, and P4 Measurement Circuit

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

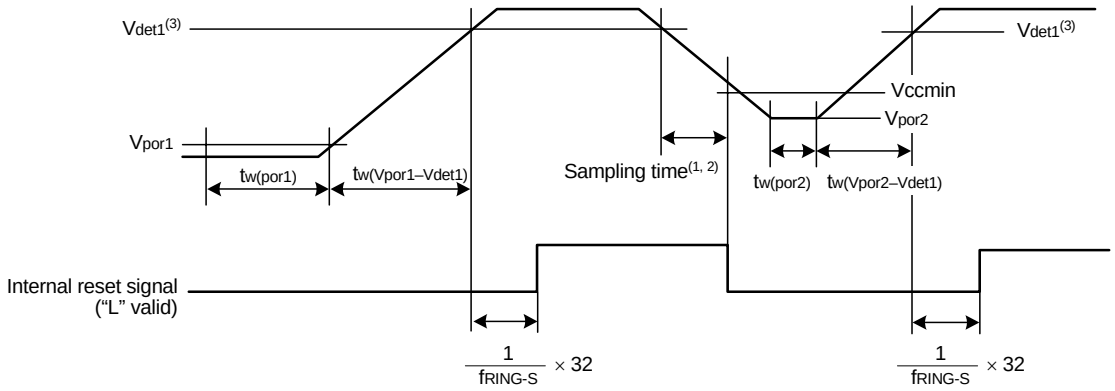
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted(1)	-20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2)	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with Vcc≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

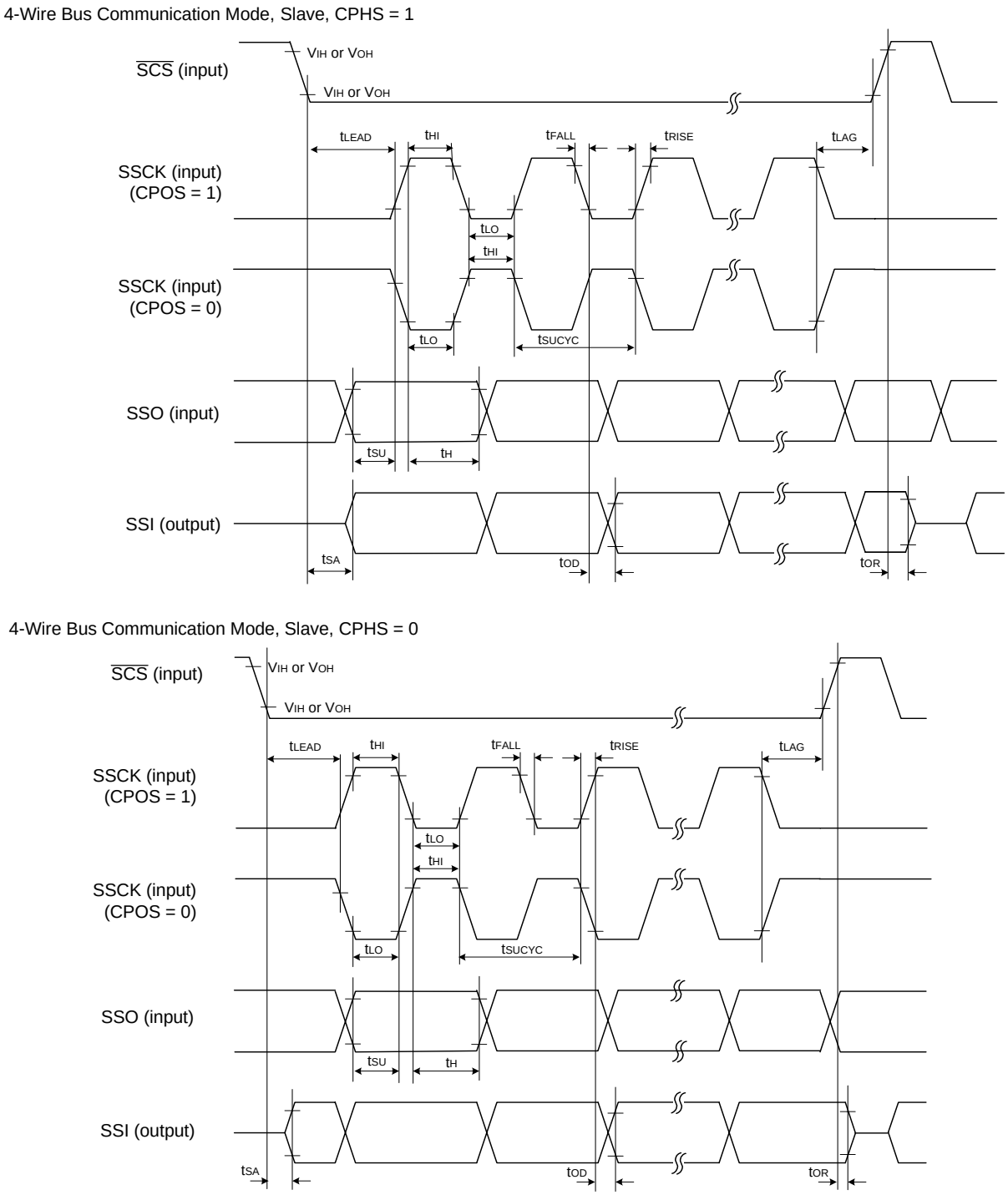


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

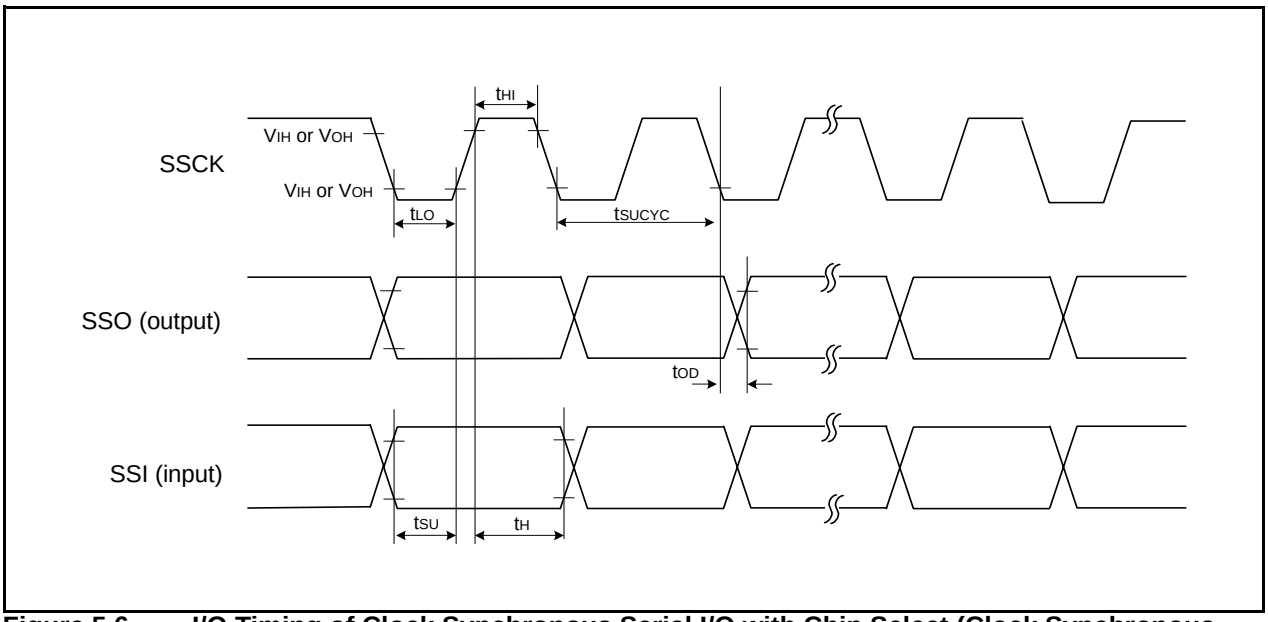


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

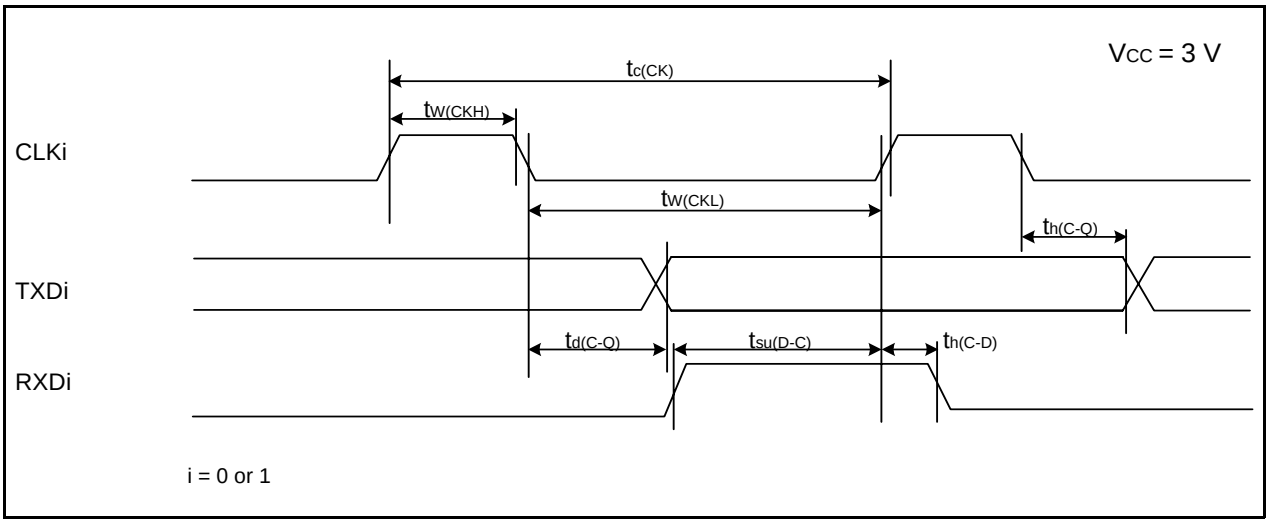


Figure 5.16 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater

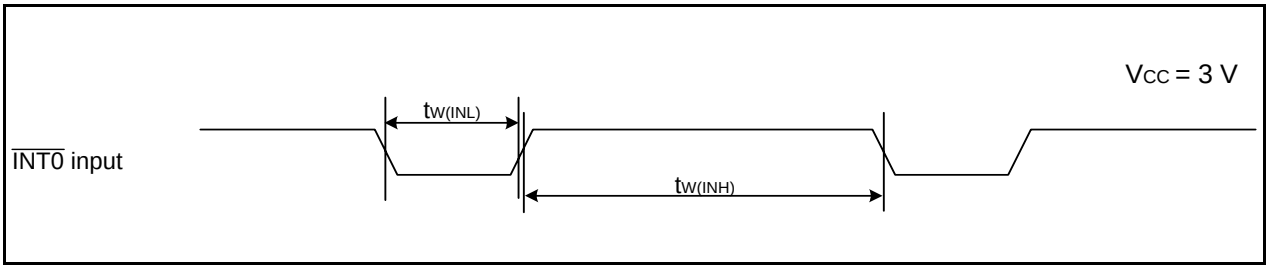
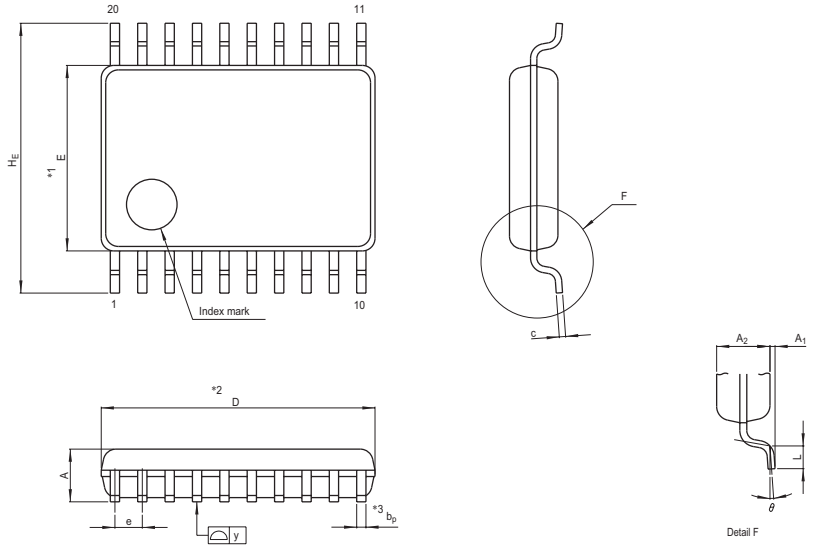


Figure 5.17 External Interrupt $\overline{INT0}$ Input Timing Diagram when VCC = 3 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

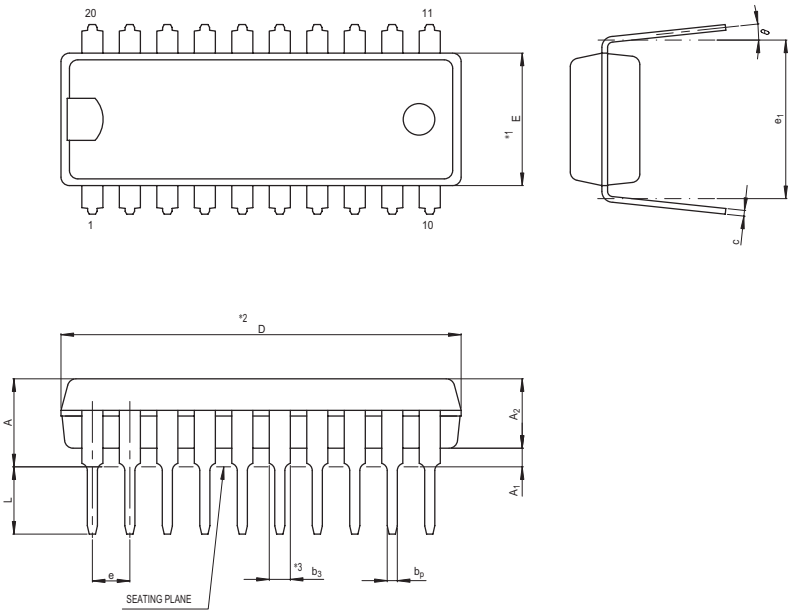
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

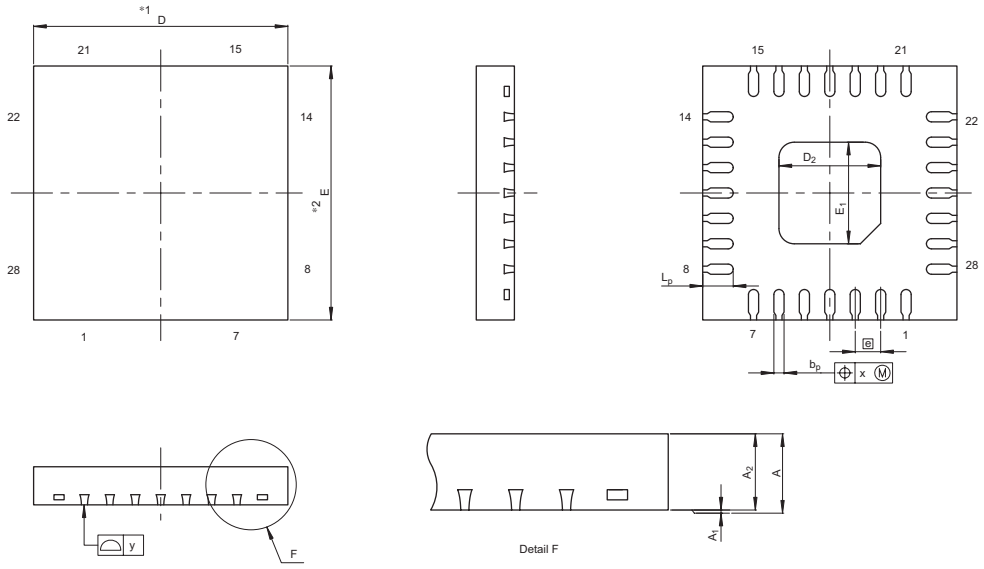
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN28-5x5-0.50	PWQN0028KA-B	28PJW-B	0.05g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.9	5.0	5.1
A_2	—	0.75	—
A	—	—	0.8
A_1	0	0	0.05
b_p	0.15	0.2	0.25
e	—	0.5	—
L_p	0.5	0.6	0.7
x	—	—	0.05
y	—	—	0.05
D_2	—	2.0	—
E_1	—	2.0	—

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