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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211b4dsp-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211b4dsp-u0</a>

## 1. Overview

These MCUs are fabricated using the high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/1B Group has on-chip data flash ROM (1 KB × 2 blocks).

The difference between the R8C/1A Group and R8C/1B Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

### 1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), portable equipment, general industrial equipment, audio equipment, etc.

**Table 1.2 Functions and Specifications for R8C/1B Group**

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ( $f(XIN) = 20$ MHz, $VCC = 3.0$ to $5.5$ V) 100 ns ( $f(XIN) = 10$ MHz, $VCC = 2.7$ to $5.5$ V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	See <b>Table 1.4 Product Information for R8C/1B Group</b>
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits $\times$ 1 channel, timer Z: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits $\times$ 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Clock synchronous serial interface	1 channel I <sup>2</sup> C bus Interface <sup>(1)</sup> Clock synchronous serial I/O with chip select (SSU)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 11 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power on reset circuit	On-chip
Electric Characteristics	Supply voltage	$VCC = 3.0$ to $5.5$ V ( $f(XIN) = 20$ MHz) $VCC = 2.7$ to $5.5$ V ( $f(XIN) = 10$ MHz)
	Current consumption	Typ. 9 mA ( $VCC = 5.0$ V, $f(XIN) = 20$ MHz, A/D converter stopped) Typ. 5 mA ( $VCC = 3.0$ V, $f(XIN) = 10$ MHz, A/D converter stopped) Typ. 35 $\mu$ A ( $VCC = 3.0$ V, wait mode, peripheral clock off) Typ. 0.7 $\mu$ A ( $VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to $5.5$ V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C
		-40 to 85°C (D version)
		-20 to 105°C (Y version) <sup>(2)</sup>
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

NOTE:

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Please contact Renesas Technology sales offices for the Y version.

## 1.4 Product Information

Table 1.3 lists Product Information for R8C/1A Group and Table 1.4 lists Product Information for R8C/1B Group.

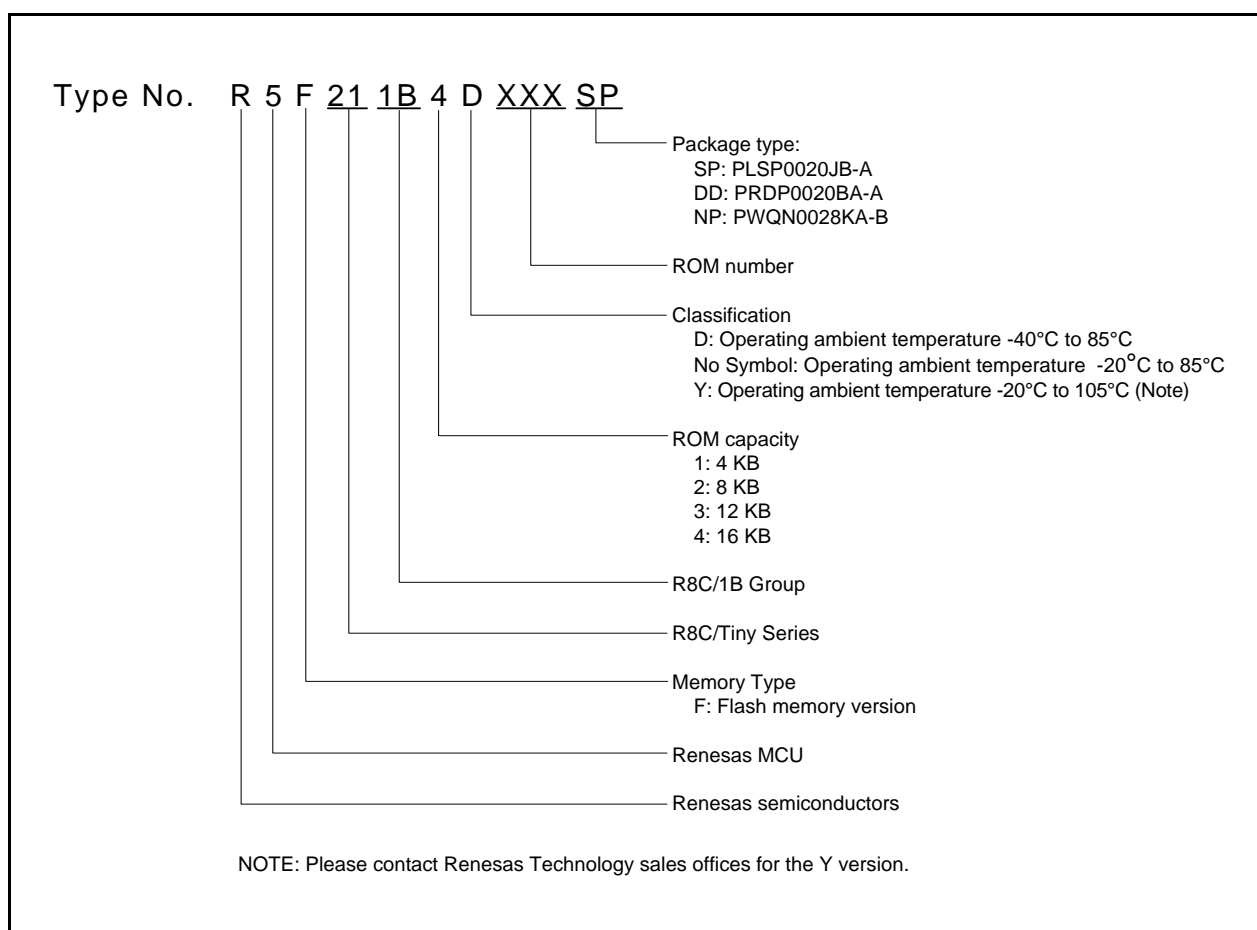
**Table 1.3 Product Information for R8C/1A Group**

**Current of October 2006**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F211A1SP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F211A2SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DD	4 Kbytes	384 bytes	PRDP0020BA-A	
R5F211A2DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2NP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	
R5F211A1XXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	Factory programming product <sup>(1)</sup>
R5F211A2XXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3XXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4XXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DXXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DXXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1XXXDD	4 Kbytes	384 bytes	PRDP0020BA-A	Factory programming product <sup>(1)</sup>
R5F211A2XXXDD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3XXXDD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4XXXDD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2XXXNP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3XXXNP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4XXXNP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

NOTE:

1. The user ROM is programmed before shipment.



**Figure 1.3** Type Number, Memory Size, and Package of R8C/1B Group

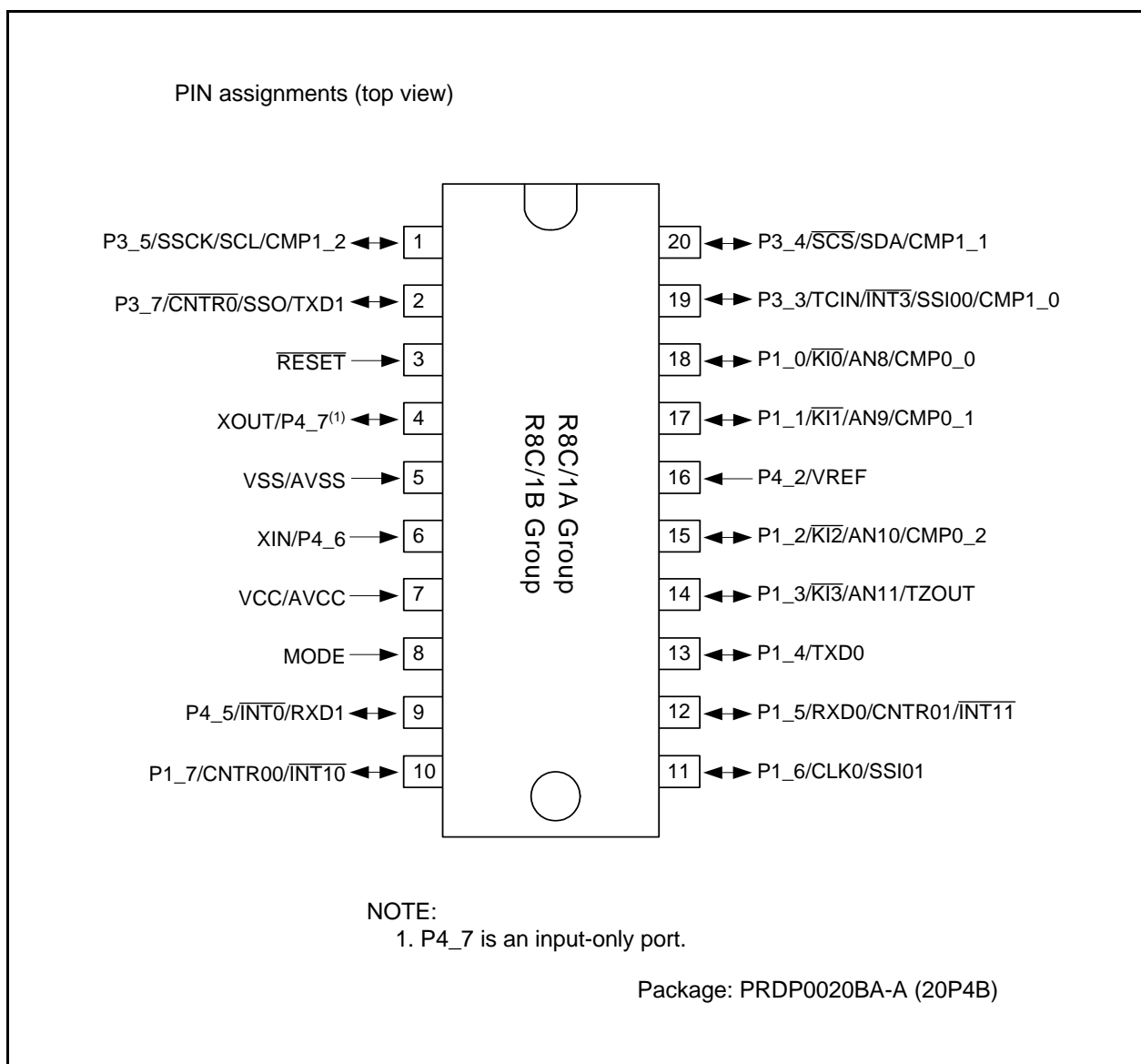


Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)

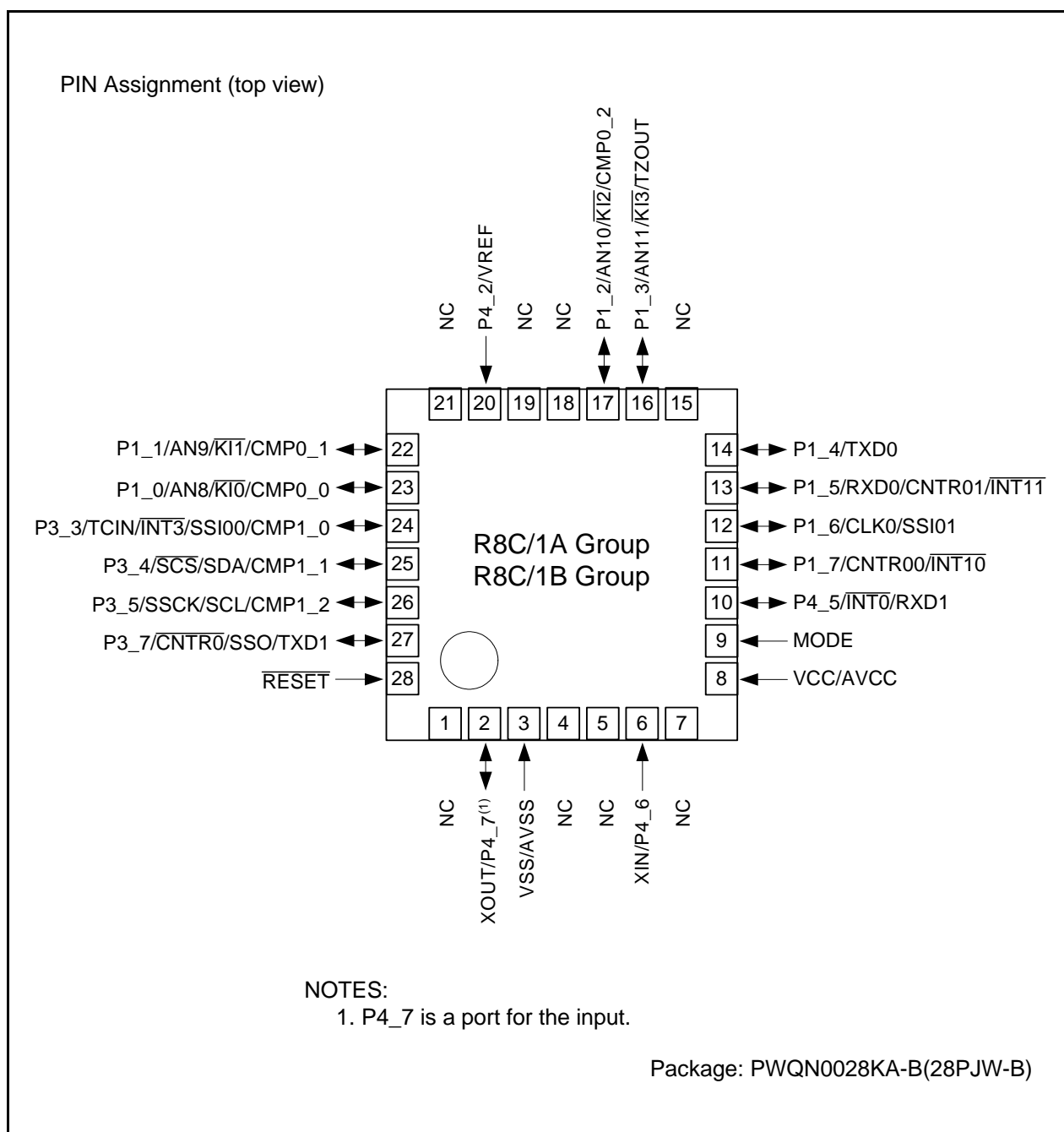


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

## 1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A Packages and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B Package.

**Table 1.5 Pin Functions**

Type	Symbol	I/O Type	Description
Power Supply Input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Power supply for the A/D converter Connect a capacitor between AVCC and AVSS.
Reset Input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main Clock Input	XIN	I	These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
Main Clock Output	XOUT	O	
INT Interrupt	INT0, INT1, INT3	I	INT interrupt input pins
Key Input Interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	O	Timer X output pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	O	Timer C output pins
Serial Interface	CLK0	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
Clock synchronous serial I/O with chip select (SSU)	SSI00, SSI01	I/O	Data I/O pin.
	SCS	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
I <sup>2</sup> C bus Interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter
A/D Converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O Port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_3 also function as LED drive ports.
Input Port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input      O: Output      I/O: Input and output



**Table 1.6 Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A Packages**

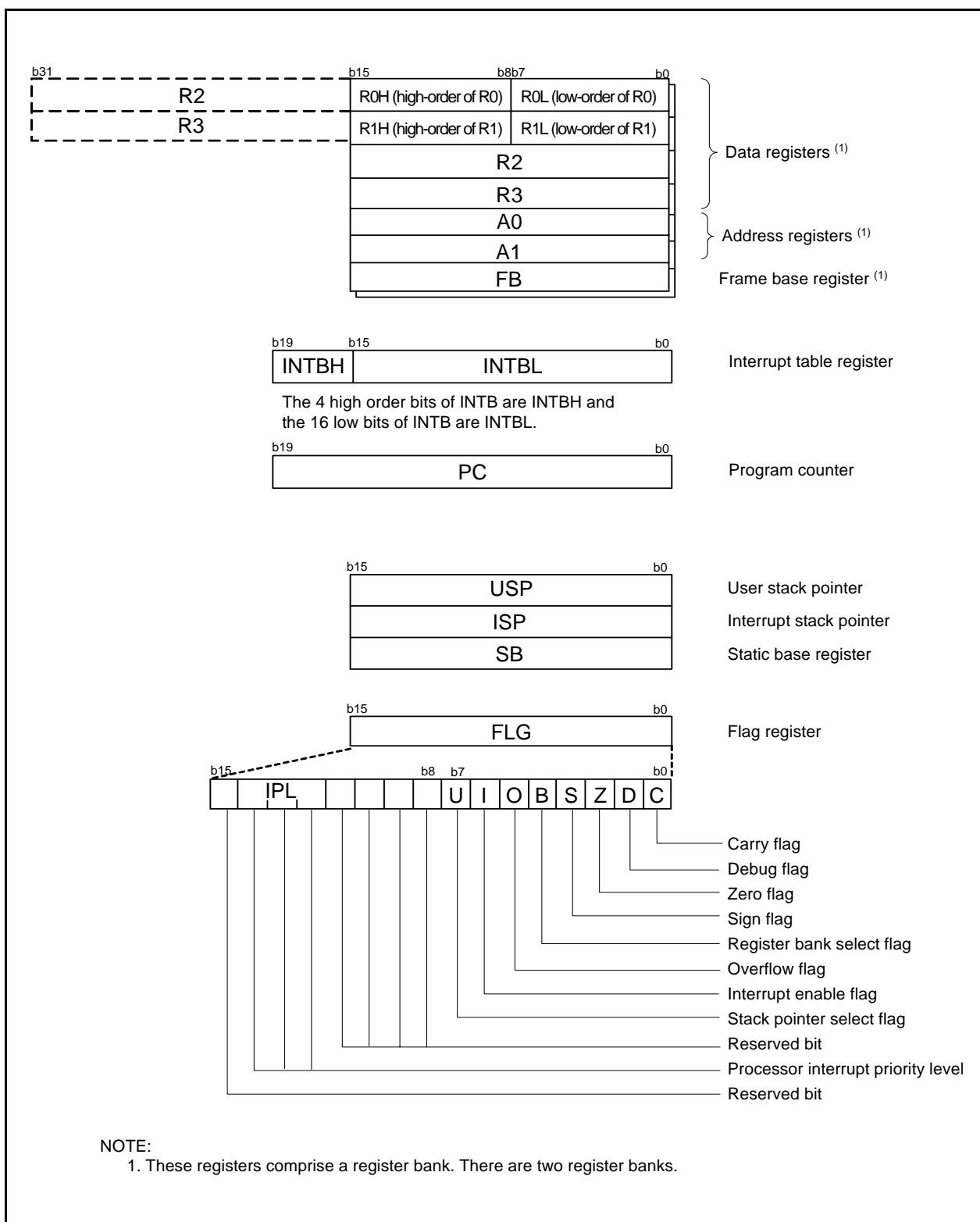
Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I <sup>2</sup> C bus Interface	A/D Converter
1		P3_5		CMP1_2		SSCK	SCL	
2		P3_7		CNTR0	TXD1	SSO		
3	RESET							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	INT0		RXD1			
10		P1_7	INT10	CNTR00				
11		P1_6			CLK0	SSI01		
12		P1_5	INT11	CNTR01	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TZOUT				AN11
15		P1_2	KI2	CMP0_2				AN10
16	VREF	P4_2						
17		P1_1	KI1	CMP0_1				AN9
18		P1_0	KI0	CMP0_0				AN8
19		P3_3	INT3	TCIN/ CMP1_0		SSI00		
20		P3_4		CMP1_1		SCS	SDA	

**Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B Package**

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I <sup>2</sup> C bus Interface	A/D Converter
1	NC							
2	XOUT	P4_7						
3	VSS/AVSS							
4	NC							
5	NC							
6	XIN	P4_6						
7	NC							
8	VCC/AVCC							
9	MODE							
10		P4_5	$\overline{\text{INT0}}$		RXD1			
11		P1_7	$\overline{\text{INT10}}$	CNTR00				
12		P1_6			CLK0	SSI01		
13		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0			
14		P1_4			TXD0			
15	NC							
16		P1_3	$\overline{\text{KI3}}$	TZOUT				AN11
17		P1_2	$\overline{\text{KI2}}$	CMP0_2				AN10
18	NC							
19	NC							
20	VREF	P4_2						
21	NC							
22		P1_1	$\overline{\text{KI1}}$	CMP0_1				AN9
23		P1_0	$\overline{\text{KI0}}$	CMP0_0				AN8
24		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		SSI00		
25		P3_4		CMP1_1		$\overline{\text{SCS}}$	SDA	
26		P3_5		CMP1_2		SSCK	SCL	
27		P3_7		$\overline{\text{CNTR0}}$	TXD1	SSO		
28	$\overline{\text{RESET}}$							

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



**Figure 2.1 CPU Register**

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer and arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.

**Table 4.2 SFR Information (2)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register <sup>(2)</sup>	SSUAIC/IIC2AIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XXXXX000b
005Ah	INT3 Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

**NOTES:**

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

## 5. Electrical Characteristics

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version ( $T_{opr} = -20^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ ).

**Table 5.1 Absolute Maximum Ratings**

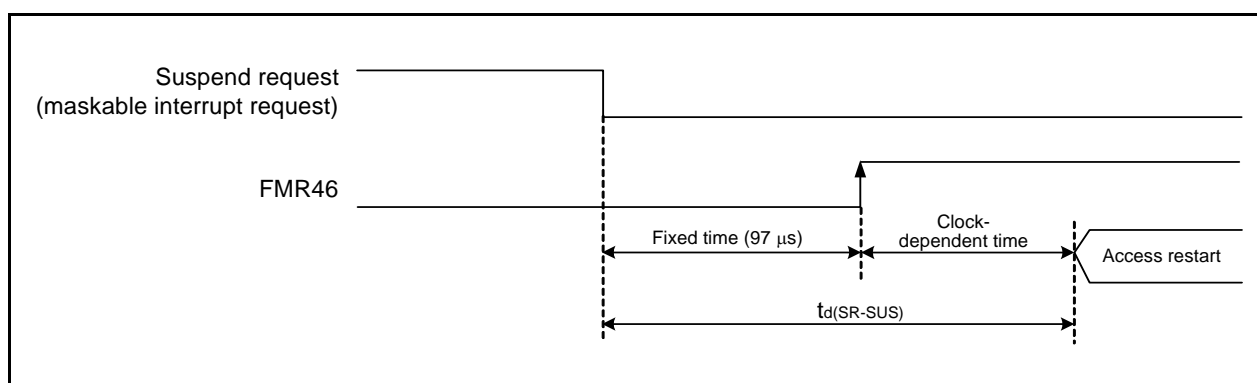
Symbol	Parameter	Condition	Rated Value	Unit
V <sub>CC</sub>	Supply voltage	V <sub>CC</sub> = AV <sub>CC</sub>	-0.3 to 6.5	V
AV <sub>CC</sub>	Analog supply voltage	V <sub>CC</sub> = AV <sub>CC</sub>	-0.3 to 6.5	V
V <sub>I</sub>	Input voltage		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>opr</sub> = 25°C	300	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage			2.7	–	5.5	V
AV <sub>CC</sub>	Analog supply voltage			–	V <sub>CC</sub>	–	V
V <sub>SS</sub>	Supply voltage			–	0	–	V
AV <sub>SS</sub>	Analog supply voltage			–	0	–	V
V <sub>IH</sub>	Input “H” voltage			0.8V <sub>CC</sub>	–	V <sub>CC</sub>	V
V <sub>IL</sub>	Input “L” voltage			0	–	0.2V <sub>CC</sub>	V
I <sub>OH(sum)</sub>	Peak sum output “H” current	Sum of all pins I <sub>OH</sub> (peak)		–	–	-60	mA
I <sub>OH(peak)</sub>	Peak output “H” current			–	–	-10	mA
I <sub>OH(ave)</sub>	Average output “H” current			–	–	-5	mA
I <sub>OL(sum)</sub>	Peak sum output “L” currents	Sum of all pins I <sub>OL</sub> (peak)		–	–	60	mA
I <sub>OL(peak)</sub>	Peak output “L” currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	30	mA
			Drive capacity LOW	–	–	10	mA
I <sub>OL(ave)</sub>	Average output “L” current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	15	mA
			Drive capacity LOW	–	–	5	mA
f(XIN)	Main clock input oscillation frequency		3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0	3.0 V ≤ V <sub>CC</sub> ≤ 5.5 V	0	–	20	MHz
		Main clock selected	2.7 V ≤ V <sub>CC</sub> < 3.0 V	0	–	10	MHz
		OCD2 = 1	HRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
		On-chip oscillator clock selected	HRA01 = 1 High-speed on-chip oscillator clock selected	–	8	–	MHz

**NOTES:**

1. V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.

**Figure 5.2 Transition Time to Suspend****Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det1</sub>	Voltage detection level <sup>(3)</sup>		2.70	2.85	3.00	V
—	Voltage detection circuit self power consumption	VCA26 = 1, V <sub>CC</sub> = 5.0 V	—	600	—	nA
t <sub>d</sub> (E-A)	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		—	—	100	μs
V <sub>ccmin</sub>	MCU operating voltage minimum value		2.7	—	—	V

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = 2.7 V to 5.5 V and T<sub>opr</sub> = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Ensure that V<sub>det2</sub> > V<sub>det1</sub>.

**Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V <sub>det2</sub>	Voltage detection level <sup>(4)</sup>		3.00	3.30	3.60	V
—	Voltage monitor 2 interrupt request generation time <sup>(2)</sup>		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V <sub>CC</sub> = 5.0 V	—	600	—	nA
t <sub>d</sub> (E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		—	—	100	μs

**NOTES:**

1. The measurement condition is V<sub>CC</sub> = 2.7 V to 5.5 V and T<sub>opr</sub> = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Ensure that V<sub>det2</sub> > V<sub>det1</sub>.

**Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency when the reset is deasserted	$V_{CC} = 5.0 \text{ V}$ , $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	8	—	MHz
—	High-speed on-chip oscillator frequency temperature • supply voltage dependence <sup>(2)</sup>	0 to +60 $^{\circ}\text{C}/5 \text{ V} \pm 5 \%$ <sup>(3)</sup>	7.76	—	8.24	MHz
		-20 to +85 $^{\circ}\text{C}/2.7 \text{ to } 5.5 \text{ V}$ <sup>(3)</sup>	7.68	—	8.32	MHz
		-40 to +85 $^{\circ}\text{C}/2.7 \text{ to } 5.5 \text{ V}$ <sup>(3)</sup>	7.44	—	8.32	MHz

## NOTES:

1. The measurement condition is  $V_{CC} = 5.0 \text{ V}$  and  $T_{opr} = 25 \text{ }^{\circ}\text{C}$ .
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

**Table 5.11 Power Supply Circuit Timing Characteristics**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on <sup>(2)</sup>		1	—	2000	$\mu\text{s}$
$t_{d(R-S)}$	STOP exit time <sup>(3)</sup>		—	—	150	$\mu\text{s}$

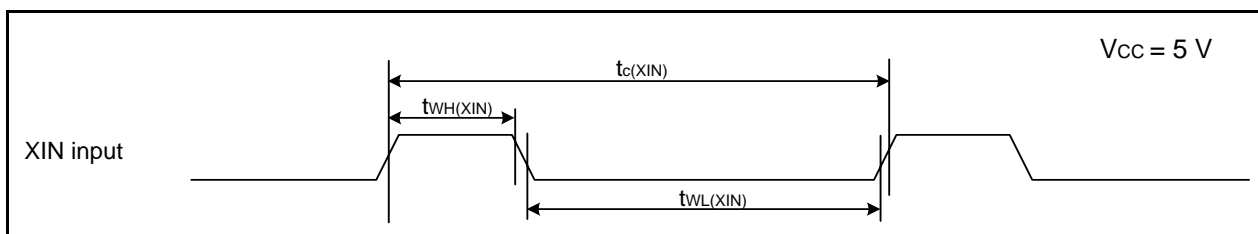
## NOTES:

1. The measurement condition is  $V_{CC} = 2.7 \text{ to } 5.5 \text{ V}$  and  $T_{opr} = 25 \text{ }^{\circ}\text{C}$ .
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

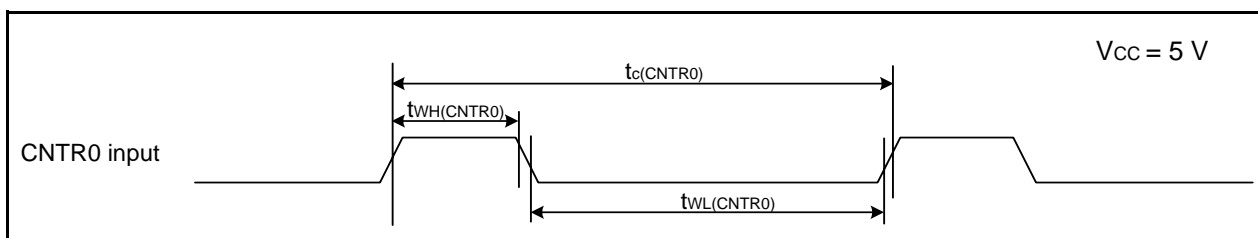


**Timing Requirements**(Unless otherwise specified:  $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_a = 25\text{ }^{\circ}\text{C}$ ) [ $V_{CC} = 5\text{ V}$ ]**Table 5.16 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

**Figure 5.8 XIN Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 5.17 CNTR0 Input, CNTR1 Input,  $\overline{INT1}$  Input**

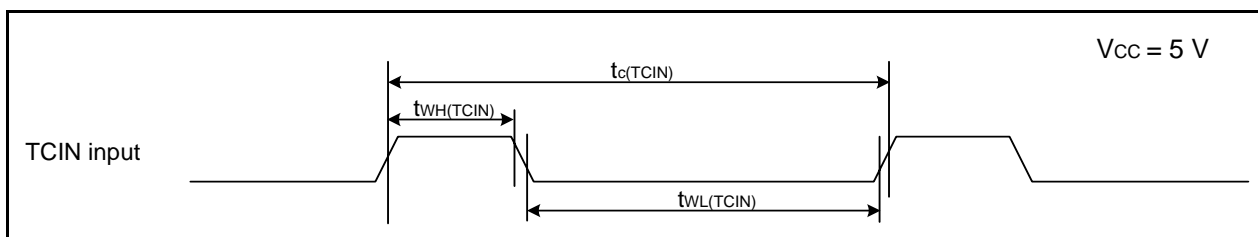
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input "H" width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input "L" width	40	–	ns

**Figure 5.9 CNTR0 Input, CNTR1 Input,  $\overline{INT1}$  Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 5.18 TCIN Input,  $\overline{INT3}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400 <sup>(1)</sup>	–	ns
$t_{WH(TCIN)}$	TCIN input "H" width	200 <sup>(2)</sup>	–	ns
$t_{WL(TCIN)}$	TCIN input "L" width	200 <sup>(2)</sup>	–	ns

**NOTES:**

1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

**Figure 5.10 TCIN Input,  $\overline{INT3}$  Input Timing Diagram when  $V_{CC} = 5\text{ V}$**

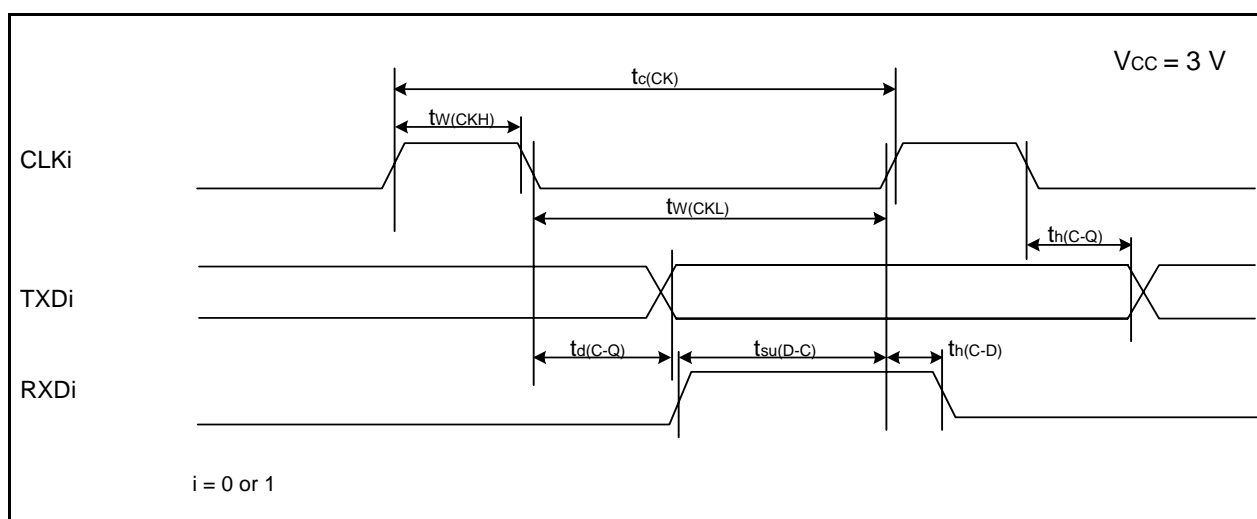
**Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -40 to 85 °C, unless otherwise specified.)**

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss, A/D converter is stopped	High-speed mode	–	8	13	mA
		High-speed mode	–	7	12	mA
		High-speed mode	–	5	–	mA
		Medium- speed mode	–	3	–	mA
		Medium- speed mode	–	2.5	–	mA
		High-speed on-chip oscillator mode	–	3.5	7.5	mA
		High-speed on-chip oscillator mode	–	1.5	–	mA
		Low-speed on-chip oscillator mode	–	100	280	μA
		Wait mode	–	37	74	μA
		Wait mode	–	35	70	μA
		Stop mode	–	0.7	3.0	μA

**Table 5.26 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input “H” width	150	—	ns
$t_{w(CKL)}$	CLKi input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

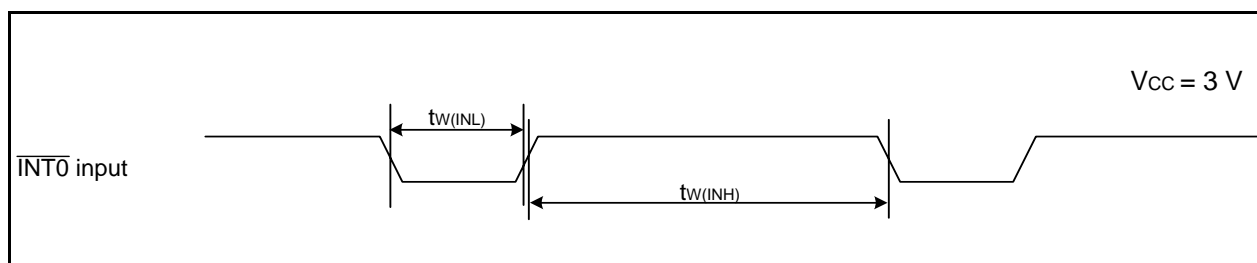
i = 0 or 1

**Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.27 External Interrupt  $\overline{INT0}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input “H” width	380 <sup>(1)</sup>	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input “L” width	380 <sup>(2)</sup>	—	ns

**NOTES:**

1. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use an  $\overline{INT0}$  input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater
2. When selecting the digital filter by the  $\overline{INT0}$  input filter select bit, use an  $\overline{INT0}$  input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater

**Figure 5.17 External Interrupt  $\overline{INT0}$  Input Timing Diagram when Vcc = 3 V**

REVISION HISTORY	R8C/1A Group, R8C/1B Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.30	Oct 03, 2006	1	1.1 "portable equipment" added
		2, 3	Table 1.1, Table 1.2; Specification Interrupts: "Internal: 9 sources" → "Internal: 11 sources"
		24	Table 5.2; Parameter: System clock added
		45	Package Dimensions; PWQN0028KA-B revised
1.40	Dec 08, 2006	20	Table 4.1; 000Fh: After reset "000XXXXXb" → "00X11111b"
		24	Table 19.2; Parameter: OCD2 = 1 On-chip oscillator clock selected revised

Notes:

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**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
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