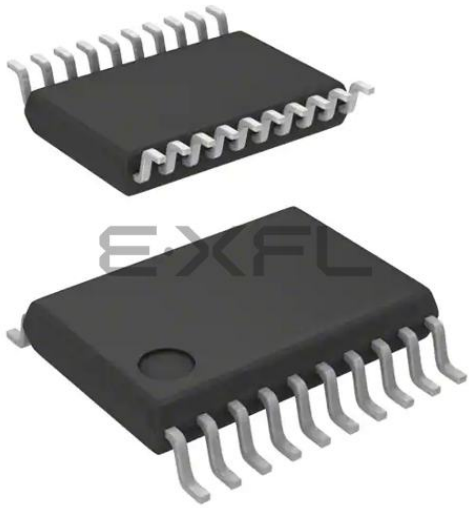

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Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f211b4sp-w4

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1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

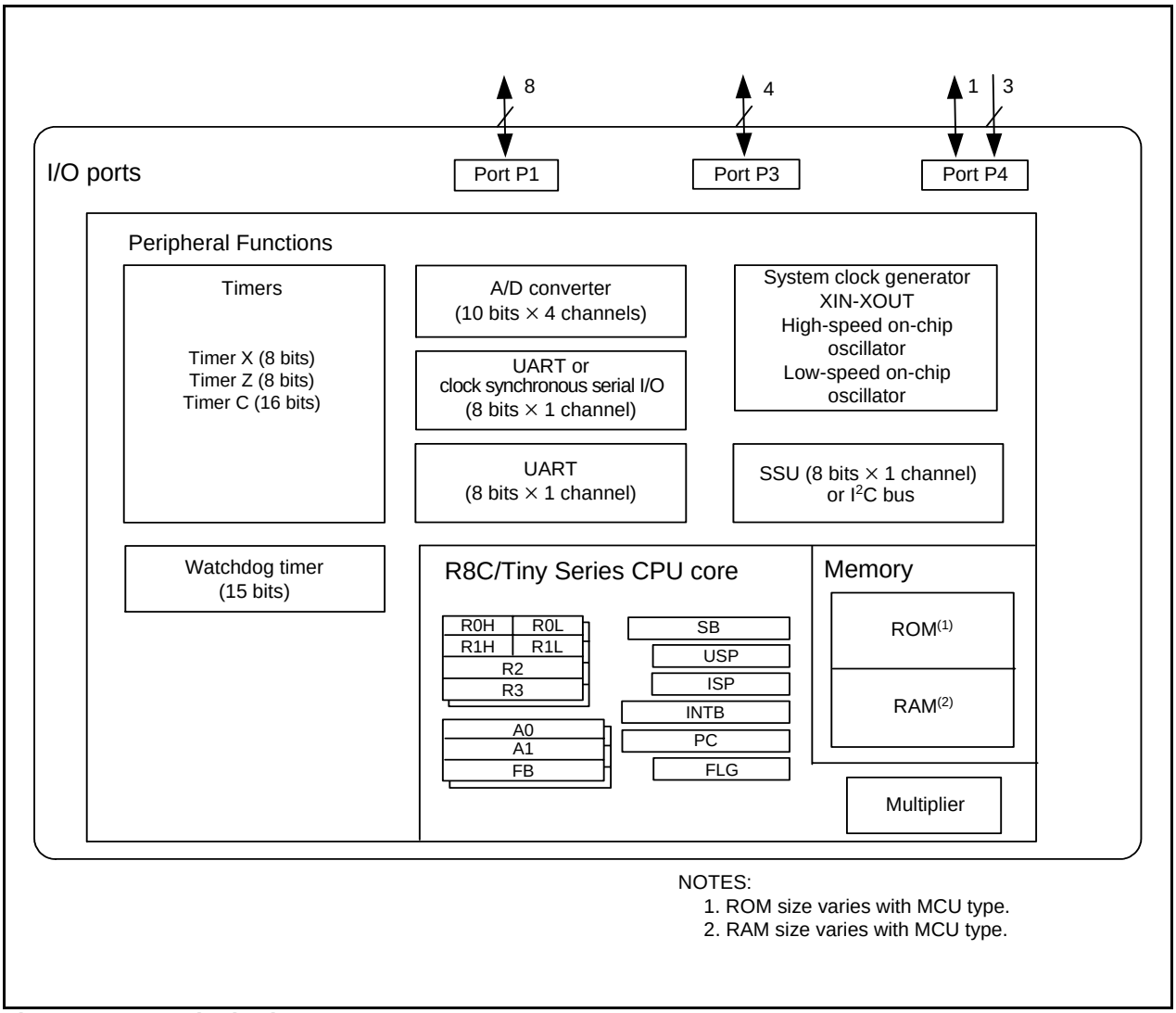


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/1A Group and Table 1.4 lists Product Information for R8C/1B Group.

Table 1.3 Product Information for R8C/1A Group Current of October 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F211A1SP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F211A2SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DD	4 Kbytes	384 bytes	PRDP0020BA-A	
R5F211A2DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2NP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	
R5F211A1XXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	Factory programming product (1)
R5F211A2XXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3XXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4XXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1DXXXSP	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F211A2DXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F211A3DXXXSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F211A4DXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F211A1XXXDD	4 Kbytes	384 bytes	PRDP0020BA-A	Factory programming product (1)
R5F211A2XXXDD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F211A3XXXDD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F211A4XXXDD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F211A2XXXNP	8 Kbytes	512 bytes	PWQN0028KA-B	
R5F211A3XXXNP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F211A4XXXNP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

NOTE:
1. The user ROM is programmed before shipment.

Table 1.4 Product Information for R8C/1B Group Current of October 2006

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F211B1SP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	
R5F211B2SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F211B2DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	
R5F211B2DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3DD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	
R5F211B1XXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	Factory programming product (1)
R5F211B2XXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3XXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4XXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1DXXXSP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F211B2DXXXSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F211B3DXXXSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F211B4DXXXSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F211B1XXXDD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Factory programming product (1)
R5F211B2XXXDD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F211B3XXXDD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F211B4XXXDD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F211B2XXXNP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	
R5F211B3XXXNP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F211B4XXXNP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

NOTE:
1. The user ROM is programmed before shipment.

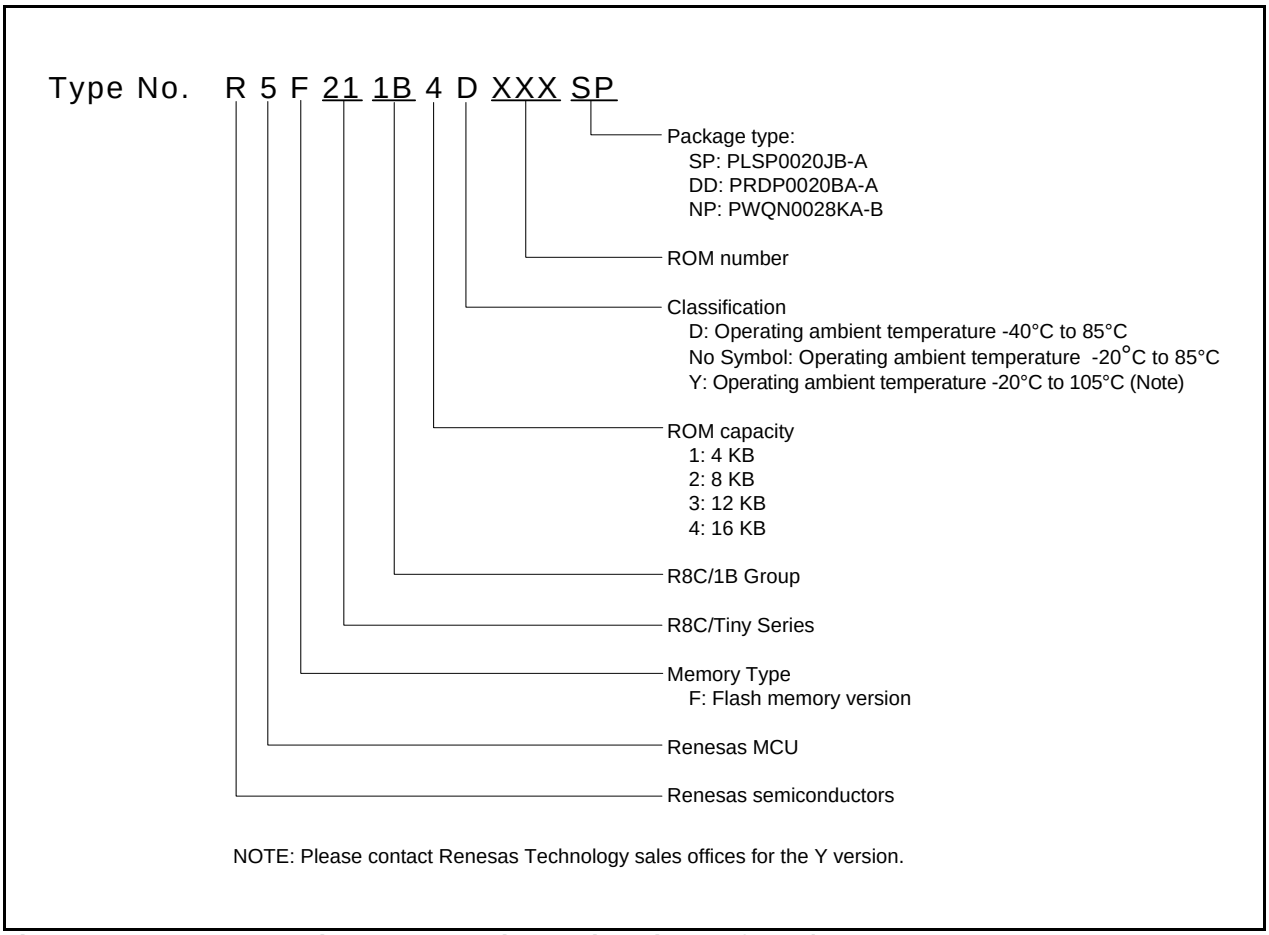


Figure 1.3 Type Number, Memory Size, and Package of R8C/1B Group

Table 1.6 Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A Packages

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
1		P3_5		CMP1_2		SSCK	SCL	
2		P3_7		$\overline{\text{CNTR0}}$	TXD1	SSO		
3	$\overline{\text{RESET}}$							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	$\overline{\text{INT0}}$		RXD1			
10		P1_7	$\overline{\text{INT10}}$	CNTR00				
11		P1_6			CLK0	SSI01		
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0			
13		P1_4			TXD0			
14		P1_3	$\overline{\text{KI3}}$	TZOUT				AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2				AN10
16	VREF	P4_2						
17		P1_1	$\overline{\text{KI1}}$	CMP0_1				AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0				AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/ CMP1_0		SSI00		
20		P3_4		CMP1_1		$\overline{\text{SCS}}$	SDA	

Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B Package

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
1	NC							
2	XOUT	P4_7						
3	VSS/AVSS							
4	NC							
5	NC							
6	XIN	P4_6						
7	NC							
8	VCC/AVCC							
9	MODE							
10		P4_5	$\overline{INT0}$		RXD1			
11		P1_7	$\overline{INT10}$	CNTR00				
12		P1_6			CLK0	SSI01		
13		P1_5	$\overline{INT11}$	CNTR01	RXD0			
14		P1_4			TXD0			
15	NC							
16		P1_3	$\overline{KI3}$	TZOUT				AN11
17		P1_2	$\overline{KI2}$	CMP0_2				AN10
18	NC							
19	NC							
20	VREF	P4_2						
21	NC							
22		P1_1	$\overline{KI1}$	CMP0_1				AN9
23		P1_0	$\overline{KI0}$	CMP0_0				AN8
24		P3_3	$\overline{INT3}$	TCIN/CMP1_0		SSI00		
25		P3_4		CMP1_1		$\overline{SCS}$	SDA	
26		P3_5		CMP1_2		SSCK	SCL	
27		P3_7		$\overline{CNTR0}$	TXD1	SSO		
28	$\overline{RESET}$							

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

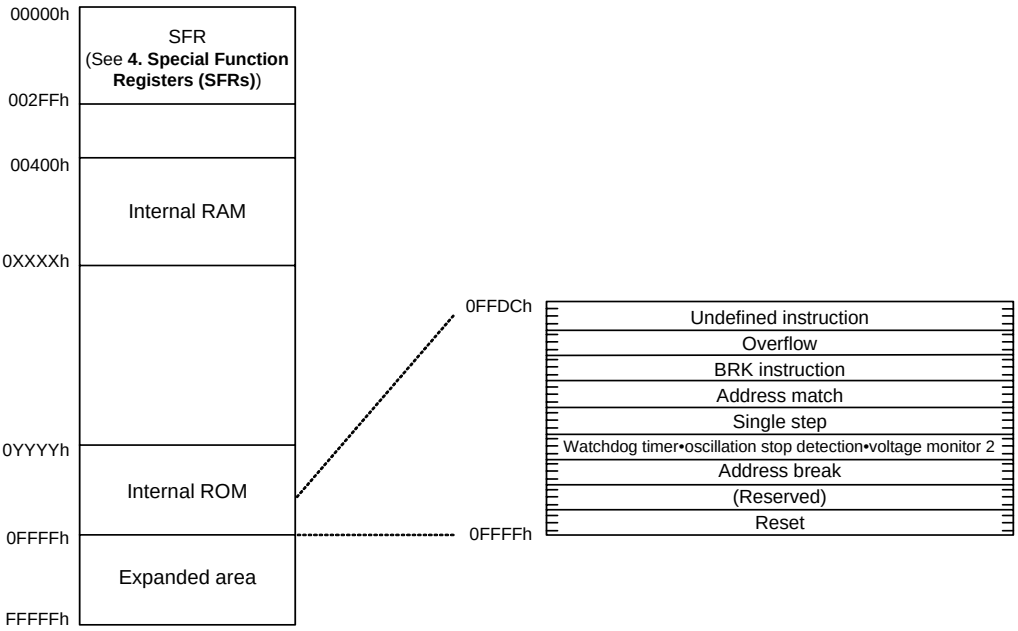
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/1A Group

Figure 3.1 is a Memory Map of R8C/1A Group. The R8C/1A Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F211A4SP, R5F211A4DSP, R5F211A4DD, R5F211A4NP, R5F211A4XXXSP, R5F211A4DXXXSP, R5F211A4XXXDD, R5F211A4XXXNP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F211A3SP, R5F211A3DSP, R5F211A3DD, R5F211A3NP, R5F211A3XXXSP, R5F211A3DXXXSP, R5F211A3XXXDD, R5F211A3XXXNP	12 Kbytes	0D000h	768 bytes	006FFh
R5F211A2SP, R5F211A2DSP, R5F211A2DD, R5F211A2NP, R5F211A2XXXSP, R5F211A2DXXXSP, R5F211A2XXXDD, R5F211A2XXXNP	8 Kbytes	0E000h	512 bytes	005FFh
R5F211A1SP, R5F211A1DSP, R5F211A1DD, R5F211A1XXXSP, R5F211A1DXXXSP, R5F211A1XXXDD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.1 Memory Map of R8C/1A Group

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/1A Group	100(3)	–	–	times
		R8C/1B Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(8)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time Delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85 °C / –40 to 85 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

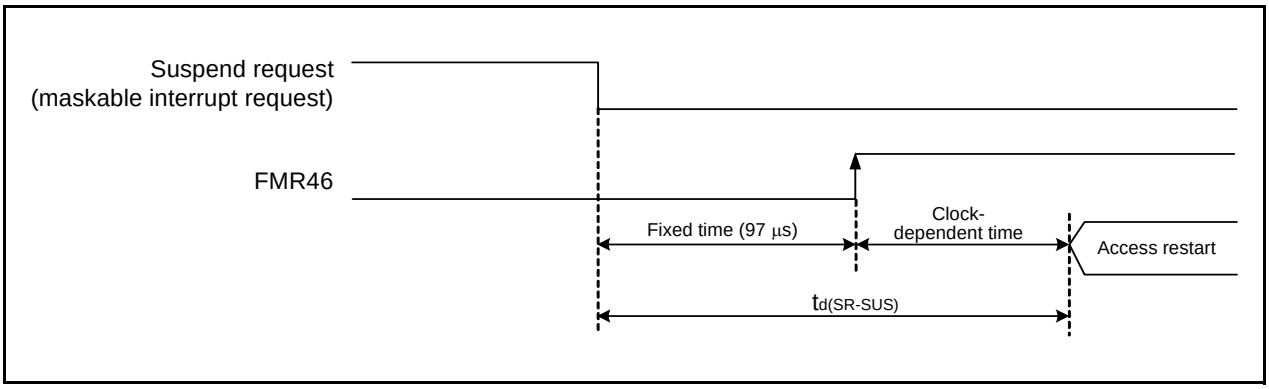


Figure 5.2 Transition Time to Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3)		2.70	2.85	3.00	V
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Ensure that $V_{det2} > V_{det1}$.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.00	3.30	3.60	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	600	–	nA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Ensure that $V_{det2} > V_{det1}$.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

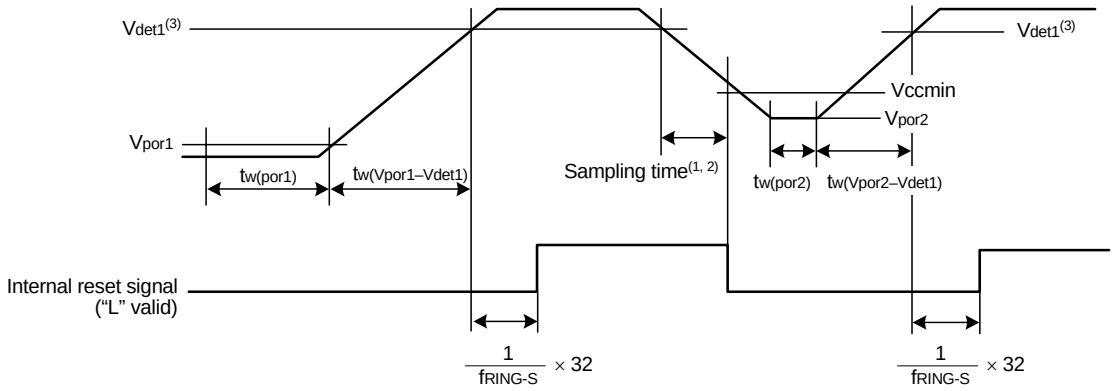
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted(1)	-20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2)	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with Vcc≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC}+50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC}+50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1.5t_{CYC}+100	ns
t_{OR}	SSI slave out open time			–	–	1.5t_{CYC}+100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Ta = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

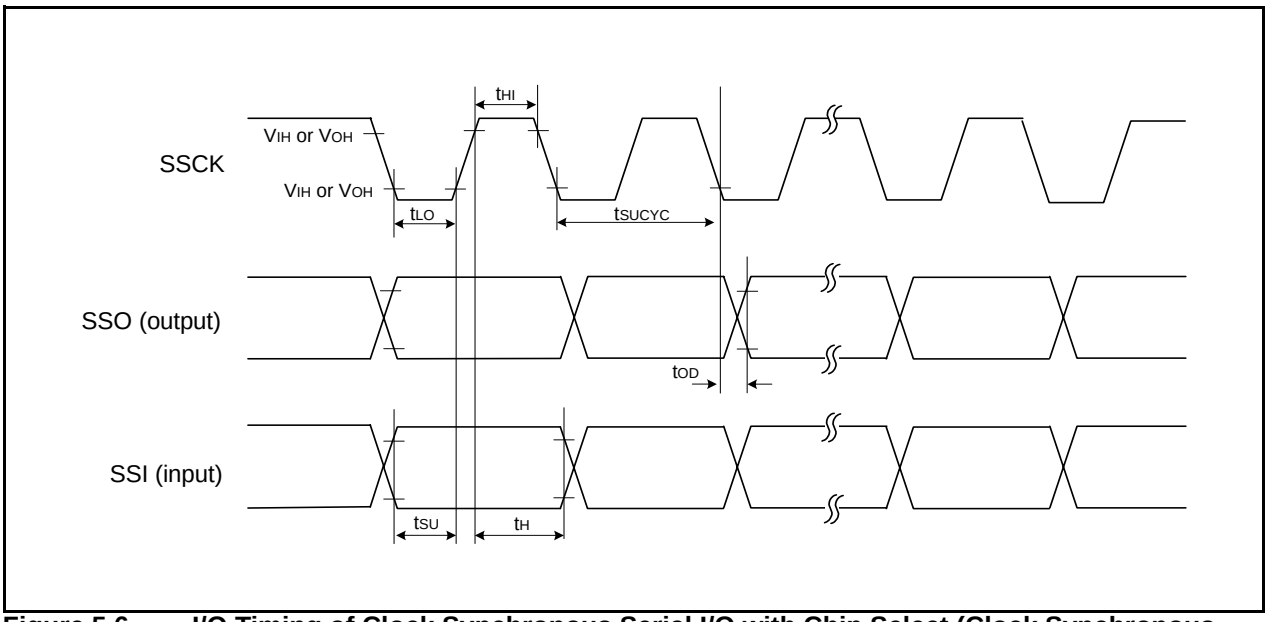


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

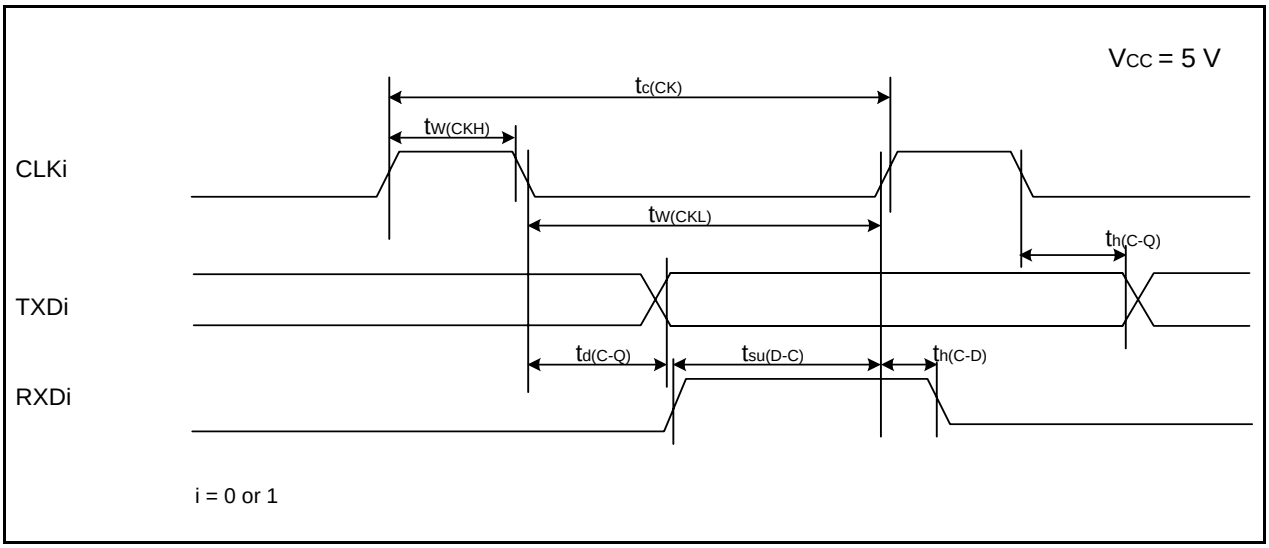


Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.20 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

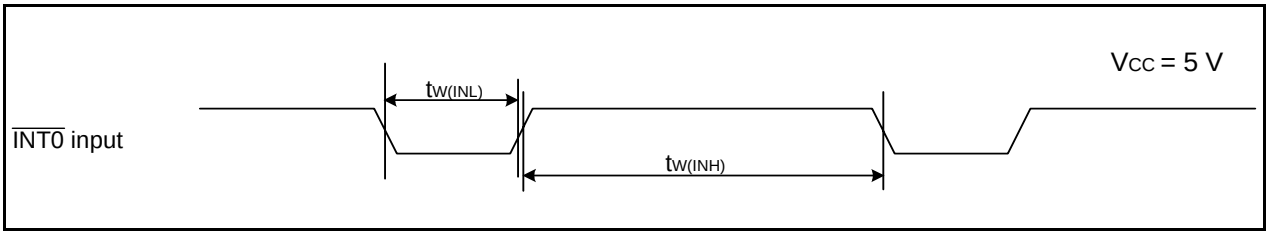


Figure 5.12 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 5 V

Timing requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Ta = 25 °C) [Vcc = 3 V]

Table 5.23 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

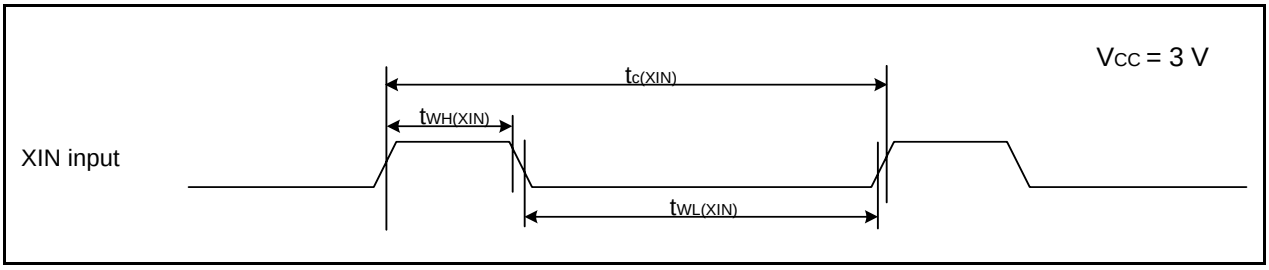


Figure 5.13 XIN Input Timing Diagram when Vcc = 3 V

Table 5.24 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	120	–	ns

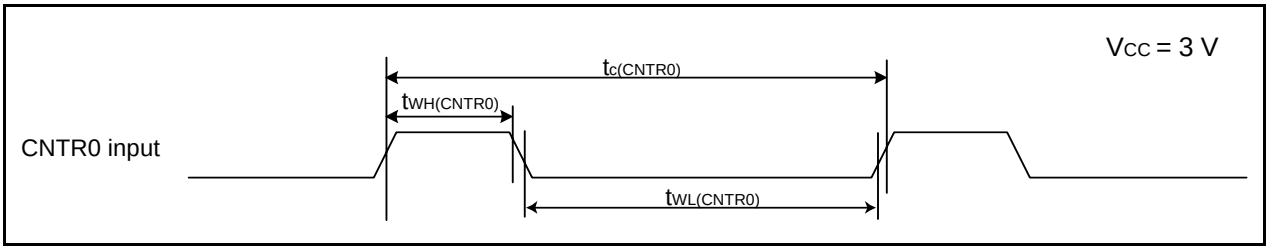


Figure 5.14 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 3 V

Table 5.25 TCIN Input, $\overline{\text{INT3}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	600(2)	–	ns

NOTES:
1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency x 1.5) or above.

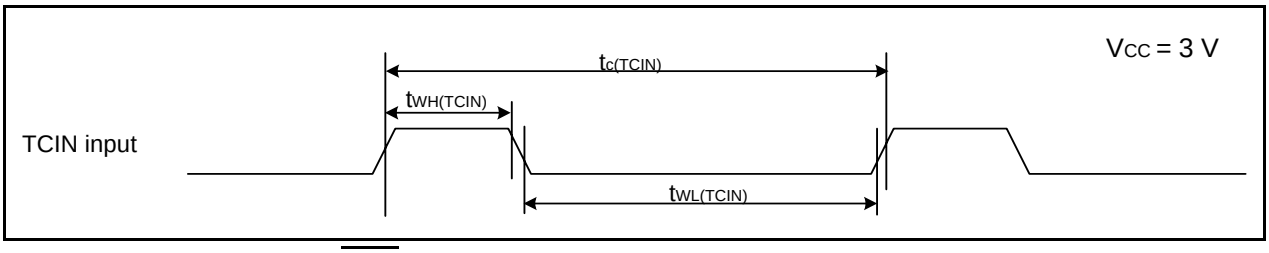
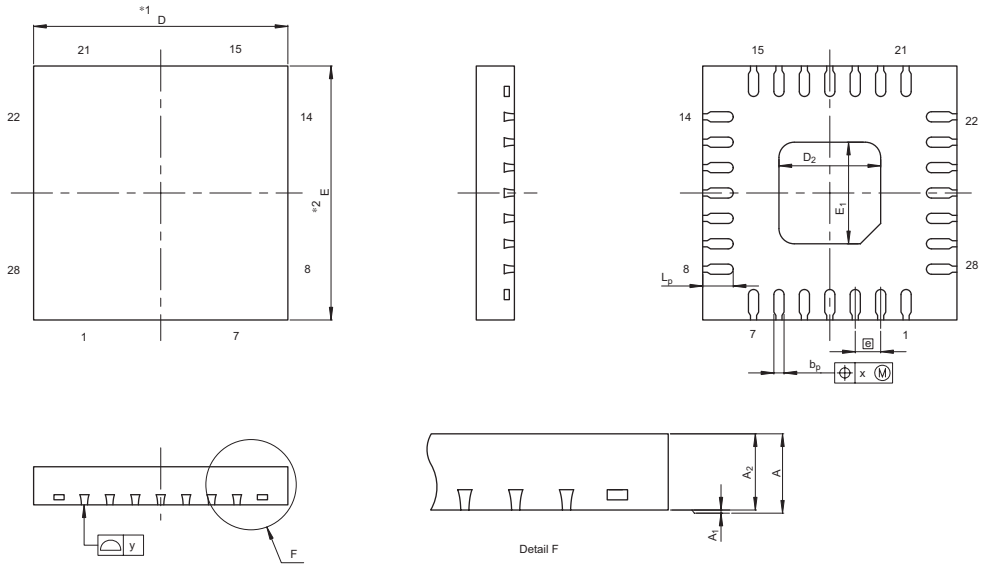


Figure 5.15 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 3 V

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN28-5x5-0.50	PWQN0028KA-B	28PJW-B	0.05g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.9	5.0	5.1
A_2	—	0.75	—
A	—	—	0.8
A_1	0	0	0.05
b_p	0.15	0.2	0.25
e	—	0.5	—
L_p	0.5	0.6	0.7
x	—	—	0.05
y	—	—	0.05
D_2	—	2.0	—
E_1	—	2.0	—

REVISION HISTORY	R8C/1A Group, R8C/1B Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.30	Oct 03, 2006	1	1.1 “portable equipment” added
		2, 3	Table 1.1, Table 1.2; Specification Interrupts: “Internal: 9 sources” → “Internal: 11 sources”
		24	Table 5.2; Parameter: System clock added
		45	Package Dimensions; PWQN0028KA-B revised
1.40	Dec 08, 2006	20	Table 4.1; 000Fh: After reset “000XXXXXb” → “00X11111b”
		24	Table 19.2; Parameter: OCD2 = 1 On-chip oscillator clock selected revised

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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