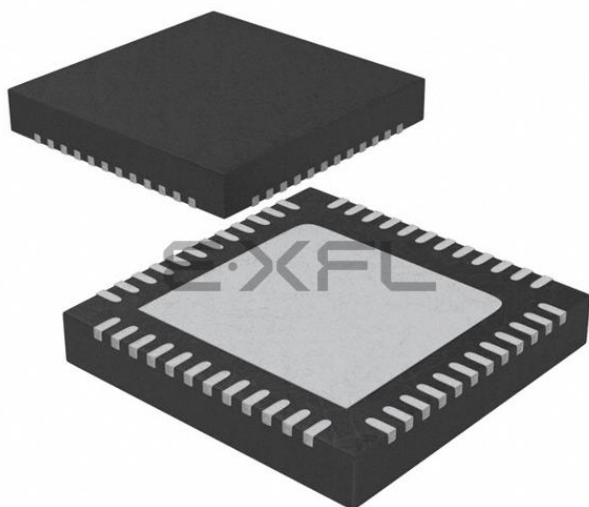




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, TSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl16z128vft4

Ordering Information ¹

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKL16Z32VFM4	32	4	28
MKL16Z64VFM4	64	8	28
MKL16Z128VFM4	128	16	28
MKL16Z32VFT4	32	4	40
MKL16Z64VFT4	64	8	40
MKL16Z128VFT4	128	16	40
MKL16Z32VLH4	32	4	54
MKL16Z64VLH4	64	8	54
MKL16Z128VLH4	128	16	54

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL16P64M48SF5RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL16P64M48SF5 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN15J ²
Package drawing	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D ¹ QFN 48-pin: 98ASA00466D ¹ LQFP 64-pin: 98ASS23234W ¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term with the “x” replaced by the revision of the device you are using.

Table of Contents

1 Ratings.....	4	3.6.2 CMP and 6-bit DAC electrical specifications.....	29
1.1 Thermal handling ratings.....	4	3.6.3 12-bit DAC electrical characteristics.....	31
1.2 Moisture handling ratings.....	4	3.7 Timers.....	34
1.3 ESD handling ratings.....	4	3.8 Communication interfaces.....	34
1.4 Voltage and current operating ratings.....	4	3.8.1 SPI switching specifications.....	34
2 General.....	5	3.8.2 Inter-Integrated Circuit Interface (I2C) timing.....	39
2.1 AC electrical characteristics.....	5	3.8.3 UART.....	40
2.2 Nonswitching electrical specifications.....	5	3.8.4 I2S/SAI switching specifications.....	40
2.2.1 Voltage and current operating requirements.....	6	3.9 Human-machine interfaces (HMI).....	44
2.2.2 LVD and POR operating requirements.....	6	3.9.1 TSI electrical specifications.....	44
2.2.3 Voltage and current operating behaviors.....	7	4 Dimensions.....	45
2.2.4 Power mode transition operating behaviors.....	8	4.1 Obtaining package dimensions.....	45
2.2.5 Power consumption operating behaviors.....	9	5 Pinout.....	45
2.2.6 EMC radiated emissions operating behaviors... ..	14	5.1 KL16 Signal Multiplexing and Pin Assignments.....	45
2.2.7 Designing with radiated emissions in mind.....	15	5.2 KL16 pinouts.....	48
2.2.8 Capacitance attributes.....	15	6 Ordering parts.....	51
2.3 Switching specifications.....	15	6.1 Determining valid orderable parts.....	51
2.3.1 Device clock specifications.....	15	7 Part identification.....	51
2.3.2 General switching specifications.....	16	7.1 Description.....	52
2.4 Thermal specifications.....	16	7.2 Format.....	52
2.4.1 Thermal operating requirements.....	16	7.3 Fields.....	52
2.4.2 Thermal attributes.....	17	7.4 Example.....	52
3 Peripheral operating requirements and behaviors.....	17	8 Terminology and guidelines.....	53
3.1 Core modules.....	17	8.1 Definition: Operating requirement.....	53
3.1.1 SWD electricals	17	8.2 Definition: Operating behavior.....	53
3.2 System modules.....	19	8.3 Definition: Attribute.....	53
3.3 Clock modules.....	19	8.4 Definition: Rating.....	54
3.3.1 MCG specifications.....	19	8.5 Result of exceeding a rating.....	54
3.3.2 Oscillator electrical specifications.....	21	8.6 Relationship between ratings and operating requirements.....	54
3.4 Memories and memory interfaces.....	23	8.7 Guidelines for ratings and operating requirements.....	55
3.4.1 Flash electrical specifications.....	23	8.8 Definition: Typical value.....	55
3.5 Security and integrity modules.....	24	8.9 Typical value conditions.....	56
3.6 Analog.....	24	9 Revision history.....	57
3.6.1 ADC electrical specifications.....	24		

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description		Temperature (°C)						Unit
			-40	25	50	70	85	105	
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.		52	52	52	52	52	52	μA
I _{IREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.		206	228	237	245	251	258	μA
I _{IREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	560	570	580	nA
		VLLS3	440	490	540	560	570	580	
		LLS	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.		432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.		45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by		366	366	366	366	366	366	μA

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.							

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

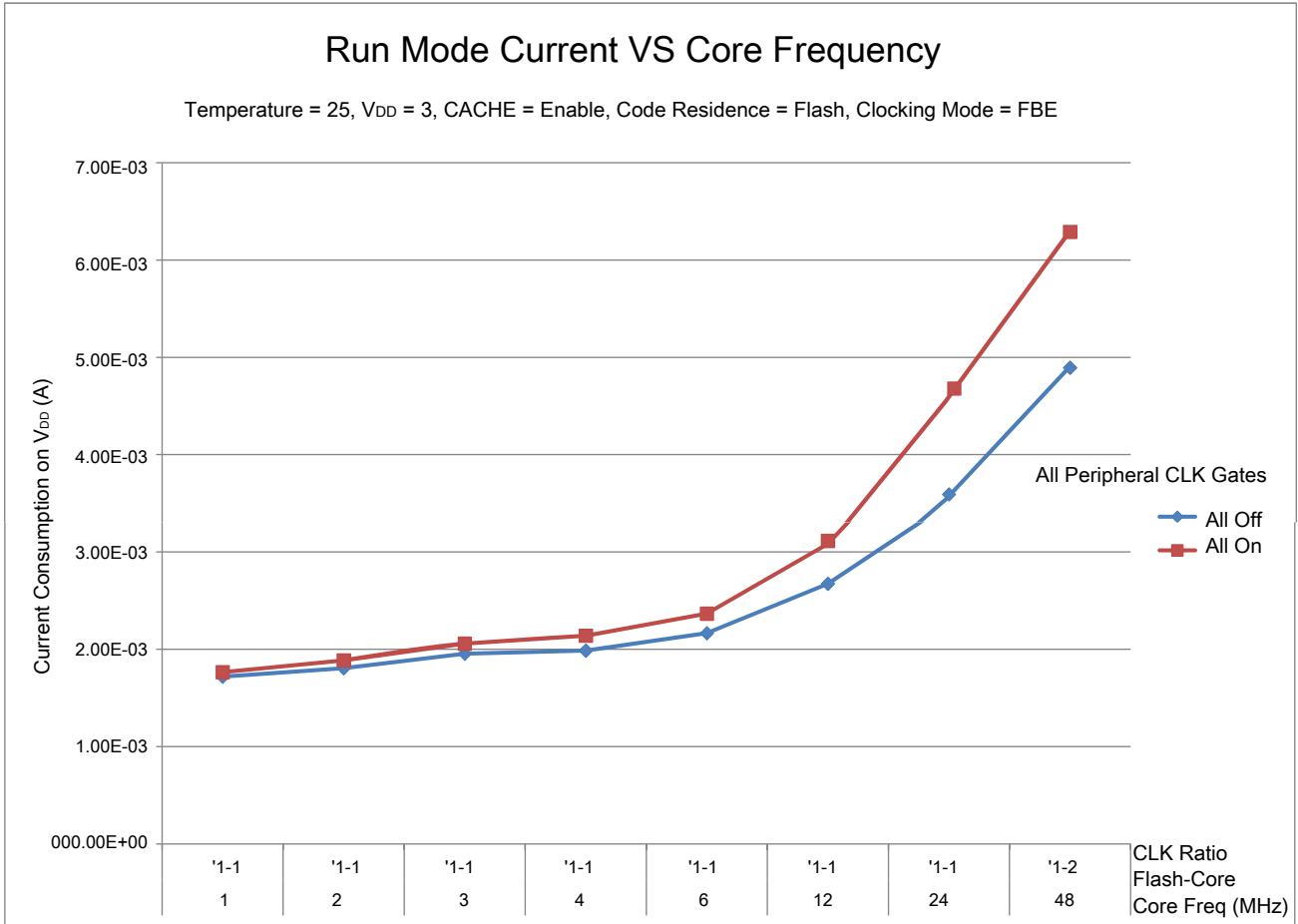


Figure 2. Run mode supply current vs. core frequency

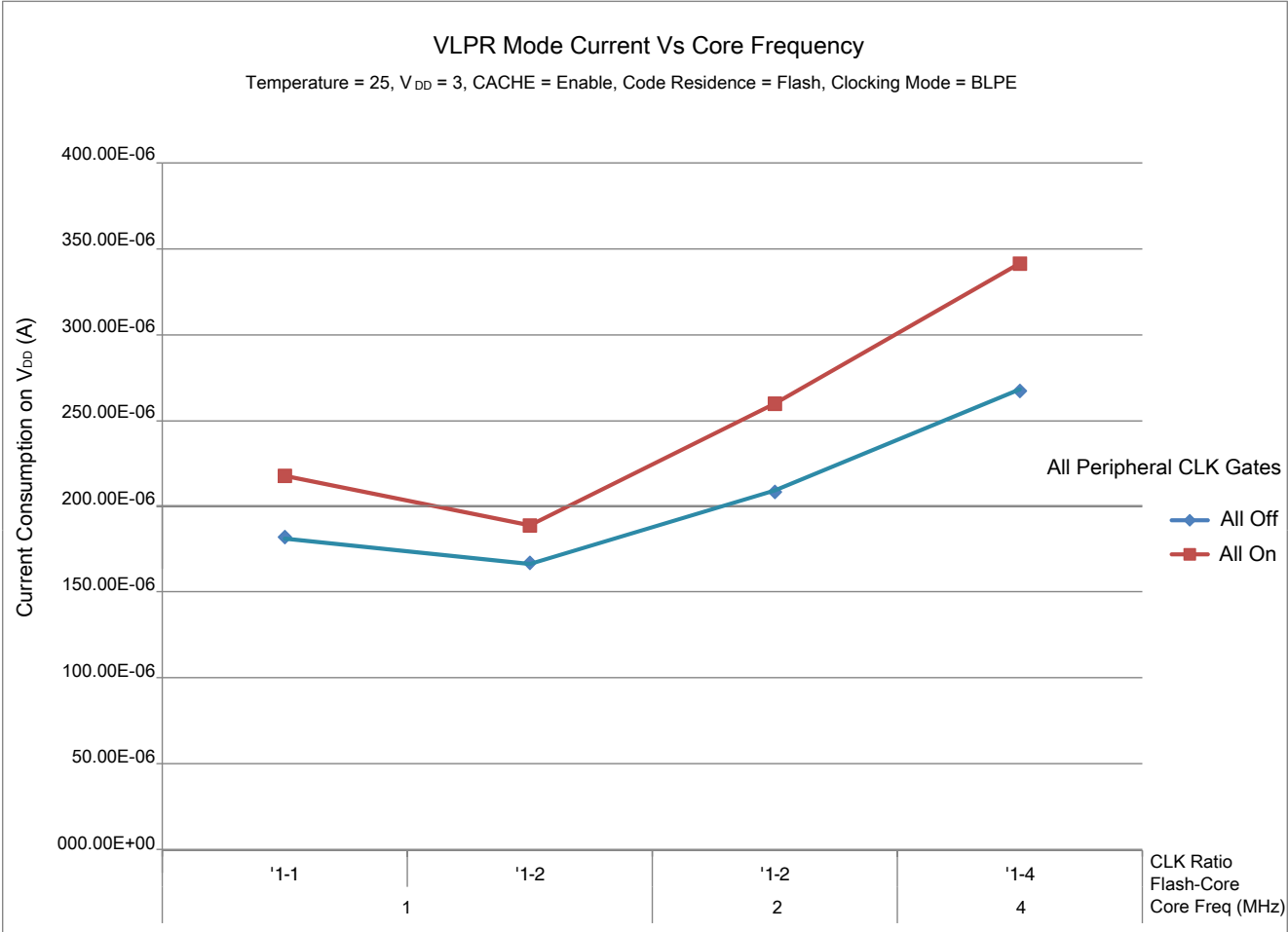


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	16	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	18	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	11	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	13	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

Table 13. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit
$f_{\text{LPTMR_ERCLK}}$	LPTMR external reference clock	—	16	MHz
$f_{\text{osc_hi_2}}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	83	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	30	34	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	68	82	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	24	28	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	12	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	2.3	2.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	6	5	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		$732 \times f_{\text{fill_ref}}$				
		Mid range (DRS = 01)	—	47.97	—	
		$1464 \times f_{\text{fill_ref}}$			MHz	
$J_{\text{cyc_fll}}$	FLL period jitter $f_{\text{VCO}} = 48 \text{ MHz}$	—	180	—	ps	7
$t_{\text{fll_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	8
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current PLL at 96 MHz ($f_{\text{osc_hi_1}} = 8 \text{ MHz}$, $f_{\text{pll_ref}} = 2 \text{ MHz}$, VDIV multiplier = 48)	—	1060	—	μA	9
I_{pll}	PLL operating current PLL at 48 MHz ($f_{\text{osc_hi_1}} = 8 \text{ MHz}$, $f_{\text{pll_ref}} = 2 \text{ MHz}$, VDIV multiplier = 24)	—	600	—	μA	9
$f_{\text{pll_ref}}$	PLL reference frequency range	2.0	—	4.0	MHz	
$J_{\text{cyc_pll}}$	PLL period jitter (RMS) $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 100 \text{ MHz}$	— —	120 50	— —	ps ps	10
$J_{\text{acc_pll}}$	PLL accumulated jitter over 1μs (RMS) $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 100 \text{ MHz}$	— —	1350 600	— —	ps ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
$t_{\text{pll_lock}}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{\text{pll_ref}})$	s	11

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, $f_{\text{ints_ft}}$.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{\text{dco_t}}$) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μ A	
	• 8 MHz (RANGE=01)	—	300	—	μ A	
	• 16 MHz	—	950	—	μ A	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μ A	
	• 4 MHz	—	400	—	μ A	
	• 8 MHz (RANGE=01)	—	500	—	μ A	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)					

Table continues on the next page...

6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

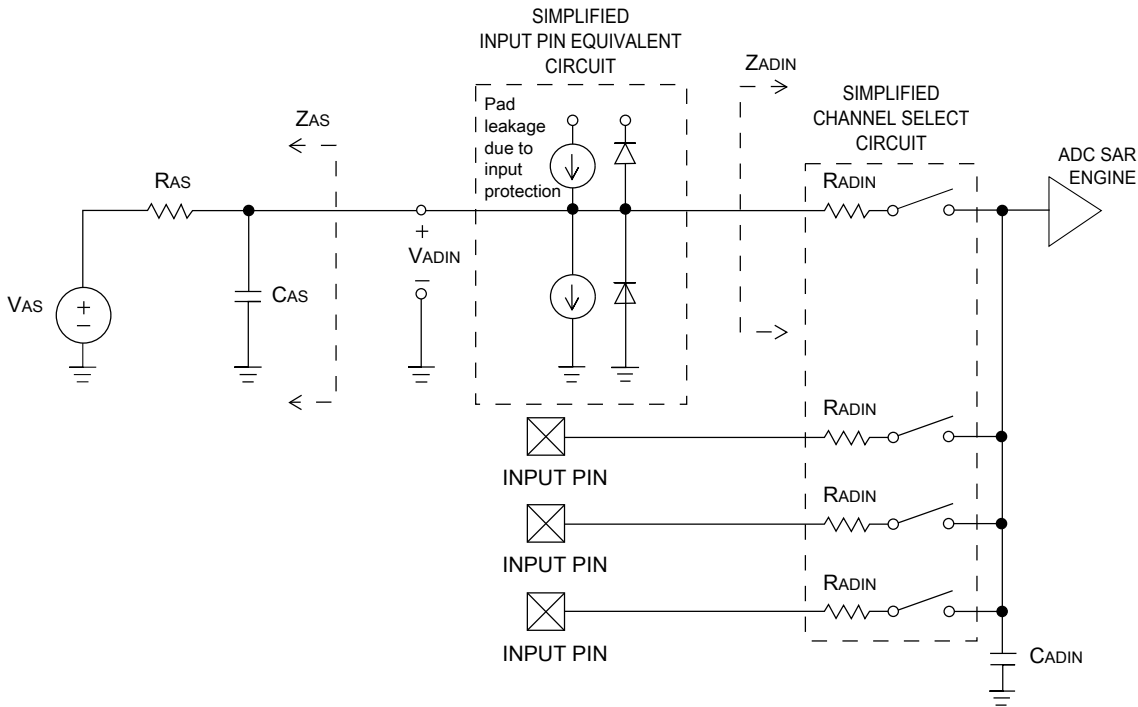


Figure 6. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5

Table continues on the next page...

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
DNL	Differential non-linearity	12-bit modes <12-bit modes	—	±0.7	–1.1 to +1.9	LSB ⁴	5
			—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	12-bit modes <12-bit modes	—	±1.0	–2.7 to +1.9	LSB ⁴	5
			—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	12-bit modes <12-bit modes	—	–4	–5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
			—	–1.4	–1.8		
E_Q	Quantization error	16-bit modes ≤13-bit modes	—	–1 to 0	—	LSB ⁴	
			—	—	±0.5		
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	–94 –85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{IN} \times R_{AS}$			mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)

Table continues on the next page...

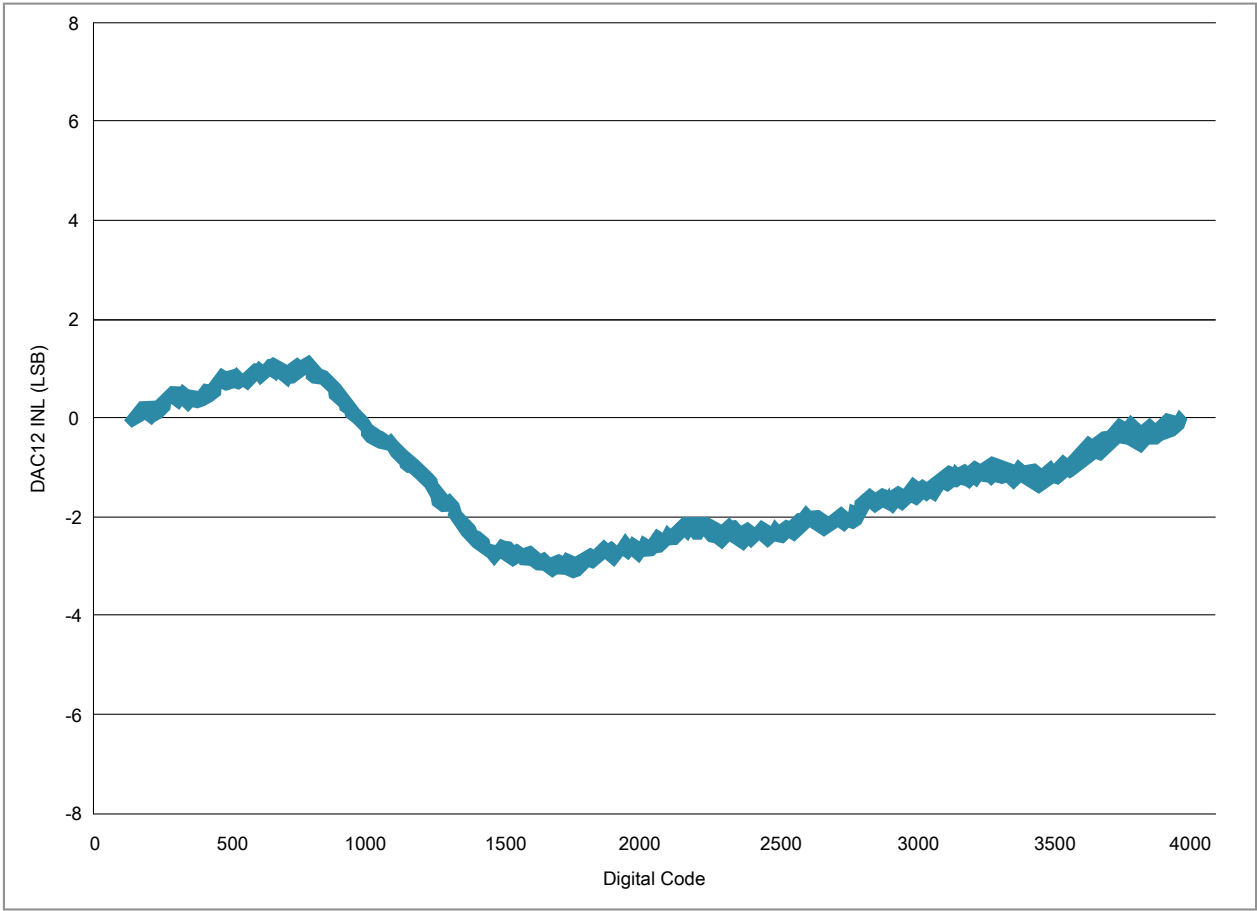


Figure 11. Typical INL error vs. digital code

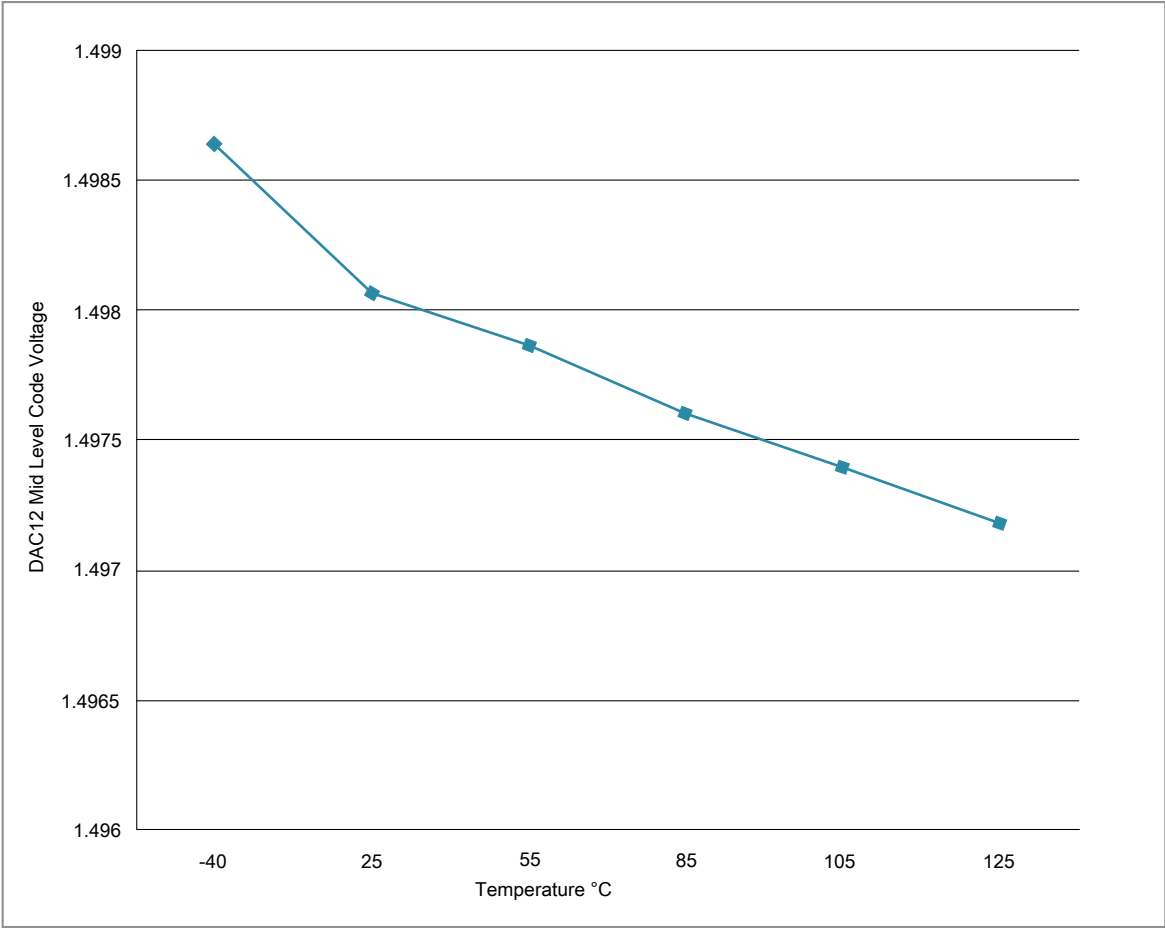


Figure 12. Offset at half scale vs. temperature

3.7 Timers

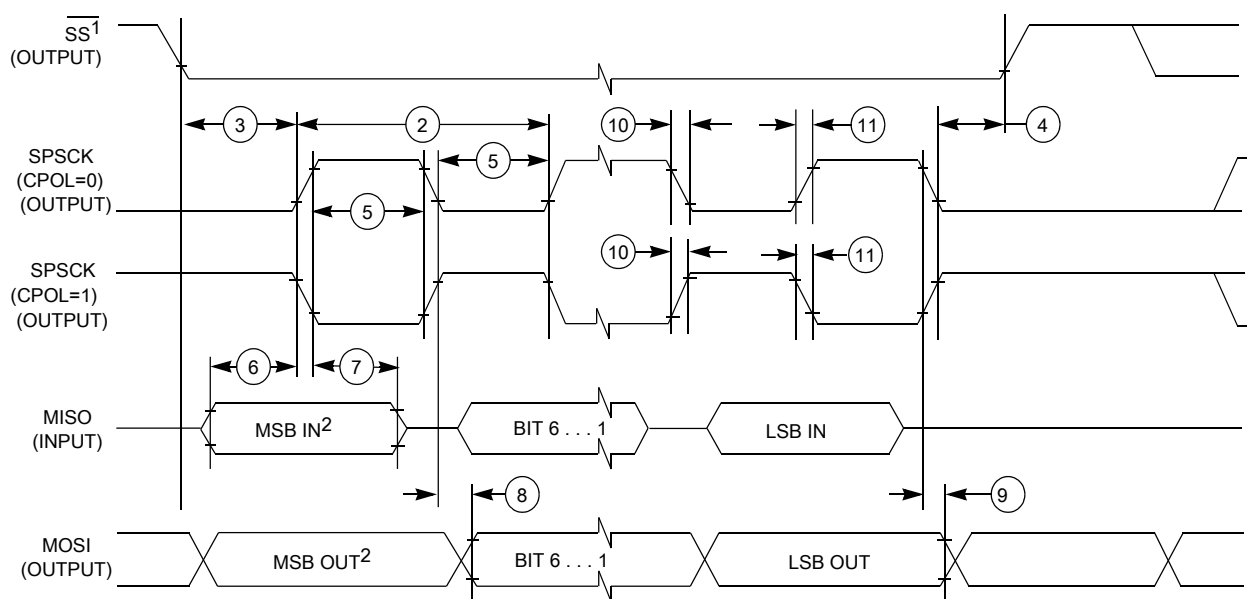
See [General switching specifications](#).

3.8 Communication interfaces

Table 31. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t_v	Data valid (after SPSCCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{\text{periph}} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{\text{periph}} = 1/f_{\text{periph}}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 13. SPI master mode timing (CPHA = 0)

Table 33. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{periph} - 25$	ns	—
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output	—	36	ns	—

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

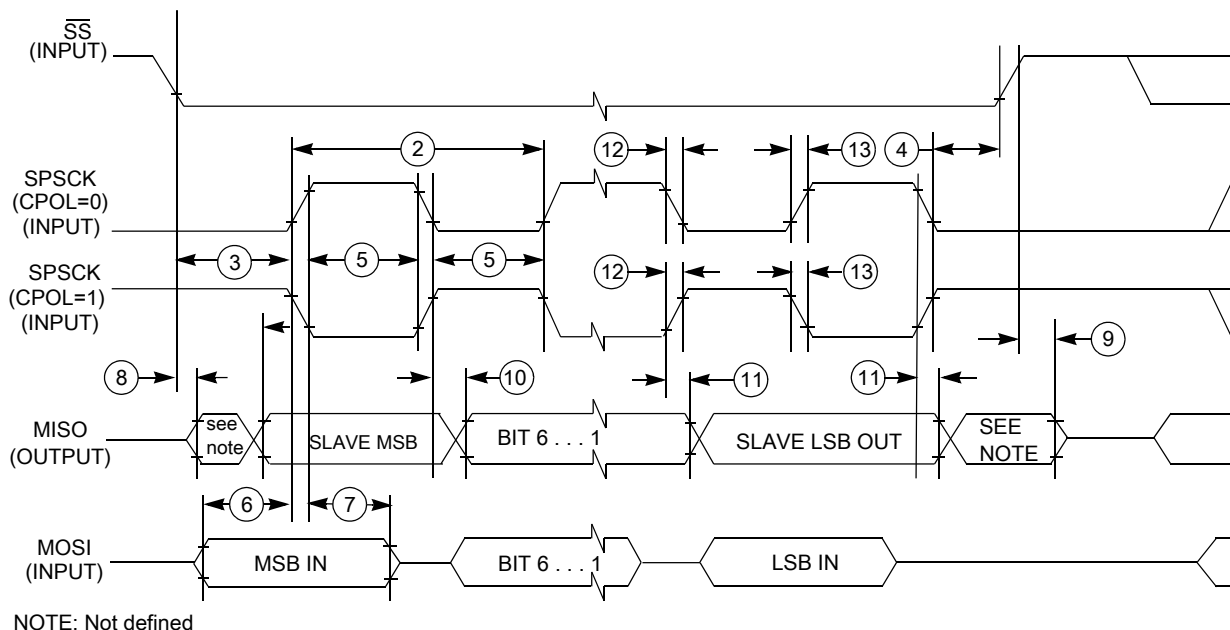


Figure 15. SPI slave mode timing (CPHA = 0)

Table 36. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

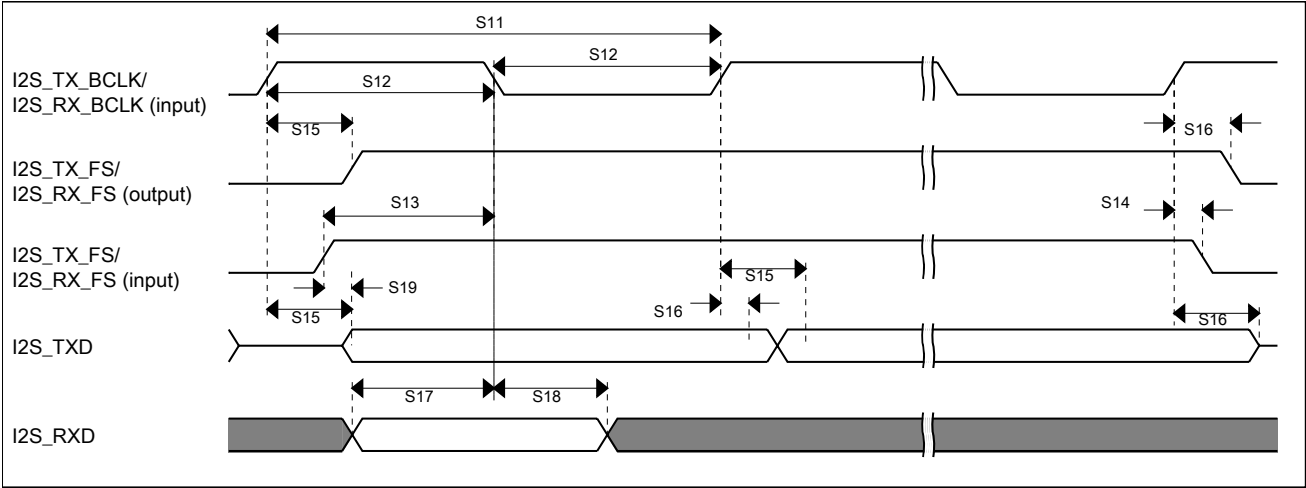


Figure 19. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 39. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00473D
48-pin QFN	98ASA00466D
64-pin LQFP	98ASS23234W

5 Pinout

5.1 KL16 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
KL##	Kinetis family	KL16
A	Key attribute	Z = Cortex-M0+
FFF	Program flash memory size	32 = 32 KB 64 = 64 KB 128 = 128 KB
R	Silicon revision	(Blank) = Main - A = Revision after main
T	Temperature range (°C)	V = -40 to 105
PP	Package identifier	- FM = 32 QFN (5 mm x 5 mm) - FT = 48 QFN (7 mm x 7 mm) - LH = 64 LQFP (10 mm x 10 mm)
CC	Maximum CPU frequency (MHz)	4 = 48 MHz
N	Packaging type	R = Tape and reel

7.4 Example

This is an example part number:

MKL16Z128VFM4

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF