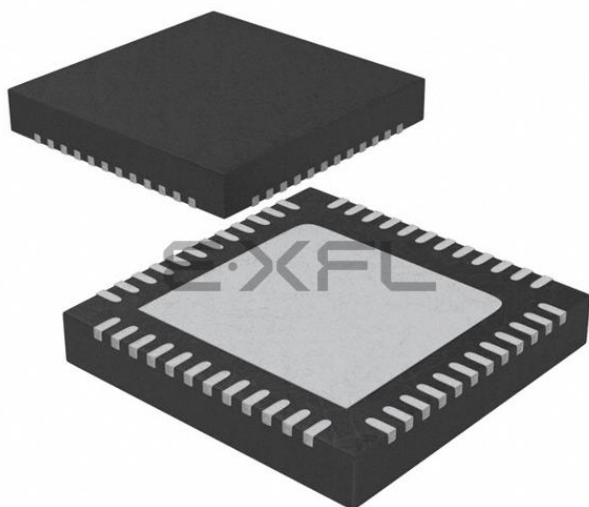




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, TSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl16z128vft4r

Table of Contents

1 Ratings.....	4	3.6.2 CMP and 6-bit DAC electrical specifications.....	29
1.1 Thermal handling ratings.....	4	3.6.3 12-bit DAC electrical characteristics.....	31
1.2 Moisture handling ratings.....	4	3.7 Timers.....	34
1.3 ESD handling ratings.....	4	3.8 Communication interfaces.....	34
1.4 Voltage and current operating ratings.....	4	3.8.1 SPI switching specifications.....	34
2 General.....	5	3.8.2 Inter-Integrated Circuit Interface (I2C) timing.....	39
2.1 AC electrical characteristics.....	5	3.8.3 UART.....	40
2.2 Nonswitching electrical specifications.....	5	3.8.4 I2S/SAI switching specifications.....	40
2.2.1 Voltage and current operating requirements.....	6	3.9 Human-machine interfaces (HMI).....	44
2.2.2 LVD and POR operating requirements.....	6	3.9.1 TSI electrical specifications.....	44
2.2.3 Voltage and current operating behaviors.....	7	4 Dimensions.....	45
2.2.4 Power mode transition operating behaviors.....	8	4.1 Obtaining package dimensions.....	45
2.2.5 Power consumption operating behaviors.....	9	5 Pinout.....	45
2.2.6 EMC radiated emissions operating behaviors... ..	14	5.1 KL16 Signal Multiplexing and Pin Assignments.....	45
2.2.7 Designing with radiated emissions in mind.....	15	5.2 KL16 pinouts.....	48
2.2.8 Capacitance attributes.....	15	6 Ordering parts.....	51
2.3 Switching specifications.....	15	6.1 Determining valid orderable parts.....	51
2.3.1 Device clock specifications.....	15	7 Part identification.....	51
2.3.2 General switching specifications.....	16	7.1 Description.....	52
2.4 Thermal specifications.....	16	7.2 Format.....	52
2.4.1 Thermal operating requirements.....	16	7.3 Fields.....	52
2.4.2 Thermal attributes.....	17	7.4 Example.....	52
3 Peripheral operating requirements and behaviors.....	17	8 Terminology and guidelines.....	53
3.1 Core modules.....	17	8.1 Definition: Operating requirement.....	53
3.1.1 SWD electricals	17	8.2 Definition: Operating behavior.....	53
3.2 System modules.....	19	8.3 Definition: Attribute.....	53
3.3 Clock modules.....	19	8.4 Definition: Rating.....	54
3.3.1 MCG specifications.....	19	8.5 Result of exceeding a rating.....	54
3.3.2 Oscillator electrical specifications.....	21	8.6 Relationship between ratings and operating requirements.....	54
3.4 Memories and memory interfaces.....	23	8.7 Guidelines for ratings and operating requirements.....	55
3.4.1 Flash electrical specifications.....	23	8.8 Definition: Typical value.....	55
3.5 Security and integrity modules.....	24	8.9 Typical value conditions.....	56
3.6 Analog.....	24	9 Revision history.....	57
3.6.1 ADC electrical specifications.....	24		

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1H}	Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V_{LVW1L}	Low-voltage warning thresholds — low range Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	1
V_{LVW2L}	Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except RESET_b) 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
V_{OH}	Output high voltage — High drive pad (except RESET_b) 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	— —	0.5 0.5	V V	1

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — High drive pad				1
	• 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 10 mA	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	—	65	μA	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R _{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• VLLS0 → RUN	—	106	120	μs	

Table continues on the next page...

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 8\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes ¹				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock ²	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz

Table continues on the next page...

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	83	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	30	34	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	68	82	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	24	28	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	12	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	2.3	2.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	6	5	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 17. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

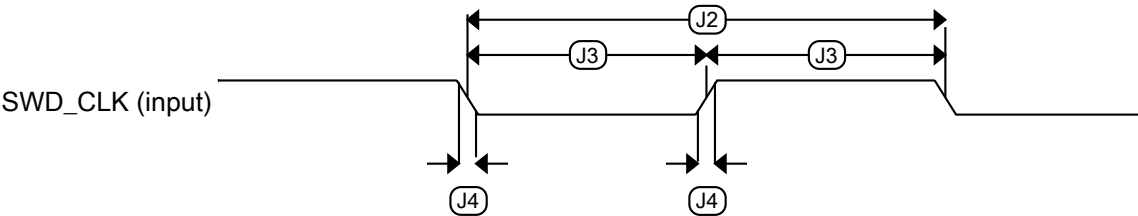


Figure 4. Serial wire clock input timing

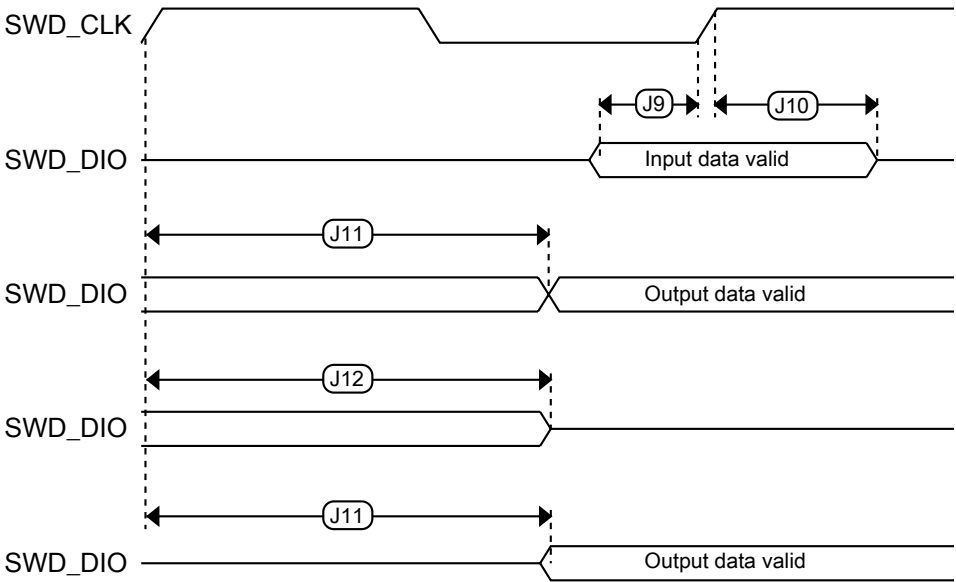


Figure 5. Serial wire data timing

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μ A	
	• 8 MHz (RANGE=01)	—	300	—	μ A	
	• 16 MHz	—	950	—	μ A	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μ A	
	• 4 MHz	—	400	—	μ A	
	• 8 MHz (RANGE=01)	—	500	—	μ A	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)					

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		—	0	—	k Ω	
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

- V_{DD} =3.3 V, Temperature =25 °C
- See crystal or resonator manufacturer's recommendation
- C_x, C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
- When low power mode is selected, R_F is integrated and must not be attached externally.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versall}}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
$t_{pgm\text{chk}}$	Program Check execution time	—	—	45	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
$t_{er\text{sscr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rd\text{once}}$	Read Once execution time	—	—	25	μs	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	—	μs	—
$t_{er\text{sall}}$	Erase All Blocks execution time	—	88	650	ms	2
$t_{vfy\text{key}}$	Verify Backdoor Access Key execution time	—	—	30	μs	1

Peripheral operating requirements and behaviors

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	—
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	—
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
DNL	Differential non-linearity	12-bit modes <12-bit modes	—	±0.7	–1.1 to +1.9	LSB ⁴	5
			—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	12-bit modes <12-bit modes	—	±1.0	–2.7 to +1.9	LSB ⁴	5
			—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	12-bit modes <12-bit modes	—	–4	–5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
			—	–1.4	–1.8		
E_Q	Quantization error	16-bit modes ≤13-bit modes	—	–1 to 0	—	LSB ⁴	
			—	—	±0.5		
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	–94 –85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{IN} \times R_{AS}$			mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)

Table continues on the next page...

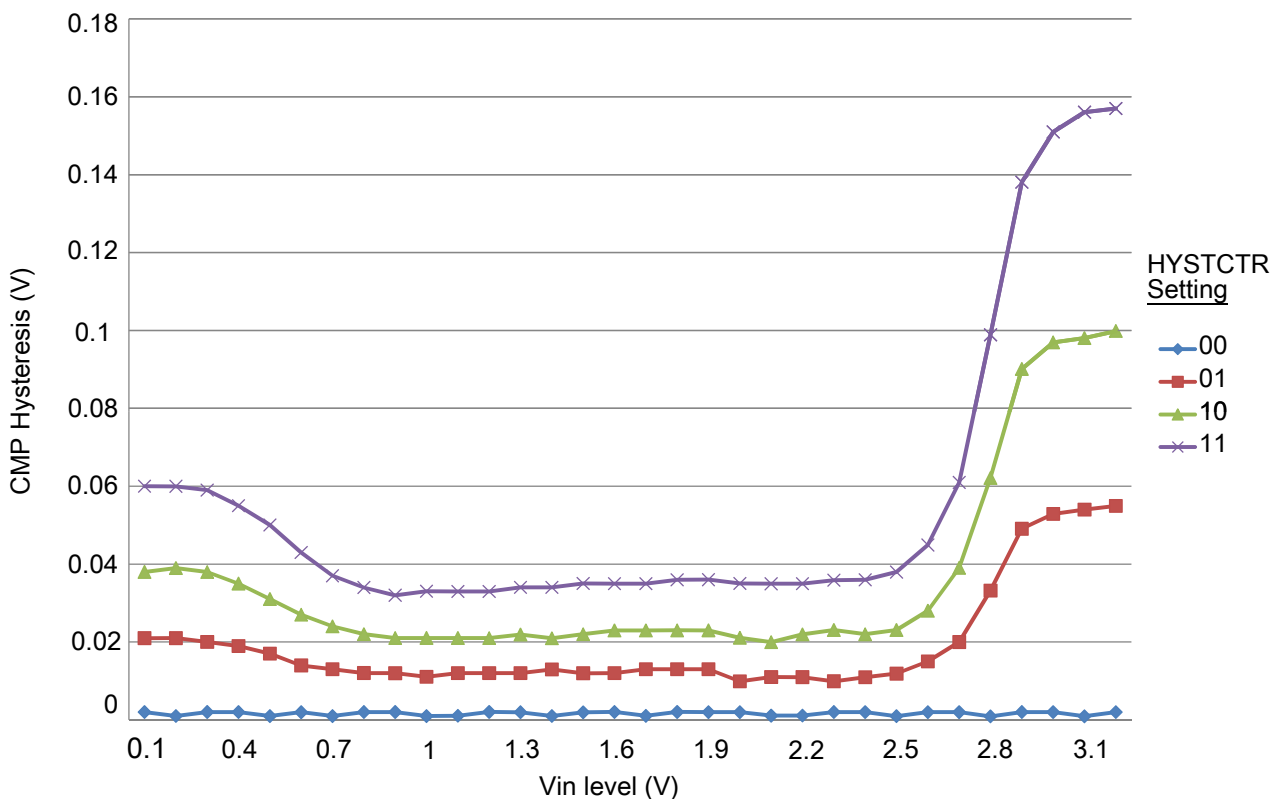


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

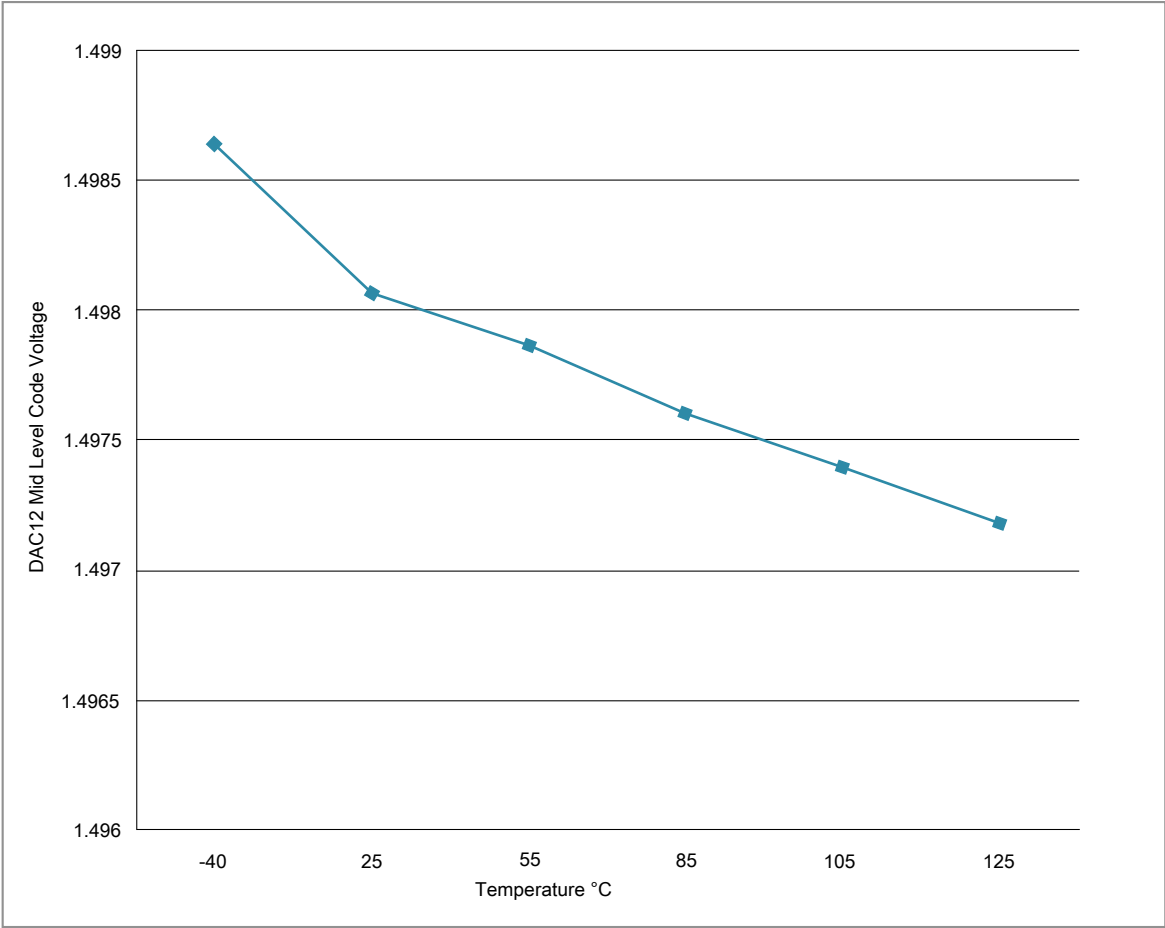


Figure 12. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 30. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$

Table 31. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

Table 33. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{periph} - 25$	ns	—
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output	—	36	ns	—

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

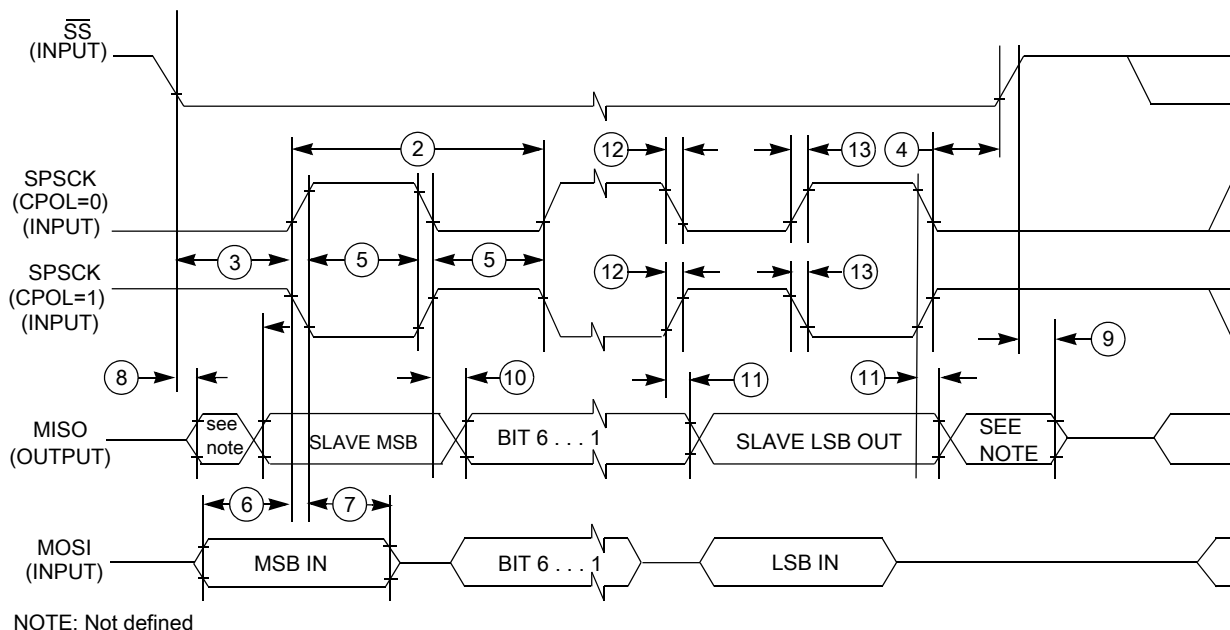


Figure 15. SPI slave mode timing (CPHA = 0)

Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	—	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	—	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	—	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

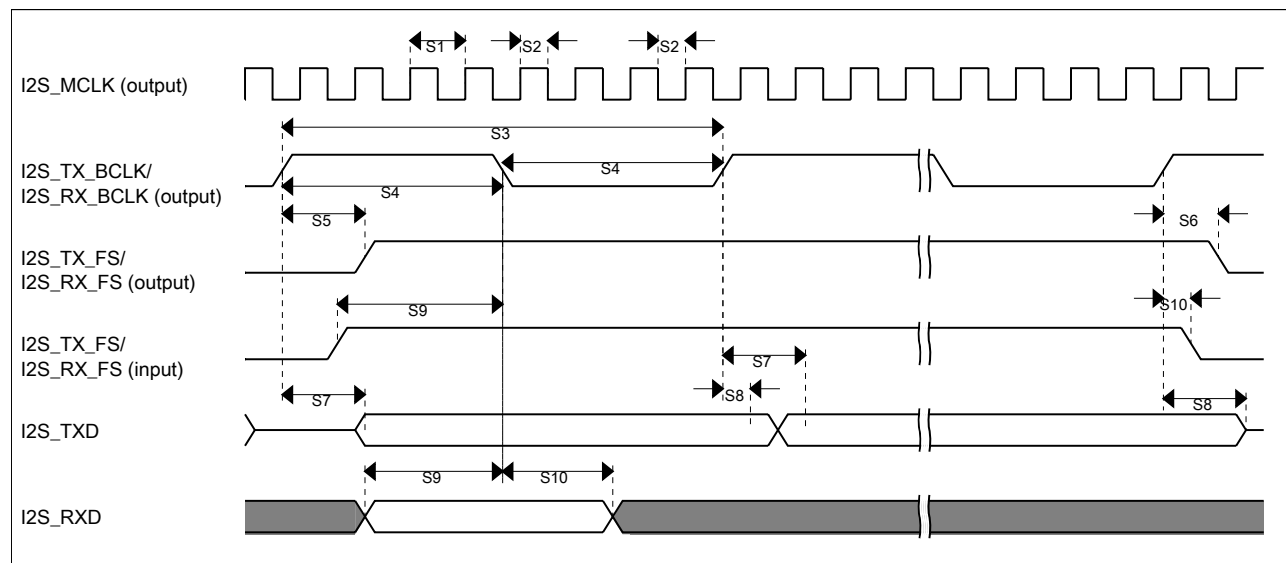


Figure 20. I2S/SAI timing — master modes

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
31	23	16	VSS	VSS	VSS							
32	24	17	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			
33	25	18	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	26	19	PTA20	RESET_b		PTA20						RESET_b
35	27	20	PTB0/ LLWU_P5	ADC0_SE8/ TSIO_CH0	ADC0_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
36	28	21	PTB1	ADC0_SE9/ TSIO_CH6	ADC0_SE9/ TSIO_CH6	PTB1	I2C0_SDA	TPM1_CH1				
37	29	—	PTB2	ADC0_SE12/ TSIO_CH7	ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	TPM2_CH0				
38	30	—	PTB3	ADC0_SE13/ TSIO_CH8	ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	TPM2_CH1				
39	31	—	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		
40	32	—	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	—	PTB18	TSIO_CH11	TSIO_CH11	PTB18		TPM2_CH0	I2S0_TX_BCLK			
42	—	—	PTB19	TSIO_CH12	TSIO_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			
43	33	—	PTC0	ADC0_SE14/ TSIO_CH13	ADC0_SE14/ TSIO_CH13	PTC0		EXTRG_IN		CMP0_OUT	I2S0_TXD0	
44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15/ TSIO_CH14	ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	
45	35	23	PTC2	ADC0_SE11/ TSIO_CH15	ADC0_SE11/ TSIO_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	
46	36	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	
47	—	—	VSS	VSS	VSS							
48	—	—	VDD	VDD	VDD							
49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		
50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	
51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO		I2S0_RX_FS	SPI0_MOSI		
53	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
54	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
55	—	—	PTC10	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS			
56	—	—	PTC11	DISABLED		PTC11	I2C1_SDA		I2S0_RXD0			
57	41	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0			
58	42	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			
59	43	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

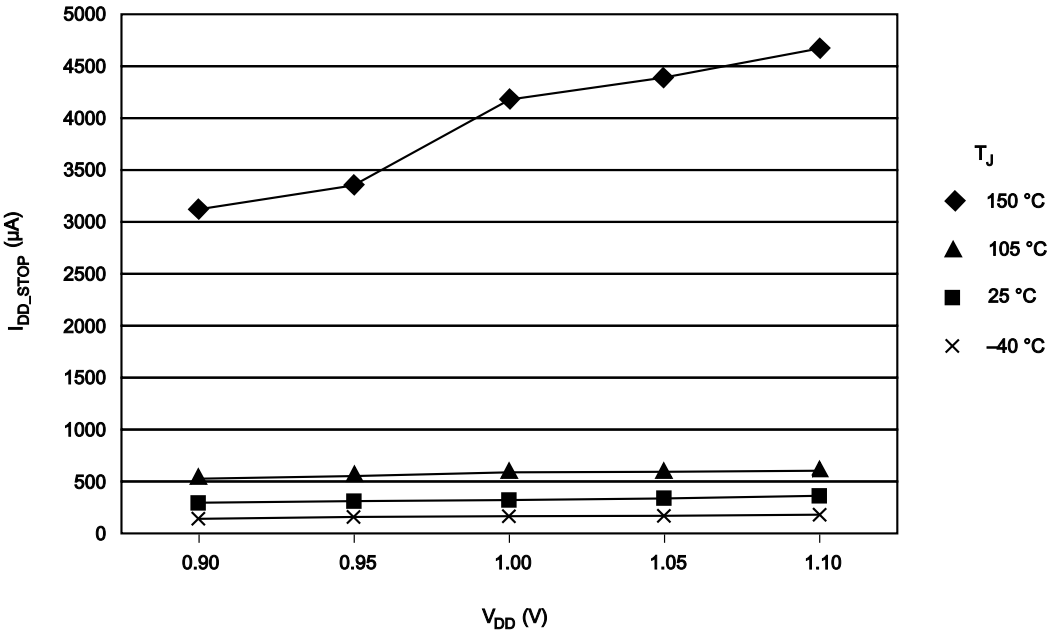
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 40. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 41. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	Updated the front page and restructured the chapters
4	5/2014	- Updated Power consumption operating behaviors - Updated Definition: Operating behavior
5	08/2014	- Updated related source in the front page - Updated Power consumption operating behaviors