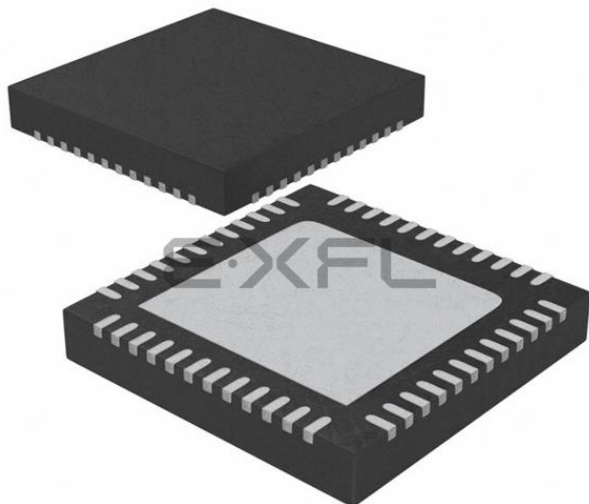




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, TSI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl16z32vft4r

Ordering Information ¹

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKL16Z32VFM4	32	4	28
MKL16Z64VFM4	64	8	28
MKL16Z128VFM4	128	16	28
MKL16Z32VFT4	32	4	40
MKL16Z64VFT4	64	8	40
MKL16Z128VFT4	128	16	40
MKL16Z32VLH4	32	4	54
MKL16Z64VLH4	64	8	54
MKL16Z128VLH4	128	16	54

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL16P64M48SF5RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL16P64M48SF5 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN15J ²
Package drawing	Package dimensions are provided in package drawings.	QFN 32-pin: 98ASA00473D ¹ QFN 48-pin: 98ASA00466D ¹ LQFP 64-pin: 98ASS23234W ¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term with the “x” replaced by the revision of the device you are using.

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	−55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	−2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	−500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	−100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1H}	Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V_{LVW1L}	Low-voltage warning thresholds — low range Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	1
V_{LVW2L}	Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except RESET_b) 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -2.5 mA	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
V_{OH}	Output high voltage — High drive pad (except RESET_b) 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10 mA	$V_{DD} - 0.5$ $V_{DD} - 0.5$	— —	V V	1, 2
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	— —	0.5 0.5	V V	1

Table continues on the next page...

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 8\text{ MHz}$ (crystal), $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes ¹				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock ²	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz

Table continues on the next page...

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V _{DD} and 25 °C		—	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTTRIM] and C4[SCFTRIM]		—	± 0.3	± 0.6	%f _{dco}	1
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 3	%f _{dco}	1, 2
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C		—	± 0.4	± 1.5	%f _{dco}	1, 2
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V _{DD} and 25 °C		—	4	—	MHz	
Δf _{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V _{DD} and 25 °C		—	+1/-2	± 3	%f _{intf_ft}	2
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V _{DD} and 25 °C		3	—	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS = 00) 640 × f _{fill_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) 1280 × f _{fill_ref}	40	41.94	48	MHz	
f _{dco_t_DM32}	DCO output frequency	Low range (DRS = 00)	—	23.99	—	MHz	5, 6

Table continues on the next page...

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versall}}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
$t_{pgm\text{chk}}$	Program Check execution time	—	—	45	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
$t_{er\text{sscr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rd\text{once}}$	Read Once execution time	—	—	25	μs	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	—	μs	—
$t_{er\text{sall}}$	Erase All Blocks execution time	—	88	650	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

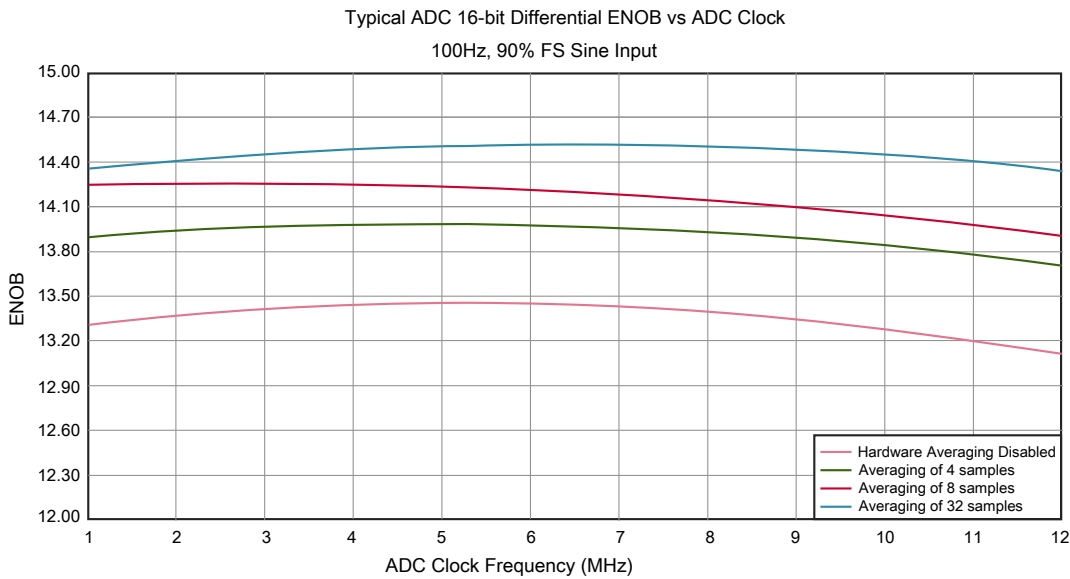


Figure 7. Typical ENOB vs. ADC_CLK for 16-bit differential mode

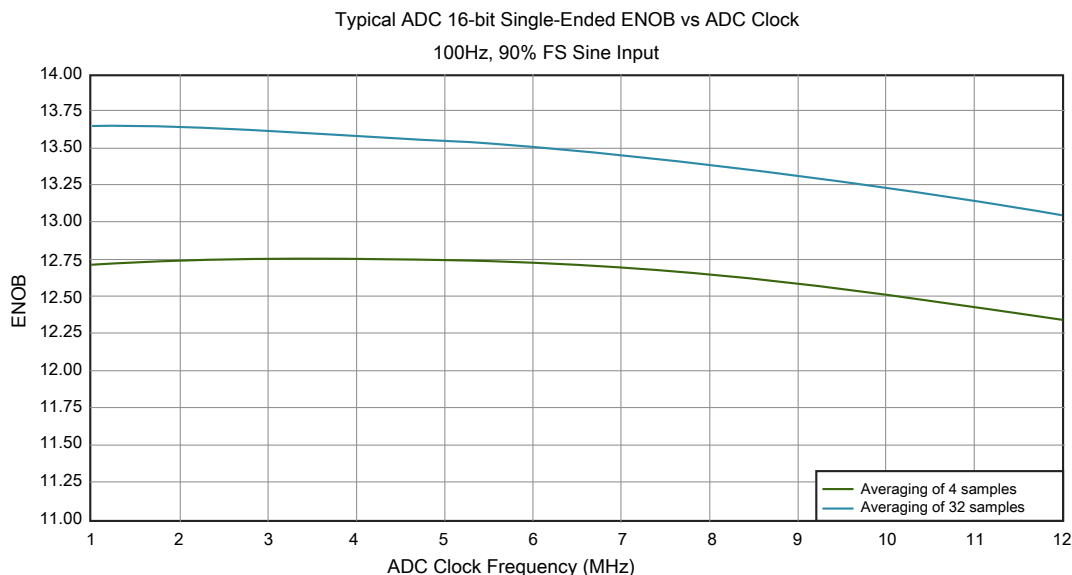


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s

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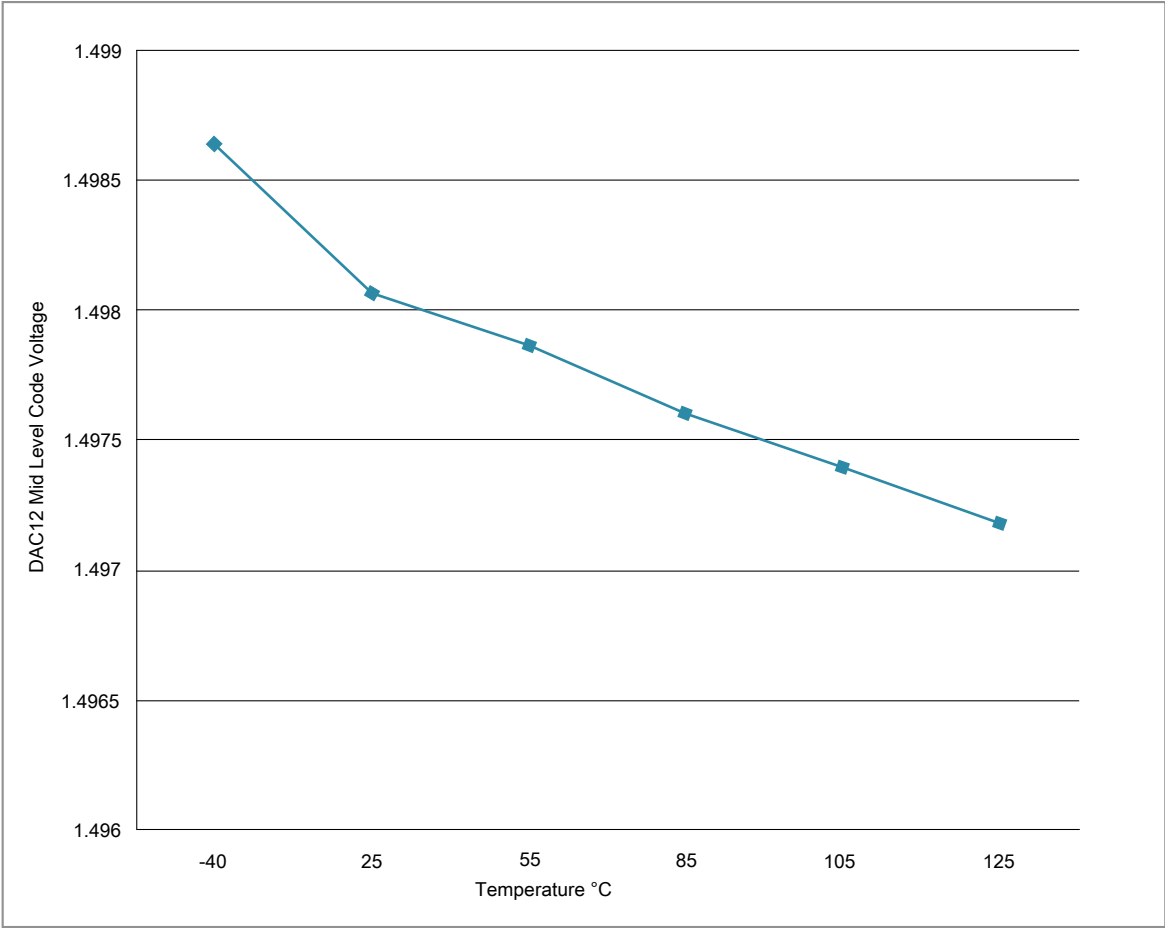


Figure 12. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 30. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

- For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
- $t_{periph} = 1/f_{periph}$

Table 31. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

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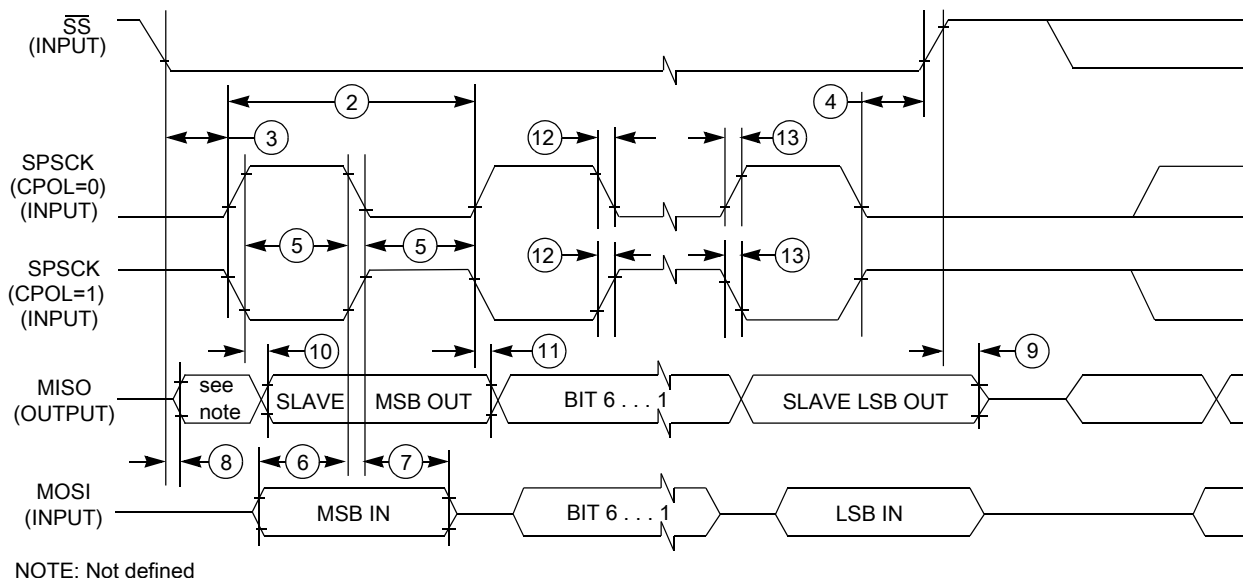


Figure 16. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 34. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD; STA}$	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU; STA}$	4.7	—	0.6	—	μs
Data hold time for I ² C bus devices	$t_{HD; DAT}$	0 ²	3.45 ³	0 ⁴	0.9 ²	μs
Data set-up time	$t_{SU; DAT}$	250 ⁵	—	100 ^{3, 6}	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	$20 + 0.1C_b$ ⁷	300	ns
Fall time of SDA and SCL signals	t_f	—	300	$20 + 0.1C_b$ ⁶	300	ns
Set-up time for STOP condition	$t_{SU; STO}$	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins (see [Voltage and current operating behaviors](#)) or when using the Normal drive pins and $V_{DD} \geq 2.7 V$

Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	—	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	—	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	—	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

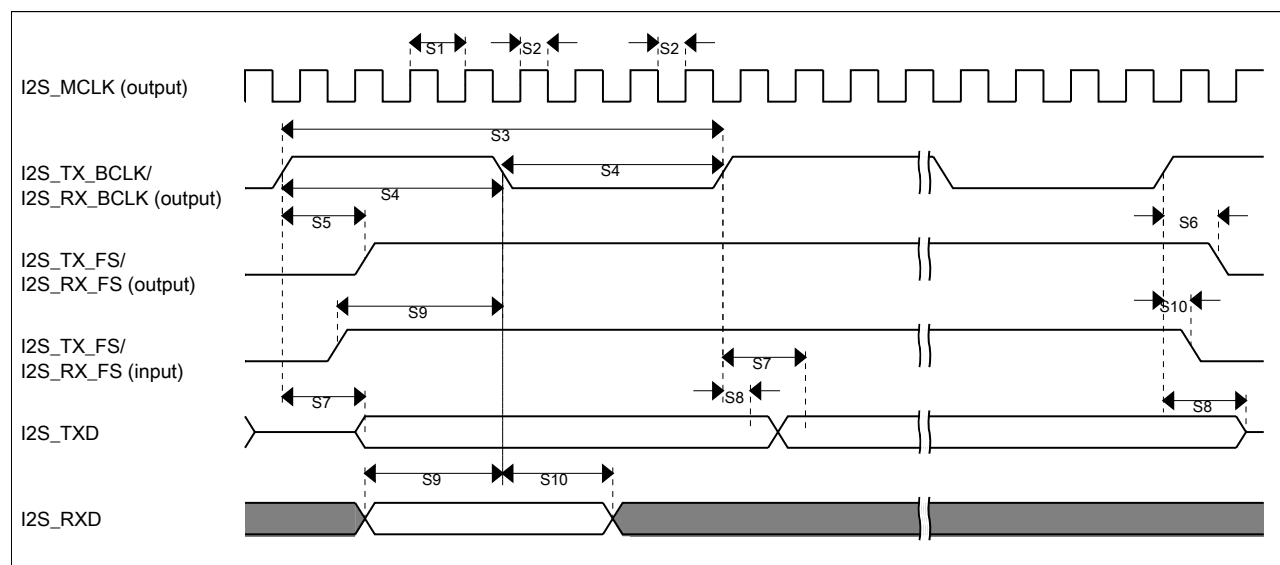


Figure 20. I2S/SAI timing — master modes

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	—	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	—	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	—	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

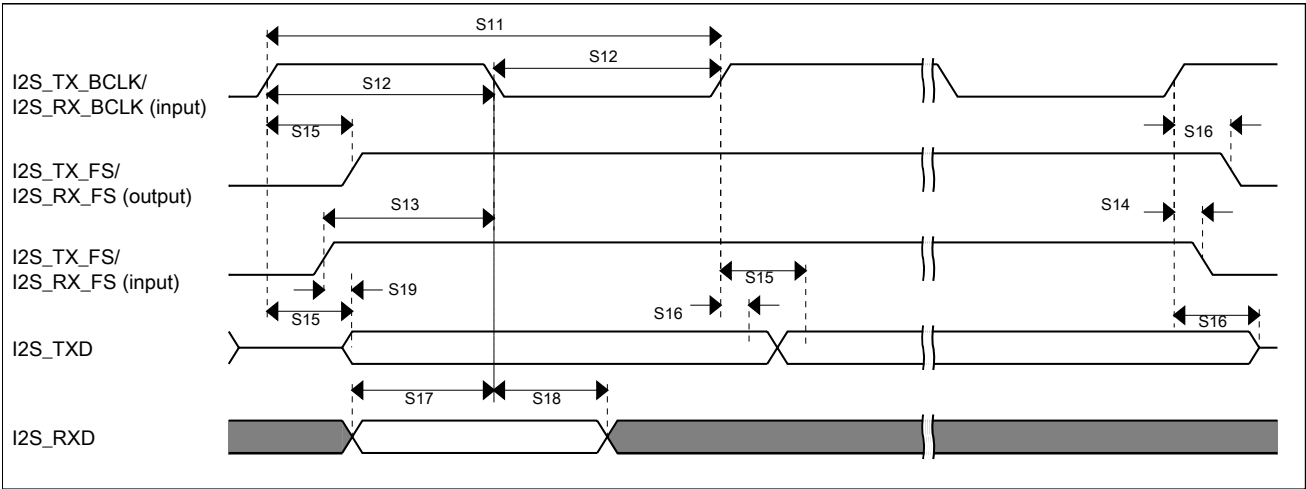


Figure 21. I2S/SAI timing — slave modes

3.9 Human-machine interfaces (HMI)

3.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA

Table continues on the next page...

Pinout

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	—	1	PTE0	DISABLED		PTE0	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	—	2	PTE1	DISABLED		PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	
3	1	—	VDD	VDD	VDD							
4	2	—	VSS	VSS	VSS							
5	3	3	PTE16	ADC0_DP1/ ADC0_SE1	ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			
6	4	4	PTE17	ADC0_DM1/ ADC0_SE5a	ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ALT3	
7	5	5	PTE18	ADC0_DP2/ ADC0_SE2	ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		
8	6	6	PTE19	ADC0_DM2/ ADC0_SE6a	ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI		
9	7	—	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			
10	8	—	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			
11	—	—	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
12	—	—	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			
13	9	7	VDDA	VDDA	VDDA							
14	10	—	VREFH	VREFH	VREFH							
15	11	—	VREFL	VREFL	VREFL							
16	12	8	VSSA	VSSA	VSSA							
17	13	—	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	14	9	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			
19	—	—	PTE31	DISABLED		PTE31		TPM0_CH4				
20	15	—	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	16	—	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	17	10	PTA0	SWD_CLK	TSI0_CH1	PTA0		TPM0_CH5				SWD_CLK
23	18	11	PTA1	DISABLED	TSI0_CH2	PTA1	UART0_RX	TPM2_CH0				
24	19	12	PTA2	DISABLED	TSI0_CH3	PTA2	UART0_TX	TPM2_CH1				
25	20	13	PTA3	SWD_DIO	TSI0_CH4	PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	21	14	PTA4	NMI_b	TSI0_CH5	PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	—	—	PTA5	DISABLED		PTA5		TPM0_CH2			I2S0_TX_BCLK	
28	—	—	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	
29	—	—	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
30	22	15	VDD	VDD	VDD							

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
31	23	16	VSS	VSS	VSS							
32	24	17	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			
33	25	18	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	26	19	PTA20	RESET_b		PTA20						RESET_b
35	27	20	PTB0/ LLWU_P5	ADC0_SE8/ TSIO_CH0	ADC0_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
36	28	21	PTB1	ADC0_SE9/ TSIO_CH6	ADC0_SE9/ TSIO_CH6	PTB1	I2C0_SDA	TPM1_CH1				
37	29	—	PTB2	ADC0_SE12/ TSIO_CH7	ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	TPM2_CH0				
38	30	—	PTB3	ADC0_SE13/ TSIO_CH8	ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	TPM2_CH1				
39	31	—	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		
40	32	—	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	—	PTB18	TSIO_CH11	TSIO_CH11	PTB18		TPM2_CH0	I2S0_TX_BCLK			
42	—	—	PTB19	TSIO_CH12	TSIO_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			
43	33	—	PTC0	ADC0_SE14/ TSIO_CH13	ADC0_SE14/ TSIO_CH13	PTC0		EXTRG_IN		CMP0_OUT	I2S0_TXD0	
44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15/ TSIO_CH14	ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	
45	35	23	PTC2	ADC0_SE11/ TSIO_CH15	ADC0_SE11/ TSIO_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	
46	36	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	
47	—	—	VSS	VSS	VSS							
48	—	—	VDD	VDD	VDD							
49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		
50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	
51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO		I2S0_RX_FS	SPI0_MOSI		
53	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
54	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
55	—	—	PTC10	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS			
56	—	—	PTC11	DISABLED		PTC11	I2C1_SDA		I2S0_RXD0			
57	41	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0			
58	42	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			
59	43	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
60	44	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		
61	45	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			
62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			
63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		
64	48	32	PTD7	DISABLED		PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		

5.2 KL16 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL16 Signal Multiplexing and Pin Assignments](#).

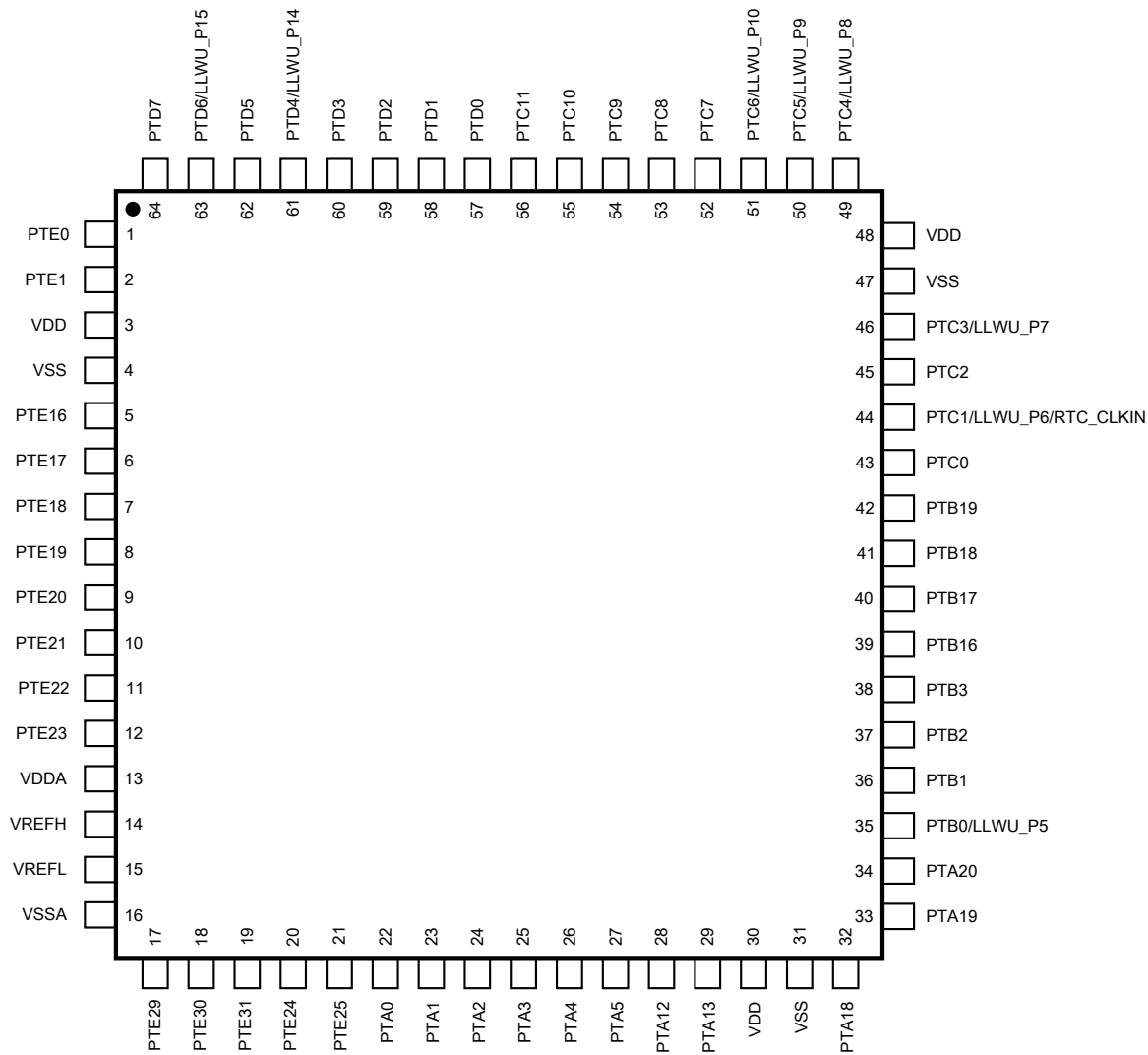


Figure 22. KL16 64-pin LQFP pinout diagram

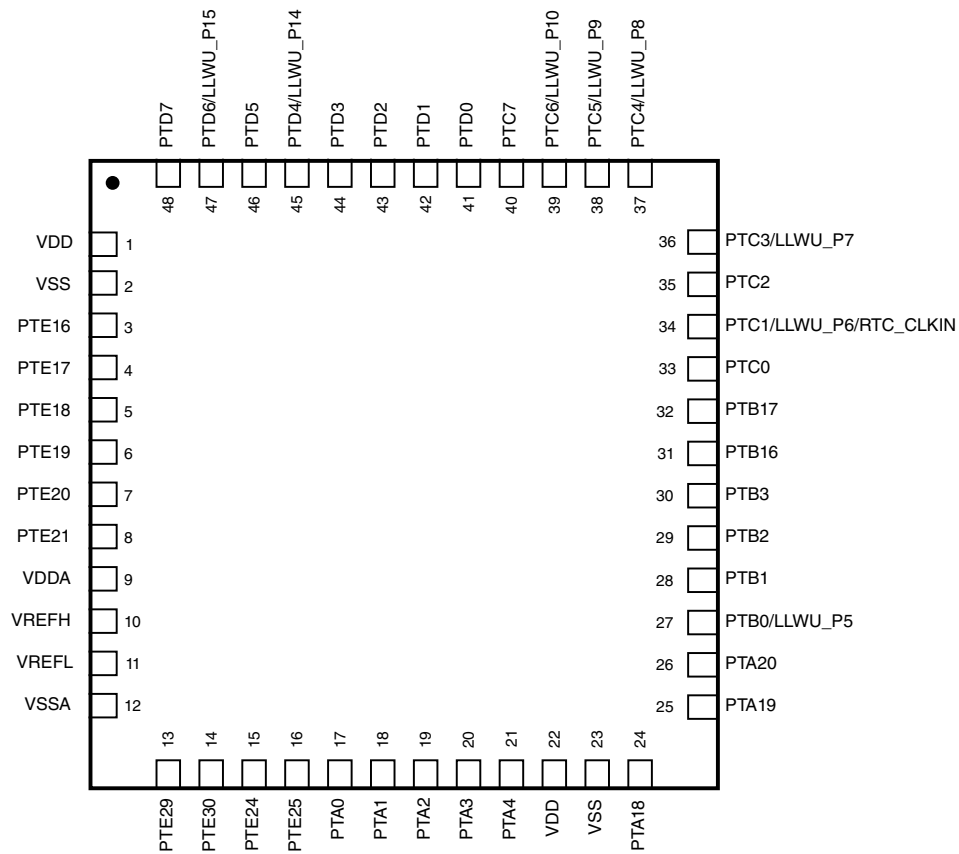


Figure 23. KL16 48-pin QFN pinout diagram

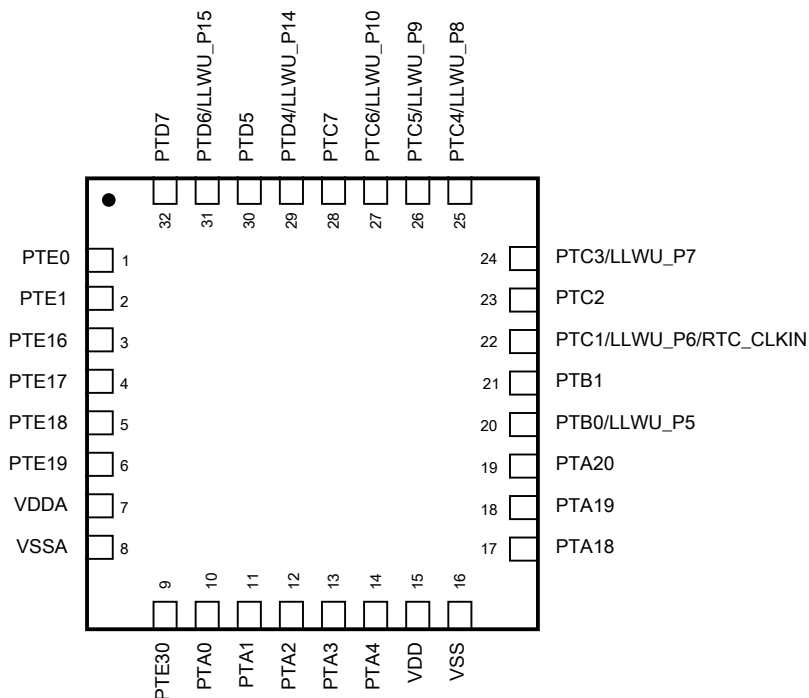


Figure 24. KL16 32-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PKL16 and MKL16

7 Part identification

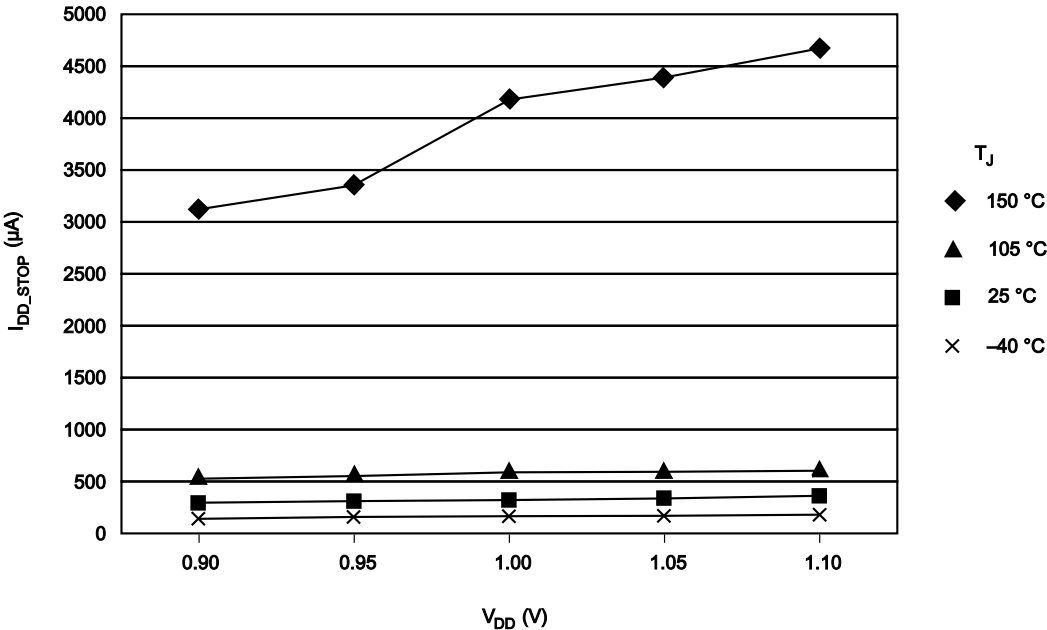
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):