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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	12
Voltage - Supply	9V ~ 16V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e622acdwb

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Die	Pin	Pin Name	Formal Name	Definition
MCU / Analog	44	(PTE1/RXD <- RXD)	LIN Transceiver Output	This pin is the LIN Transceiver output test pin. It internally connects the MCU PTE1/RXD pin with the Analog die LIN transceiver output pin RXD. Note: Do not connect in the application.
MCU	45 48	VSSA/VREFL VDDA/VREFH	ADC Supply and Reference Pins	These pins are the power supply and voltage reference pins for the analog-to-digital converter (ADC).
MCU	46 47	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	11	RST_A	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	12	IRQ_A	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	13	LIN	LIN Bus	This pin represents the single wire bus transmitter and receiver.
Analog	14	A0CST	Analog Input Trim Pin	This is the Analog Input Trim Pin for the A0 input. This is to connect a known fixed resistor value to trim the current source measurement.
Analog	15	A0	Analog Input Pin	This pin is an analog input port with selectable source values.
Analog	16 19 25 30	GND1 GND2 GND3 GND4	Power Ground Pins	These pins are device power ground connections.
Analog	29 26 20 17	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for DC motor drivers, or as high side and low side switches. Note: The HB3 and HB4 have a lower $R_{DS(ON)}$ then HB1 and HB2.
Analog	18 21 27 28 31 32 35	VSUP1 VSUP2 VSUP3 VSUP4 VSUP5 VSUP6 VSUP7	Power Supply Pins	These pins are device power supply pins.
Analog	22 23	EC ECR	EC Glass Pin EC Ballast Resistor Pin	These are the Electrochrome Circuitry Pins. The EC Pin has to be connected to the EC Glass and the ECR Pin has to be connected to the external ballast resistor.
Analog	24	TESTMODE	TESTMODE Input	Pin for test purpose only. In application, this pin needs to be tied GND.
Analog	34 35	HS1a HS1b	High Side HS1 Output	This output pin is a low $R_{DS(ON)}$ high side switch.
Analog	36 38	HS2 HS3	High Side HS2 Output High Side HS3 Output	These output pins are low $R_{DS(ON)}$ high side switches.
Analog	39	H0	Hall-effect Sensor / General Purpose Input	This pin provides an input for a Hall-effect sensor or general purpose input.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions(1) MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 5.5	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins except VDD, VSS, PTA0:PTA4 PTA0:PTA4	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 17)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
ESD Voltage Human Body Model(2) H0 pin Human Body Model(2) all other pins Machine Model(2) Charge Device Model(2)	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3}	 ±1000 ±2000 ±200 ±750	V

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Ambient Temperature[3]	T_A	-40 to 85	°C
Operating Junction Temperature[4]	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C

Notes

3. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
4. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pull-up Resistor to VSUP	R_{PU}	20	30	47	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	20	—	µA
Output Current Shutdown Threshold	I_{BLIM}	100	230	280	mA
Output Current Shutdown Timing	I_{BLS}	5.0	–	40	µs
Leakage Current to GND					
V_{SUP} Disconnected, V_{BUS} at 18 V	I_{BUS}	–	1.0	10	µA
Recessive state, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V ≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}	$I_{BUS\text{-}PAS\text{-}REC}$	0.0	3.0	20	µA
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V	$I_{BUS\text{-}NOGND}$	-1.0	–	1.0	mA
LIN Receiver					VSUP
Receiver Threshold Dominant	V_{BUS_DOM}	–	–	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	–	–	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	–	–	0.175	
HIGH SIDE OUTPUT HS1					
Switch On Resistance					mΩ
T_J = 25 °C, I_{LOAD} = 1.0 A	$R_{DS(ON)\text{-}HS1}$	–	185	225	
Over-current Shutdown	I_{HSOC1}	6.0	–	9.0	A
Over-current Shutdown blanking time[14]	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio[15]	$CR_{RATIOHS1}$	0.84	1.2	1.56	V/A
V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2.0 A)					
High Side Switching Frequency[14]	f_{PWMHS}	–	–	25	kHz
High Side Freewheeling Diode Forward Voltage	V_{HSF}	–	0.9	–	V
T_J = 25 °C, I_{LOAD} = 1.0 A					
Leakage Current	I_{LeakHS}	–	<0.2	10	µA

Notes

14. This parameter is guaranteed by process monitoring but is not production tested.
15. This parameter is guaranteed only if correct trimming was applied.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

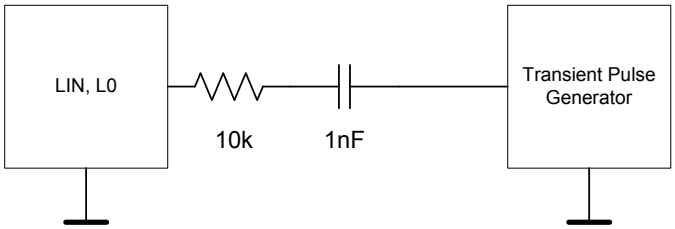
All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate[26], [27]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.0 V…18 V	D1	0.396	–	–	
Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.6 V…18 V	D2	–	–	0.581	
Driver Characteristics for Slow Slew Rate[26], [28]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.0 V…18 V	D3	0.417	–	–	
Duty Cycle4: D4 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.6 V…18 V	D4	–	–	0.590	
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	20	—	V/µs
Receiver Characteristics and Wake-up Timings					
Receiver Dominant Propagation Delay[29]	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay[29]	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	t_{PROPWL}	30	50	150	µs
Bus Wake-up Event Reported [30]	t_{WAKE}	—	20	—	µs

Notes

26. V_{SUP} from 7.0 to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
27. See Figure 6, page 17.
28. See Figure 7, page 18.
29. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
30. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 9 and Figure 8, page 18. In Sleep mode, the V_{DD} rise time is strongly dependent upon the decoupling capacitor at the VDD pin.

TIMING DIAGRAMS



Note: Waveform in accordance to ISO7637 part 1, test pulses 1, 2, 3a and 3b.

Figure 4. Test Circuit for Transient Test Pulses

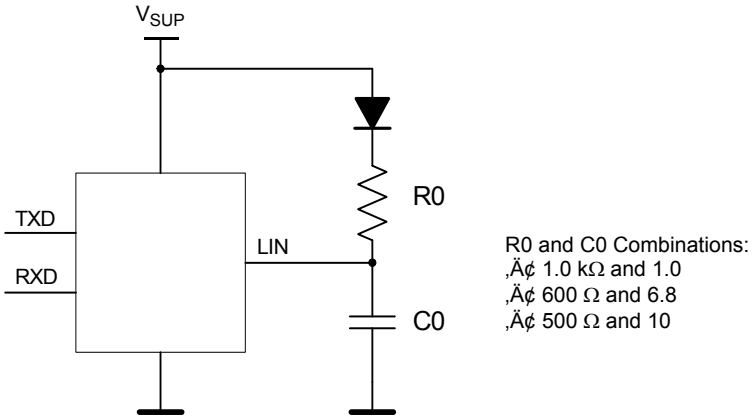


Figure 5. Test Circuit for LIN Timing Measurements

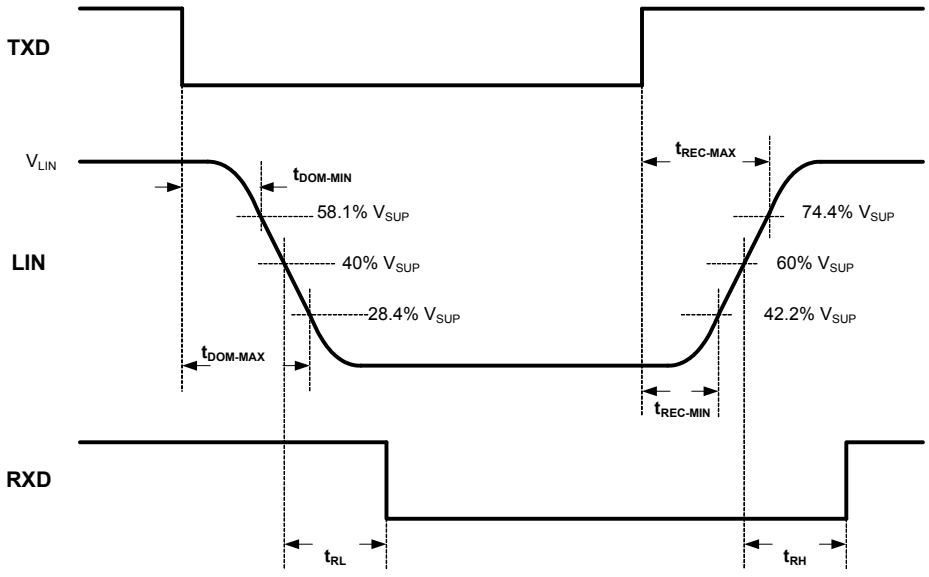
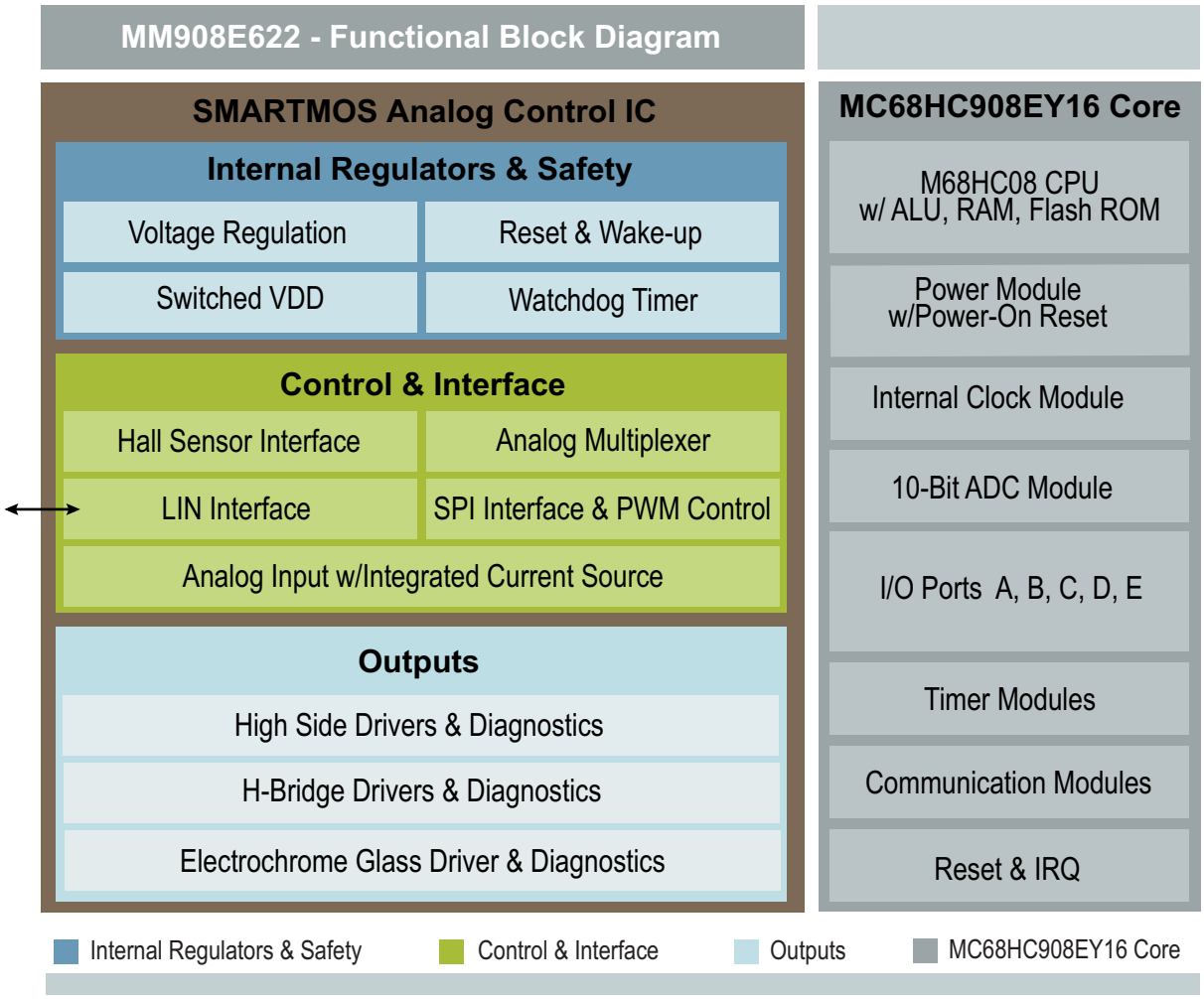


Figure 6. LIN Timing Measurements for Normal Slew Rate

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



SMARTMOS ANALOG CONTROL IC

INTERNAL REGULATORS & SAFETY:

VOLTAGE REGULATION

The voltage regulator circuitry provides the regulated voltage for the Analog IC, as well as the VDD/VSS rails for the core IC. The on-chip regulator consists of two elements, the main regulator, and the low voltage reset circuit. The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

SWITCHED VDD

This function provides a switchable +5.0 V V_{DD} rail for an external load.

WATCHDOG TIMER

The watchdog timer module generates a reset, in case of a watchdog timeout or wrong watchdog timer reset. A watchdog reset event will reset all registers in the SPI, excluding the RSR.

RESET, IRQ & WAKE-UP

There are several functions on the Analog IC that can generate a reset or wake-up signal to the core IC. There is a pin that is used to detect an external wake-up event. The Reset signal has many possible sources in the Analog IC circuitry. The IRQ function on the Analog IC will notify the core IC of pending system critical conditions.

up sources can be selected (maskable) which is not possible in Sleep mode.

Figure 12 show the procedure to enter the Stop mode and how the system wakes up.

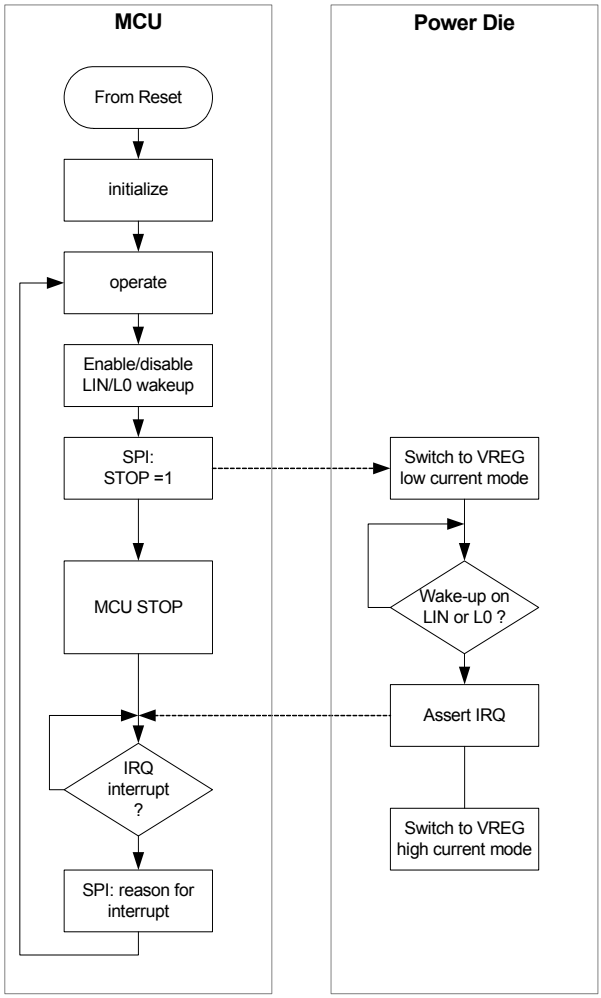


Figure 12. STOP mode Wake-up Procedure

Sleep Mode

In Sleep mode, the voltage regulator is turned off and the MCU is not supplied (V_{DD} = 0 V), the $\overline{RST\_A}$ pin also is pulled low.

To enter the Sleep mode, the Sleep bit in the System Control Register has to be set.

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0, and is not maskable. The wake-up behaves like a power on reset. The wake-up / reset source can be evaluated by the L0WF and/or LINWF bits in the Reset Status Register.

Sleep mode has a lower current consumption than Stop mode, but requires a longer time to wake-up. The wake-up sources can not be selected (not maskable).

Figure 13 show the procedure to enter the Sleep mode and how a wake-up is performed.

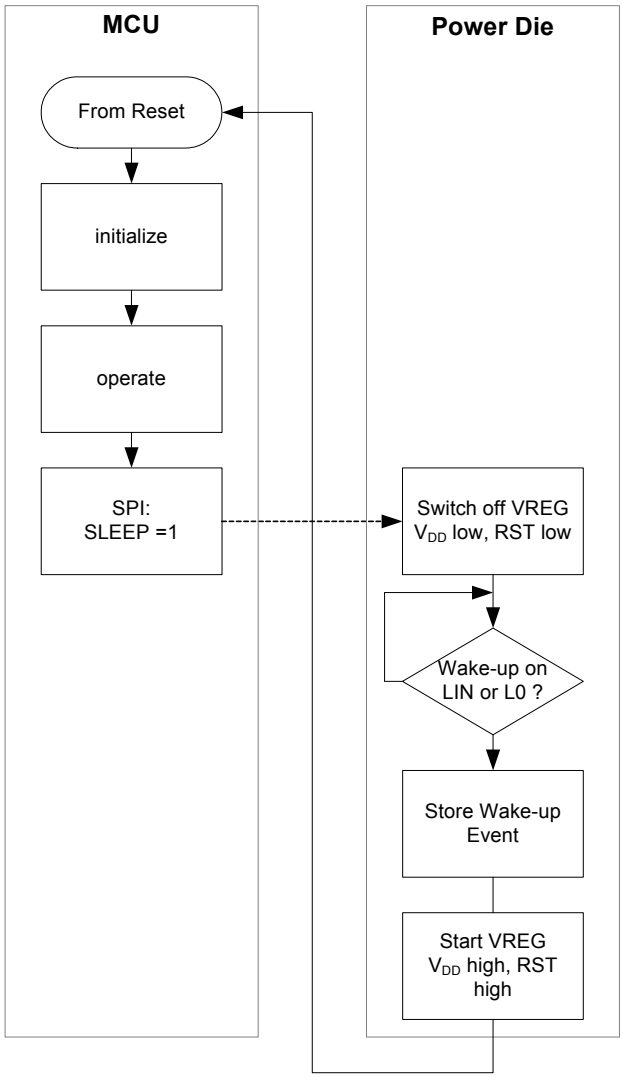


Figure 13. SLEEP Mode Wake-up Procedure

Table 6 summarized the Operating modes.

ANALOG DIE INPUTS/OUTPUTS

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with internal current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave mode. The fall time from dominant to recessive, and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20 kBit/s, as well as high baud rates for test and programming. The slew rate can be adapted with 2 bits SRS[1:0] in the System Control Register. The initial slew rate is optimized for 20 kBit/s.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled by setting the PSON bit in the System Control Register (SYSCTL).

If the transmitter works in the current limitation region, the LINCL bit in the System Status Register (SYSSTAT) is set and the LIN transceiver is disabled after a certain time.

For improved performance and safe behavior when the LIN bus shorts to Ground, or LIN bus leakage during low power mode, the internal pull-up resistor on the LIN pin is disconnected from VSUP and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

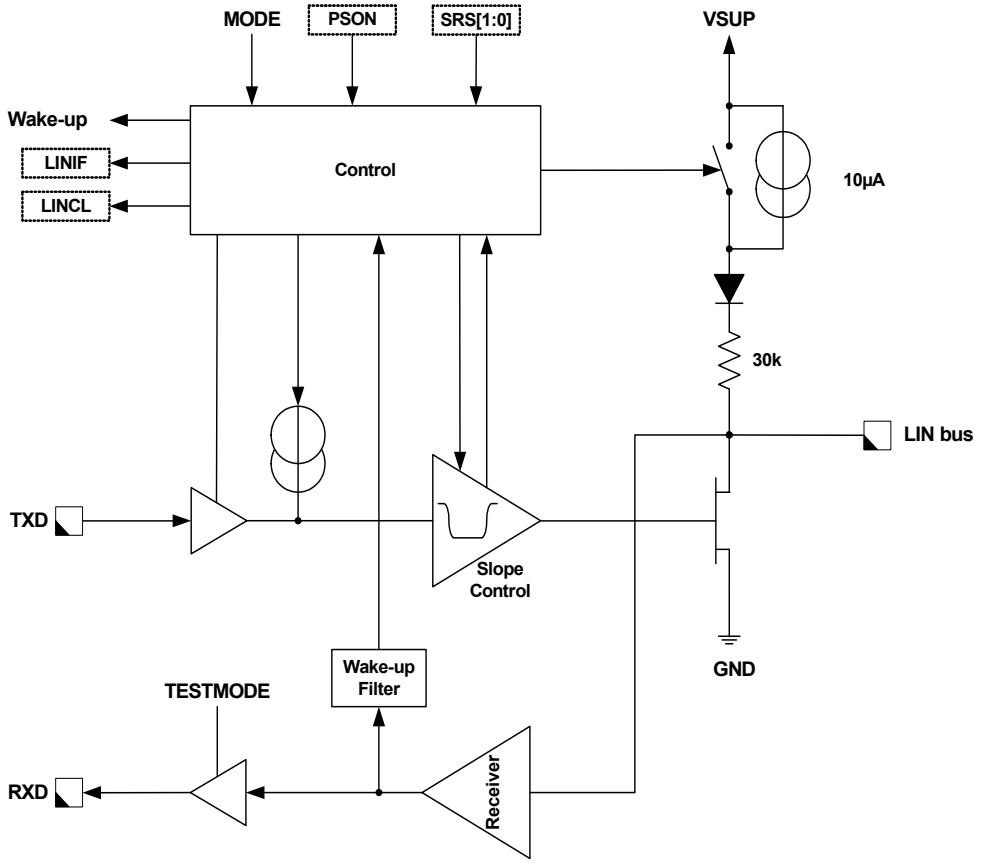
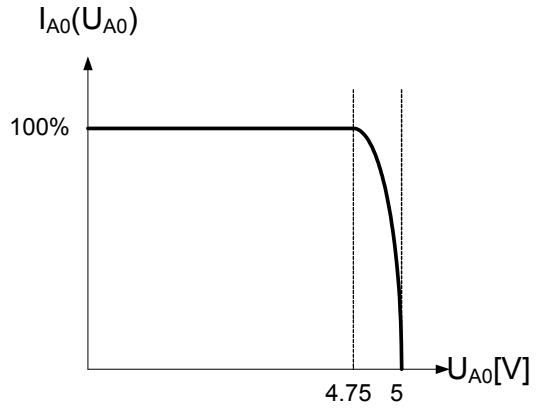


Figure 16. LIN Interface

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see Figure 2, page 2). When TXD is LOW, the LIN pin is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD pin has an internal pull-up current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.



To calibrate the current sources an extra pin (A0CST) is envisioned. On this pin, an accurate resistor can to be connected. Switching the current sources to this resistor allows the user to measure the current, and use the measured value for calculating the current on A0.

Analog Multiplexer / ADOUT Pin

The ADOUT pin is the analog output interface to the Analog-to-digital converter of the MCU. To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog die. This multiplexer has twelve different sources, which can be selected with the SS[3:0] bits in the A0MUCTL register.

Half-bridge (HB1:HB4) Current Recopy

The multiplexer is connected to the four current sense circuits on the low side FET of the half bridges. This sense circuits offers a voltage proportional to the current through the MOSFET. The resolution is depending on the CSA bit in the A0 and Multiplexer control register (A0MUCTL).

High Side (HS1:HS3) Current Recopy

The multiplexer is connected to the three high side switches. These sense circuits offer a voltage proportional to the current through the transistor.

Analog Input A0 and A0CST

A0 and A0CST are directly connected to the analog multiplexer. It offers the possibility to read analog values from the periphery.

Temperature Sensor

The analog die includes an on chip temperature sensor. This sensor offers a voltage which is proportional to the actual mean chip junction temperature.

VSUP Prescaler

The VSUP prescaler offers a possibility to measure the external supply voltage. The output of this voltage is V_{SUP} / $RATIO_{VSUP}$.

EC Output

The EC output is directly connected to the multiplexer to be able to read the actual voltage on the EC pin.

A0 and Multiplexer Control Register (A0MUCTL)

Register Name and Address: A0MUCTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read Write	CSON	CSSEL 1	CSSEL 0	CSA	SS3	SS2	SS1	SS0
Reset	0	0	0	0	0	0	0	0

CSON — Current Source on/off

This read/write bit enables the current source for the A0 or A0CST inputs. Reset clears CSON bit.

1 = Current Source enabled
0 = Current Source disabled

CSSEL[1:0] — Current Source Select Bits

These read/write bits select the current source values for A0 or A0CST input. Reset clears CSSEL[1:0] bits.

Table 7. A0 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	40 µA
0	1	120 µA
1	0	320 µA
1	1	800 µA

CSA — H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-bridges HB1:HB4 current recopy. Reset clears the CSA bit.

1 = low current sense amplification
0 = high current sense amplification

SS[3:0] — Analog Source Input Select Bits

These read/write bits selects the analog input source for the ADOUT pin. Reset clears the SS[3:0] bits

Table 8. Analog Multiplexer Configuration Bits

SS3	SS2	SS1	SS0	Channel
0	0	0	0	current recopy HB1
0	0	0	1	current recopy HB2
0	0	1	0	current recopy HB3
0	0	1	1	current recopy HB4
0	1	0	0	current recopy HS1

CRM — Current Recirculation Mode bit

This read/write bit selects the recirculation mode during PWM. Reset clears the CRM bit.

1 = recirculation via switched on low side MOSFET
0 = recirculation via low side free wheeling diode

HBxOCF — Half-bridges Over-current Flag Bit

This read/write bit indicates that an over-current condition on either the LS or the HS FET on HBx has occurred.

Clear HBxOCF and enable Half-bridge by writing a logic [1] to HBxOCF. Writing a logic [0] to HBxOCF has no effect. Reset clears the HBxOCF bit.

1 = over-current condition on HBx occurred
0 = no over-current condition on HBx

High Side Drivers

The high side outputs are low resistive high side switches targeted for driving lamps. The high sides are protected against over-temperature, over-current and over-voltage/ under-voltage.

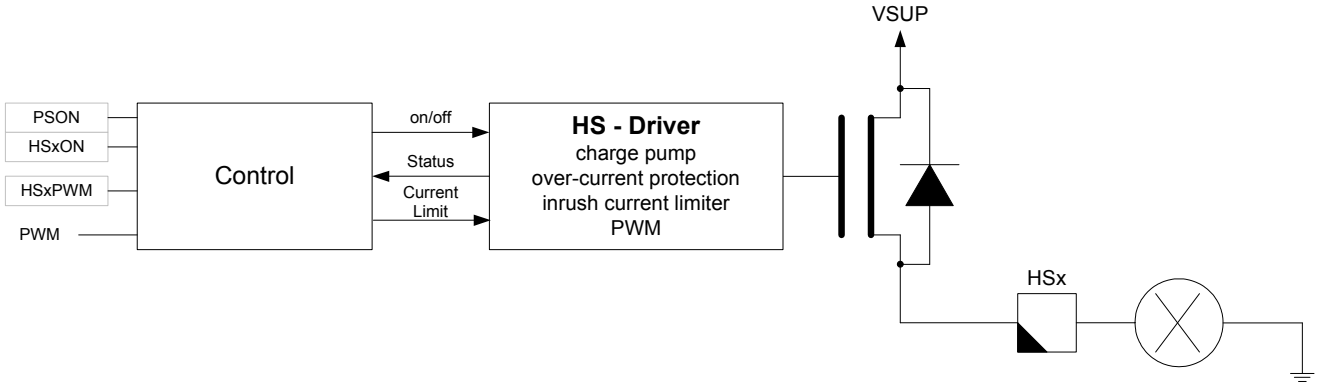


Figure 23. HS Circuitry

HIGH SIDE OPERATING MODES

The high sides outputs are enabled if the PSON bit in the System Control Register (SYSCTL) is set.

Each high side output is permanently switched on, if the HSxON bit in the High Side Output Register (HSOUT) is set.

PWM control of the output is enabled, if the HSxPWM bit High Side Output Register (HSOUT) is set. In this operating mode, the high side MOSFET is on, if the input PWM signal (PWM pin) is high.

Table shows the behavior of the high side MOSFETs depending on the HSONx and PWMHSx bits.

HBF— HB1:4 Failure Bit

This read only bit is set if a fail condition on one of the half-bridge outputs is present.

1 = HB1:4 pin over-current fail
0 = HB1:4 normal operating

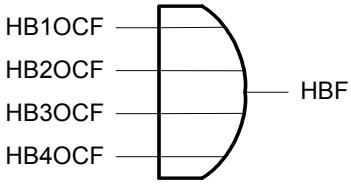


Figure 28. HBF Flag Generation

ECF— EC pin Failure Bit

This read only bit is set if a fail condition on the electrochrome output is present

1 = EC pin fail
0 = EC normal operating

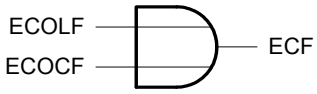


Figure 29. ECF Flag Generation

WINDOW WATCHDOG

The window watchdog is to supervise the device and to recover from (e.g. code runaways) or similar conditions.

The use of a window watchdog adds additional safety as the watchdog clear has not only to occur, but to be done at a certain time frame / window.

Normal Mode

The window watchdog function is only available in Normal mode, and is halted in Stop and Sleep mode. Upon setting the WDRE bit, the watchdog functionality is activated. Once this function is enabled, it is not possible to disable it via software. Reset clears the WDRE bit.

To prevent a Watchdog reset, the Watchdog timer has to be cleared in the Window Open frame. This is done by writing a logic “1” to the WDRST bit in the Watchdog Control register (WDCTL). The actual reset of the watchdog counter occurs at the end of the corresponding SPI transmission, with the rising edge of the $\overline{SS}$ signal.

If the watchdog is enabled, it will generate a system reset when the timer has reached its end value, or if a watchdog reset (WDRST) has occurred in the closed window.

The watchdog period can be selected with 2 bits in the WDCTL, in order to get 10 ms, 20 ms, 40 ms, and 80 ms periods.

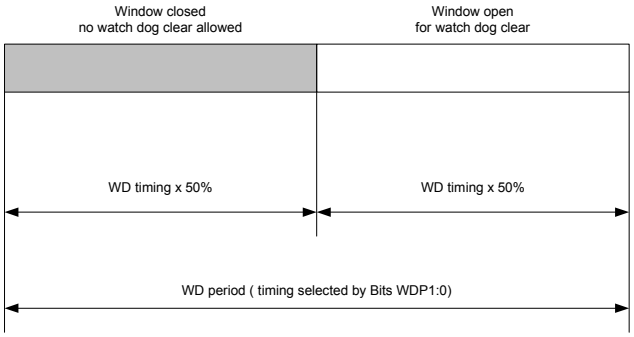


Figure 30. Window Watchdog Period

Stop Mode

Operations of the watchdog function is ceased in stop mode (counter/oscillator stopped). After a wake-up, the watchdog timer **is automatically cleared,** in order to give the MCU the full time to reset the watchdog.

Sleep Mode

Operations of the watchdog function are halted in sleep mode. Due to the main voltage regulator asserting an LVR reset, the Watchdog functionality is disabled, and the WDRE bit is cleared as soon as sleep mode is entered. To reenable this function bit WDRE has to be set after wake-up.

Watchdog Control Register (WDCTL)

Register Name and Address: WDCTL - $0B

	Bit7	6	5	4	3	2	1	Bit0
Read	WDRE	WDP1	WDP0	0	0	0	0	0
Write								WDRST
Reset	0	0	0	0	0	0	0	0

WDRE - Watchdog Reset Enable Bit

This read/write (write once) bit activates the watchdog The WDRE can only be set and can’t be cleared by software. Reset clears the WDRE bit.

1 = Watchdog enabled
0 = Watchdog disabled

WDP1:0 - Watchdog Period Select Bits

This read/write bit select the clock rate of the Watchdog. Reset clears the WDP1:0 bits.

Table 12. Watchdog Period Selection Bits

WDP1	WDP0	Mode
0	0	80 ms window watchdog period
0	1	40 ms window watchdog period

- Register read data is internally latched into the SPI, at the time when the parity bit is transferred
- $\overline{SS}$ high will force MISO to a high-impedance

Master Address Byte

A4 - A0

includes the address of the desired register.

R/$\overline{W}$

includes the information if it is a read or a write operation.

- If R/$\overline{W}$ = 1 (read operation), second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0 (write operation), master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* registers on rising edge of $\overline{SS}$.

Parity P

completes the total number of 1 bits of (R/W,A[4-0]) to an even number. e.g. (R/W,A[4-0]) = 100001 -> P0 = 0.

The parity bit is only evaluated during write operations and ignored for read operations.

Bit X

not used

Master Data Byte

This byte includes data to be written or no valid data during a read operation.

Slave Status Byte

This byte always includes the contents of the system status register ($0C), independent if it is a write or read operation, or which register was selected.

Slave Data Byte

This byte includes the contents of selected register, during write operation in includes the register content prior to write operation.

SPI REGISTER OVERVIEW

Table 13 **SUMMARIZES THE SPI REGISTER ADDRESSES AND THE BIT NAMES OF EACH REGISTER.**

Table 13. SPI Register Overview

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$00	System Control (SYSCTL)	R	PSON	0	0	HTIS1	HTIS0	VIS	SRS1	SRS0
		W		STOP	SLEEP					
$01	Half-bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	High Side Output (HSOUT)	R	HVDDON	0	HS3PWM	HS2PWM	HS1PWM	HS3ON	HS2ON	HS1ON
		W								
$03	Half-bridge Status and Control (HBSCTL)	R	CRM	0	0	0	HB4OCF	HB3OCF	HB2OCF	HB1OCF
		W								
$04	High Side Status and Control (HSSCTL)	R	HVDDOCF	0	0	0	0	HS3OCF	HS2OCF	HS1OCF
		W								
$05	EC Status and Control (ECSCTL)	R	ECON	ECOLT	ECRON	0	0	0	ECOCF	ECOLF
		W								
$06	EC Digital to Analog Control (ECDACC)	R	0	0	ECDAC5	ECDAC4	ECDAC3	ECDAC2	ECDAC1	ECDAC0
		W								
$07	H0/L0 Status and Control (HLSCTL)	R	L0F	0	0	H0OCF	H0F	H0EN	H0PD	H0MS
		W								

Table 13. SPI Register Overview

$08	A0 and Multiplexer Control (A0MUCTL)	R	CSON	CSSEL1	CSSEL0	CSA	SS3	SS2	SS1	SS0
		W								
$09	Interrupt Mask (IMR)	R	L0IE	H0IE	LINIE	HTRD	HTIE	LVIE	HVIE	PSFIE
		W								
$0A	Interrupt Flag (IFR)	R	L0IF	H0IF	LINIF	0	HTIF	LVIF	HVIF	PSFIF
		W								
$0B	Watchdog Control (WDCTL)	R	WDRE	WDP1	WDP0	0	0	0	0	0
		W								WDRST
$0C	System Status (SYSSTAT)	R	LINCL	HTIF	VF	H0F	HVDDF	HSF	HBF	ECF
		W								
$0D	Reset Status (RSR)	R	POR	PINR	WDR	HTR	LVR	0	LINWF	L0WF
		W								
$0E	System Test (SYSTEST)	R	reserved							
		W								
$0F	System Trim 1 (SYSTRIM1)	R	HVDDT1	HVDDT0	reserved	reserved	itrim3	itrim2	itrim1	itrim0
		W								
$10	System Trim 2 (SYSTRIM2)	R	0	0	0	0	0	0	0	0
		W	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
$11	System Trim 3 (SYSTRIM3)	R	0	0	0	0	0	0	0	0
		W	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0

Factory TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E622, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” ($FF) state:

- $FD80:$FDDF Trim and Calibration Values
- $FFFE:$FFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values located in the flash memory is explained by the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller, without using any external components. The untrimmed frequency of the low frequency base clock (IBASE) will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate these dependencies, a ICG trim value is located at address $FDC2. After trimming, the ICG is in a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF), and stabilized (4.7 μF) V_{DD} = 5.0 V, $T_{AMBIENT}$~25°C), and will vary over temperature and voltage (V_{DD}), as indicated in the 68HC908EY16 datasheet.

To trim the ICG, this value has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to copied after every reset.

Watchdog Period Range Value (AWD Trim)

The window watchdog supervises device recovery (e.g. from code runaways).

The application software has to clear the watchdog within the open window. Due to the high variation of the watchdog period, and therefore the reduced width of the watchdog window, a value is stored at address $FDCF. This value classifies the watchdog period into 3 ranges (Range 0, 1, 2). It allows the application software to select one of three time intervals to clear the watchdog based on the stored value. The classification is done in a way that the application software can have up to ±19% variation of the of optimal clear interval, e.g. caused by ICG variation.

Effective Open Window

Having a variation in the watchdog period in conjunction with a 50% open window, results in an effective open window, which can be calculated by:

latest window open time: t_open = t_wd max / 2

earliest window closed time: t_closed = t_wd min

System Trim Register 3 (SYSTRIM3)

Register Name and Address: IFBHSTRIM - $11

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0
Reset	0	0	0	0	0	0	0	0

CRHBHC3:2 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC3:2 bits.

Table 20. Current Recopy Trim for HB3:4 (CSA=0)

CRHBHC3	CRHBHC2	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHS5:3 - Current Recopy HS2:3 Trim Bits

These write only bits are for trimming the current recopy of the high side HS2 and HS3. The provided trim values have to be copied into these bits after every reset. Reset clears the CRHS5:3 bits.

Table 21. Current Recopy Trim for HS2:3

CRHS5	CRHS4	CRHS3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHS2:0 - Current Recopy HS1 Trim Bits

These write only bits are for trimming the current recopy of the high side HS1. The provided Trim values have to be copied into these bits after every reset. Reset clears the CRHS2:0 bits.

Table 22. Current Recopy Trim for HS1

CRHS2	CRHS1	CRHS0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

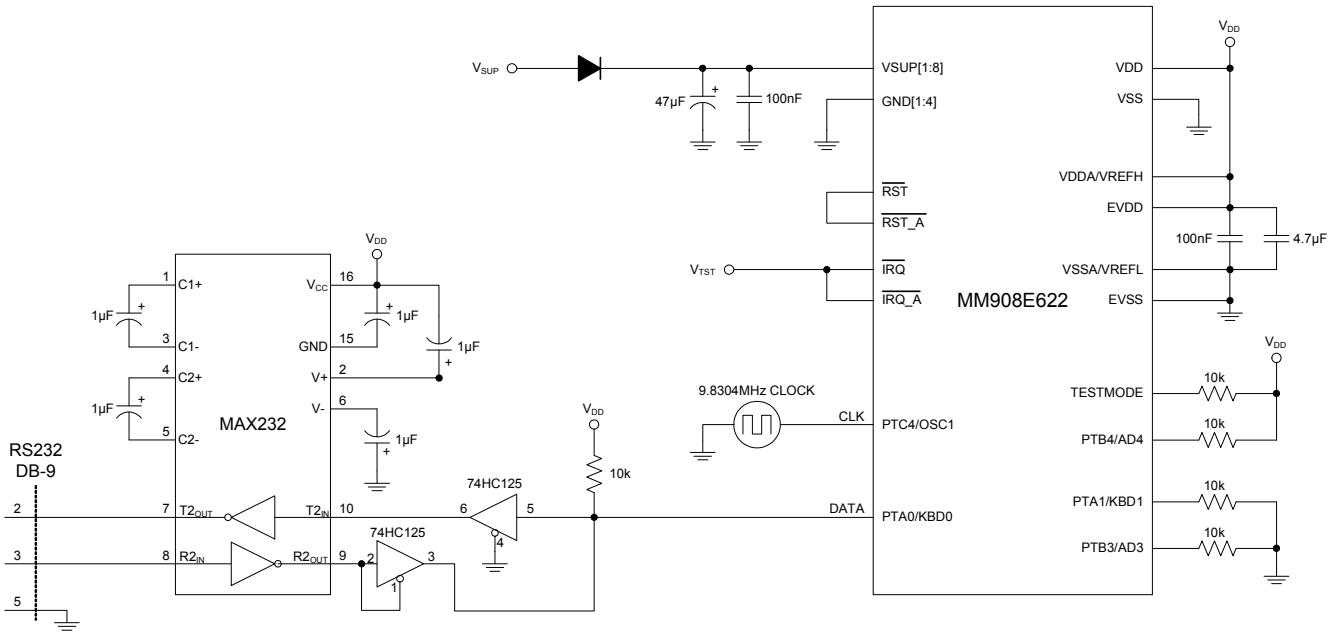


Figure 33. Normal Monitor Mode Circuit

Table 23 summarizes the possible configurations and the necessary setups.

Table 23. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	TEST MODE	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Time-out	Communication Speed		
					PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	1	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	1	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND								ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	0	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

34. PTA0 must have a pullup resistor to V_{DD} in monitor mode
35. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1
36. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
37. X = don't care
38. V_{TST} is a high voltage V_{DD} + 3.5 V ≤ V_{TST} ≤ V_{DD} + 4.5 V

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale web site www.freescale.com.

VSUP Pins (VSUP[1:8])

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

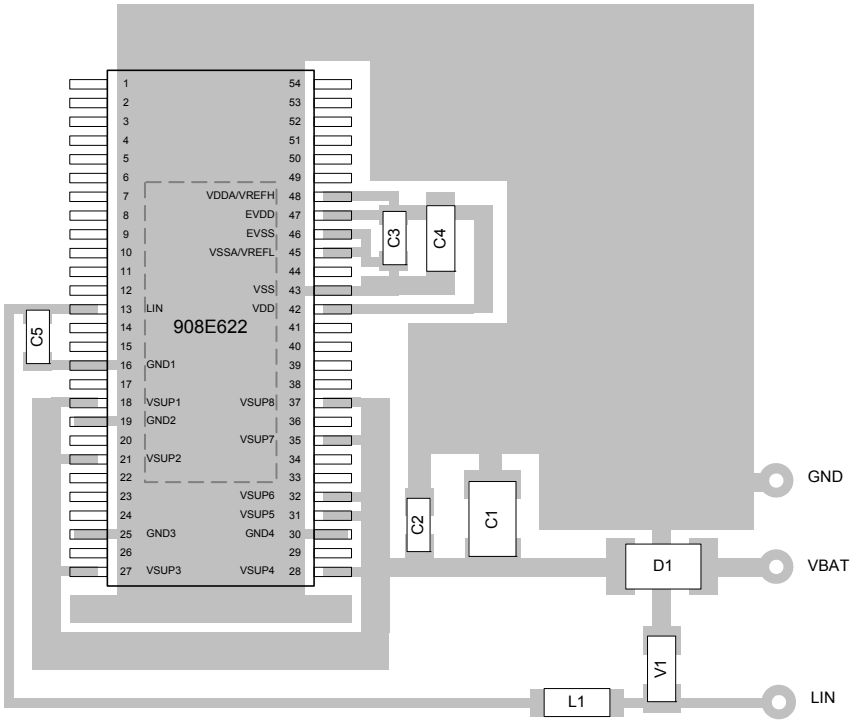


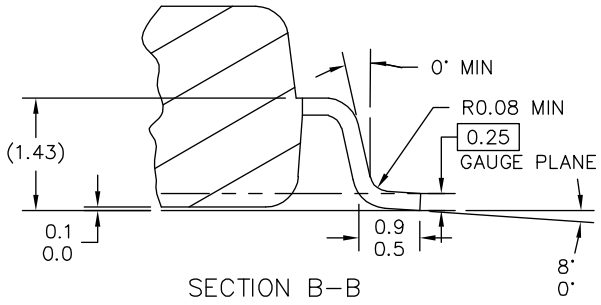
Figure 35. PCB Layout Recommendations

Table 24. Component Value Recommendation

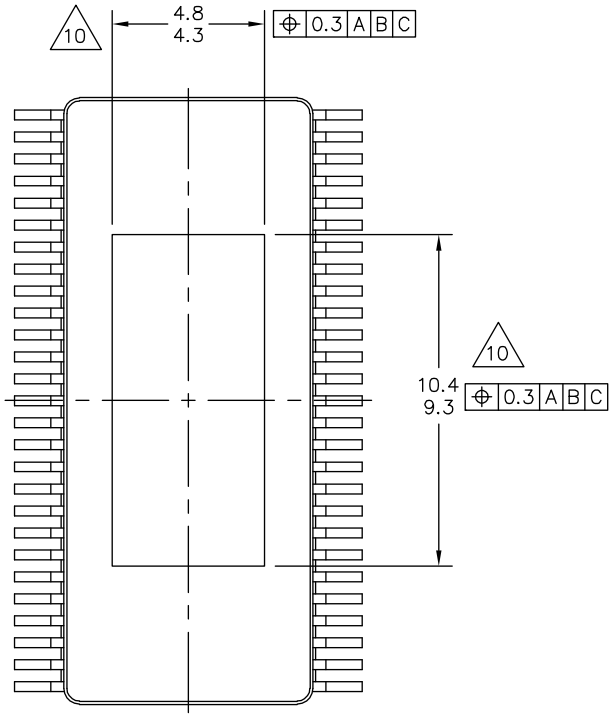
Component	Recommended Value[39]	Comments / Signal routing
D1		reverse battery protection
C1	Bulk Capacitor	
C2	100 nF, SMD Ceramic, Low ESR	Close to VSUP pins with good ground return
C3	100 nF, SMD Ceramic, Low ESR	Close (<3.0 mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH/ VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7 uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180 pF, SMD Ceramic, Low ESR	Close (<5.0 mm) to LIN pin. Total Capacitance on LIN has to be below 220pF. (C_{total} = $C_{LIN-Pin}$ + C5 + $C_{Varistor}$ ~ 10 pF + 180 pF + 15 pF)
V1[40]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[40]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

Notes

39. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
40. Components are recommended to improve EMC and ESD performance.



SECTION B–B



VIEW C–C

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TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D	REV: O
	CASE NUMBER: 1823–01	17 NOV 2005
	STANDARD: NON–JEDEC	

EK SUFFIX (Pb-free)
54-PIN SOICW-EP
98ASA10712D
ISSUE 0

908E622

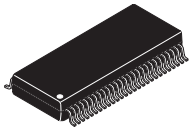
ADDITIONAL INFORMATION

THERMAL ADDENDUM

INTEGRATED QUAD H-BRIDGE, TRIPLE HIGH-SIDE AND EC GLASS DRIVER WITH EMBEDDED MCU AND LIN FOR MIRROR

908E622

54-PIN
SOICW-EP



98ASA10712D
54-PIN SOICW-EP

Note For package dimensions, refer to the 908E622 device datasheet.

Thermal Addendum

Introduction

This thermal addendum ia provided as a supplement to the MM908E622 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E622 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

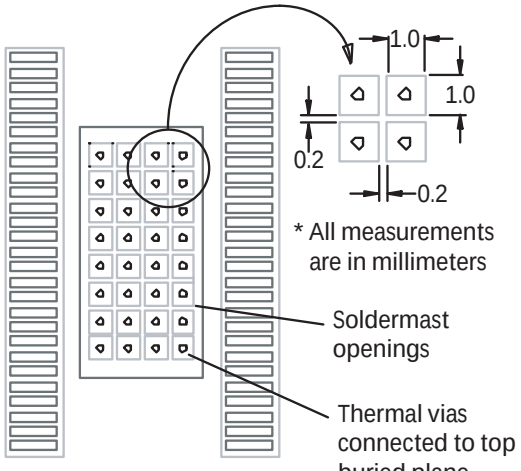
Standards

Table 25. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 36. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5

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