Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	12
Voltage - Supply	9V ~ 16V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e622acek

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low Voltage Reset (LVR)					
Threshold	V_{LVRON}	3.8	4.2	4.65	V
Hysteresis	V_{LVR_HYS}	50	–	300	mV
Low Voltage Interrupt (LVI)					V
Threshold	V_{LVION}	6.0	–	7.5	
Hysteresis	V_{LVI_HYS}	0.3	–	0.8	
High Voltage Interrupt (HVI)					V
Threshold	V_{HVION}	20	–	24	
Hysteresis	V_{HVI_HYS}	0.5	–	1.5	
High Temperature Interrupt (HTI)[11]					°C
Threshold T_J	T_{ION}	125	–	150	
Hysteresis	T_{IH}	5.0	–	10.0	
High Temperature Reset (HTR)[11]					°C
Threshold T_J	T_{RON}	155	–	180	
Hysteresis	T_{IH}	5.0	–	10.0	
VOLTAGE REGULATOR[12]					
Normal Mode Output Voltage[13]					V
I_{OUT} = 60 mA, 7.5 V < V_{SUP} < 20 V	V_{DDRUN1}	4.75	5.0	5.25	
I_{OUT} = 60 mA, V_{SUP} < 7.5 V and V_{SUP} > 20 V	V_{DDRUN2}	4.75	5.0	5.25	
Normal Mode Total Output Current	I_{OUTRUN}	–	120	150	mA
Load Regulation - I_{OUT} = 60 mA, V_{SUP} = 9.0 V, T_J = 125 °C	V_{LR}	–	–	100	mV
STOP Mode Output Voltage[13]	V_{DDSTOP}	4.75	5.0	5.25	V
STOP Mode Total Output Current	$I_{OUTSTOP}$	150	500	1100	µA

Notes

11. This parameter is guaranteed by process monitoring but is not production tested.
12. Specification with external low ESR ceramic capacitor 1.0 µF< C < 4.7 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Its not recommended to use capacitor values above 4.7 µF
13. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.

Table 3. Static Electrical Characteristics (continued)

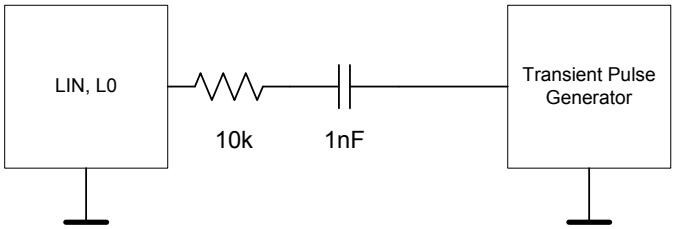
All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUT A0, A0CST					
Current Source A0, A0CST[23], [24]					µA
CSSEL1:0 = 00	I_{CS1}	–	40	–	
CSSEL1:0 = 01	I_{CS2}	–	120	–	
CSSEL1:0 = 10	I_{CS3}	–	320	–	
CSSEL1:0 = 11	I_{CS4}	–	800	–	
WAKE-UP INPUT L0					
Input Voltage Threshold Low	V_{LT}	–	–	1.5	V
Input Voltage Threshold High	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{LH}	0.5	–	–	V
Input Current	I_N	-10	–	10	µA
Wake-up Filter Time[25]	t_{WUP}	–	20	–	µs

Notes

23. This parameter is guaranteed only if correct trimming was applied
24. The current values are optimized to read a NTC temperature sensor, e.g. EPCOS type B57861 (R25 = 3000 Ω, R/T characteristic 8016)
25. This parameter is guaranteed by process monitoring but is not production tested.

TIMING DIAGRAMS



Note: Waveform in accordance to ISO7637 part 1, test pulses 1, 2, 3a and 3b.

Figure 4. Test Circuit for Transient Test Pulses

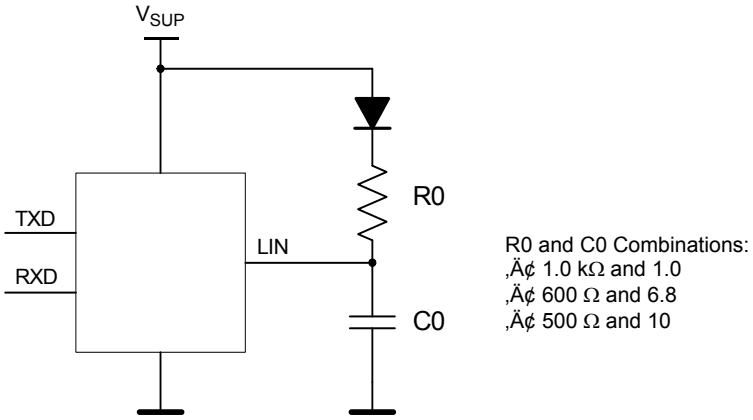


Figure 5. Test Circuit for LIN Timing Measurements

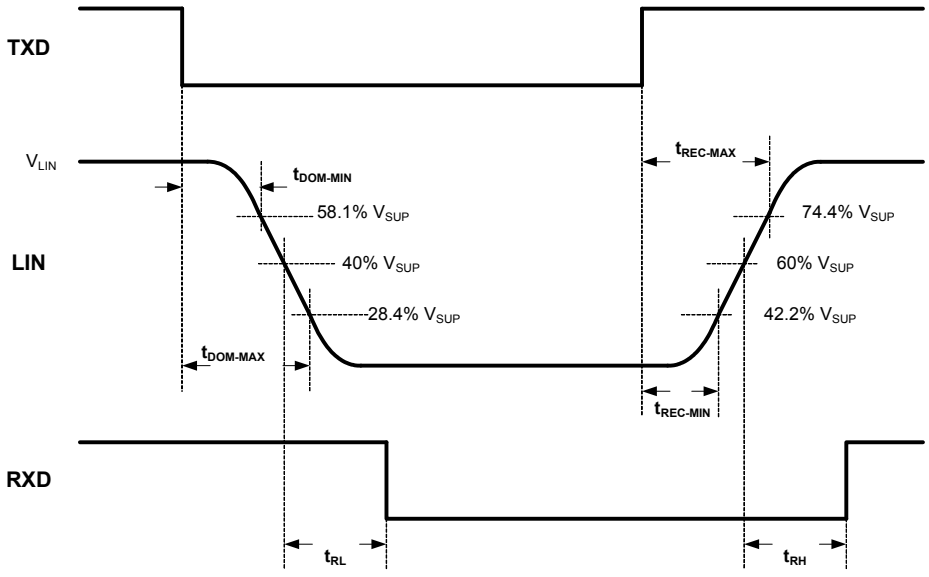


Figure 6. LIN Timing Measurements for Normal Slew Rate

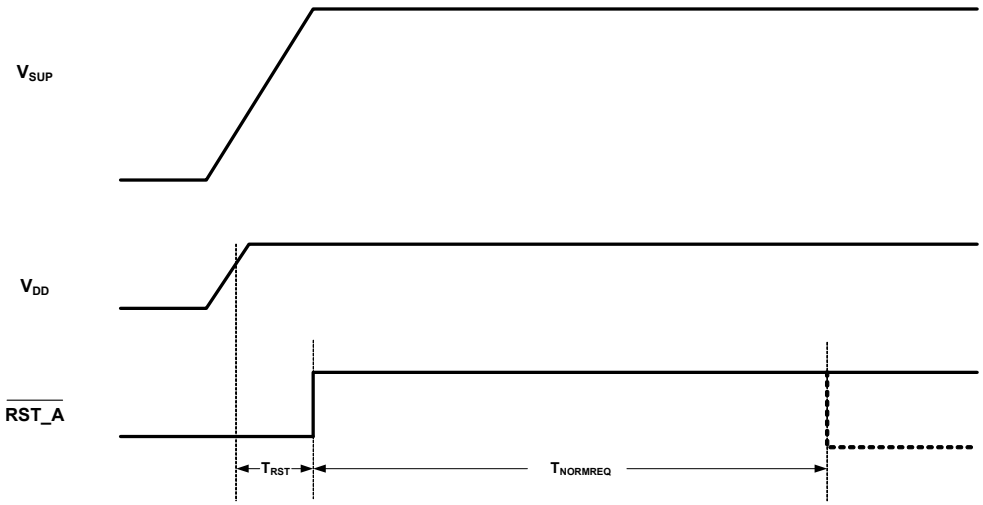


Figure 10. Power On Reset and Normal Request Timeout Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E622 was designed and developed as a highly integrated and cost effective solution for automotive and industrial applications. For automotive body electronics, the 908E622 is well suited to perform complete mirror control via a three-wire LIN bus.

This device combines an HC908EY16 MCU core with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as half-bridge outputs and three high side switches. Other ports are also provided, which include a circuitry for EC-glass control, one Hall-effect sensor input port, one analog input port with a switched current source, one wake-up pin, and a selectable HVDD pin. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See Figure 2, 908E622 Simplified Internal Block Diagram, page 2, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 3 for a depiction of the pin locations on the package.

PORT A I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device, and is internally connected to the SPI clock pin of the analog die.

The PTA6/$\overline{SS}$ pin is not accessible in this device, and is internally connected to the SPI slave select input of the analog die.

For details, refer to the 68HC908EY16 datasheet.

PORT B I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc.

The PTB1/AD1, PTB2/AD2, PTB6/AD6/TBCH0, PTB7/AD7/TBCH1 pins are not accessible in this device.

For details, refer to the 68HC908EY16 datasheet.

PORT C I/O PINS

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device, and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details, refer to the 68HC908EY16 datasheet.

PORT D I/O PINS

PTD0/TACH0/BEMF and PTD1/TACH1 are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

PTD0/TACH0 pin is internally connected to the PWM input of the analog die and only accessible for test purposes (cannot be used in the application).

For details, refer to the 68HC908EY16 datasheet.

PORT E I/O PIN

PTE0/TXD and PTE1/RXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

PTE1/RXD is internally connected to the RXD pin of the analog die and only accessible for test purposes (cannot be used in the application).

For details, refer to the 68HC908EY16 datasheet.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details, refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details, refer to the 68HC908EY16 datasheet.

The supply and reference signals are internally connected.

It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

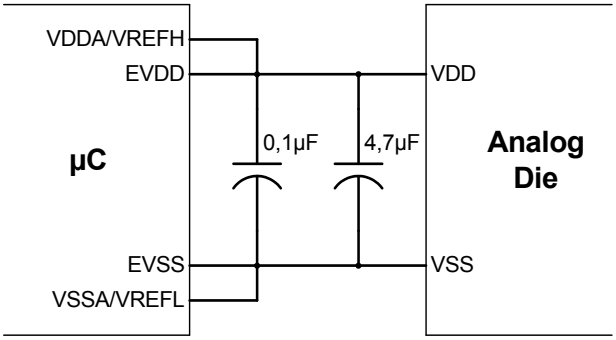
For details, refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 datasheet.



TEST MODE PIN (TESTMODE)

This pin is for test purpose only. In the application this pin must be forced to GND.

For Programming/Test this pin has to be forced to V_{DD} to bring the analog die into Test mode. In Test mode, the Reset Timeout (80 ms) is disabled and the LIN receiver is disabled

NOTE: After detecting a RESET (internal or external), the PSON bit needs to be set within 80 ms. If not the device will automatically enter sleep mode.

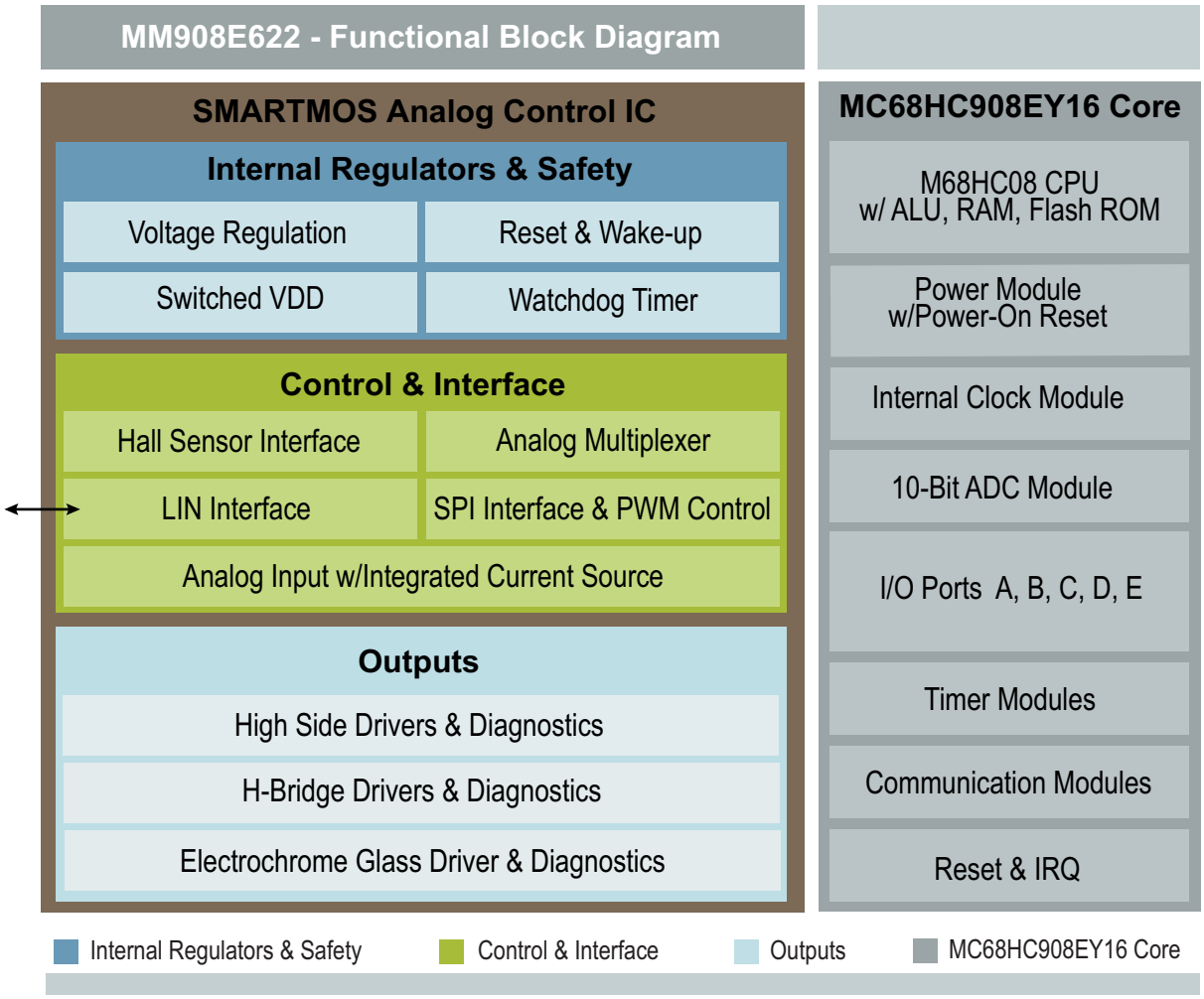
MCU TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or can be connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance, the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



SMARTMOS ANALOG CONTROL IC

INTERNAL REGULATORS & SAFETY:

VOLTAGE REGULATION

The voltage regulator circuitry provides the regulated voltage for the Analog IC, as well as the VDD/VSS rails for the core IC. The on-chip regulator consists of two elements, the main regulator, and the low voltage reset circuit. The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0 V to the microcontroller.

SWITCHED VDD

This function provides a switchable +5.0 V V_{DD} rail for an external load.

WATCHDOG TIMER

The watchdog timer module generates a reset, in case of a watchdog timeout or wrong watchdog timer reset. A watchdog reset event will reset all registers in the SPI, excluding the RSR.

RESET, IRQ & WAKE-UP

There are several functions on the Analog IC that can generate a reset or wake-up signal to the core IC. There is a pin that is used to detect an external wake-up event. The Reset signal has many possible sources in the Analog IC circuitry. The IRQ function on the Analog IC will notify the core IC of pending system critical conditions.

CONTROL & INTERFACE:

HALL SENSOR INTERFACE

This interface can be configured to support an input pin as a general purpose input, or as a hall-effect sensor input to be able to read 3-pin / 2-pin hall sensors or switches.

SPI INTERFACE & PWM CONTROL

The SPI and PWM interfaces are mastered by the core IC (CPU), and are used to control the output functions of the Analog IC, as well as to report status and failure information of the Analog IC.

LIN INTERFACE

The LIN interface function supports the single wire bus transmit and receive capabilities. It is suited for automotive bus systems, and is based on the LIN bus/physical layer specification. The LIN driver is a low side MOSFET with slope control, internal current limitation, and thermal shutdown.

ANALOG MULTIPLEXER

To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog IC. This multiplexer has eleven different sources on the Analog IC, which can be selected with the SS[3:0] bits (through SPI communication) in the A0MUCTL register.

ANALOG INPUT W/INTEGRATED CURRENT SOURCE

The A0 pin provides a switchable current source to allow the reading of switches, NTC, etc., without the need for an additional supply line for the sensor (single wire). There are four different selectable current source values.

OUTPUTS:

HIGH SIDE DRIVERS & DIAGNOSTICS

The HS outputs are low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM, or feature a real PWM capability using the PWM input.

H-BRIDGE DRIVERS & DIAGNOSTICS

The device includes power MOSFETs configured as four half-bridge driver outputs. These outputs are short-circuit and over-temperature protected. Over-current protection is done on both high side and low side MOSFETs.

ELECTROCHROME GLASS DRIVER & DIAGNOSTICS

The driver provides a controlled voltage, in order to adjust the transparency of an electrochrome glass, and to control the reflection of a rear view mirror. The value of the voltage can be adjusted by the use of an on-chip DA converter.

MM68HC908EY16 CORE IC -

M68HC08 CPU W/ALU, RAM, FLASH ROM

This possesses the functionality of the CPU08 architecture, along with 512 bytes of RAM and 15,872 bytes of FLASH memory, with in-circuit programming.

POWER MODULE W/P0WER-ON-RESET

This block of circuitry manages the power supplied to the core IC, as well as providing POR, LVI, Watchdog timer, and MCU supervision circuitry (COP).

INTERNAL CLOCK MODULE

This module provides the clocks needed by the core IC functions, without the need for external components. Software selectable bus frequencies are available. It also provides a clock monitor function.

10-BIT ADC MODULE

This module provides an 8-channel, 10-bit successive approximation analog-to-digital converter (ADC).

I/O PORTS A, B, C, D, E

There are many I/O pins that are controlled by the CPU through the several I/O ports of the core IC.

TIMER MODULES

There are two 16-bit, 2 channel timer interface modules with selectable input capture, output compare, and PWM capabilities for each channel.

COMMUNICATION MODULES

There are several communication functions supported by the core IC, including an enhanced serial communication interface module (ESCI) for the LIN communication, and an SPI module for inter-IC communication.

RESET & IRQ

There are interrupt and reset connections between the Analog IC and the core IC, for concise control and error/ exception management.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E622 ANALOG DIE MODES OF OPERATION

The 908E622 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

The different modes can be selected by the STOP and SLEEP bits in the System Control Register.

Figure 11 describes how transitions are done between the different operating modes, and Table 6, page 27 gives an overview of the operating modes.

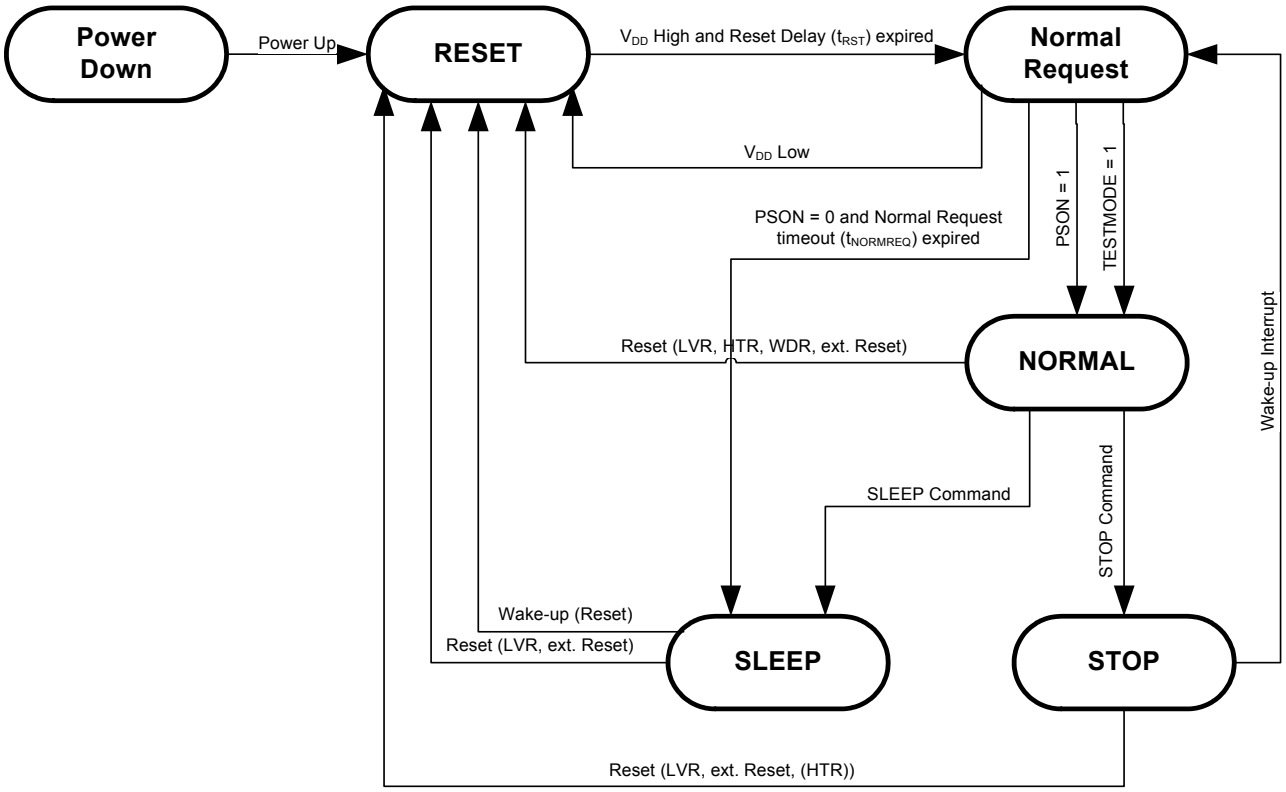


Figure 11. Operating Modes and Transitions

Normal Mode

This Mode is normal operating mode of the device. All functions and power stages are active and can be enabled/disabled. The voltage regulator provides the +5.0 V V_{DD} to the MCU.

After a reset (e.g. Power On Reset, Wake-up from Sleep), the MCU sets the PSON bit in the System Control Register within 80 ms typical ($t_{NORMREQ}$). This is to ensure the MCU has started up and is operating correctly. If the PSON bit is not set within the required time frame, the device enters SLEEP mode to reduce power consumption (fail safe).

This MCU monitoring can be disabled, e.g. for programming by applying V_{DD} on the TESTMODE pin.

Stop Mode

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability). To enter the Stop mode, the STOP bit in the System Control Register has to be set and the MCU has to be stopped (see the 908EY16 datasheet for details).

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0, and is maskable with the LINIE and/or L0IE bits in the Interrupt Mask Register. The analog die is generating an interrupt on $\overline{IRQ\_A}$ pin to wake-up the MCU. The wake-up / interrupt source can be evaluated with the L0IF and LINIF bits in the Interrupt Flag Register.

Stop mode has a higher current consumption than Sleep mode, but allows a quicker wake-up. Additionally, the wake-

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	$\overline{\text{RST\_A}}$ Output	MCU monitoring/ Watchdog Function	Power Stages	LIN Interface
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Disabled
Normal Request	V_{DD} ON	N/A	HIGH	$t_{NORMREQ}$ (80 ms typical) time out to set PSON bit in System Control Register	Disabled	Disabled
Normal (Run)	V_{DD} ON	N/A	HIGH	Window Watchdog active if enabled	Enabled	Enabled
Stop	V_{DD} ON with limited current capability	LIN wake-up, L0 state change (SPI PSON=1)(33)	HIGH	Disabled	Disabled	Recessive state with wake-up capability
Sleep	V_{DD} OFF	LIN wake-up L0 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability

Notes

33. The SPI is still active in Stop mode. However, due to the limited current capability of the voltage regulator in Stop mode, the PSON bit has to be set before the increased current caused from a running MCU causes an LVR.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 datasheet.

INTERRUPTS

The 908E622 has seven different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ pin is generated to report an event or fault to the MCU. All interrupts are maskable and can be enabled/disabled via the SPI (Interrupt Mask Register). After reset all interrupts are automatically disabled.

Low Voltage Interrupt

Low voltage interrupt (LVI) is related to external supply voltage V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVIF bit in the Interrupt Flag Register. In case the low voltage interrupt is enabled (LVIE = 1), an interrupt will be initiated.

During Sleep and Stop mode the low voltage interrupt circuitry is disabled.

High Voltage Interrupt

The high voltage interrupt (HVI) is related to the external supply voltage V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVIF bit in the Interrupt Flag Register. If the high voltage interrupt is enabled (HVIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HVI circuitry is disabled.

High Temperature Interrupt

The high temperature interrupt (HTI) is generated by the on chip temperature sensors. If the chip temperature is above the HTI threshold, the HTIF bit in the Interrupt Flag Register will be set. If the high temperature interrupt is enabled (HTIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HTI circuitry is disabled.

LIN Interrupt

The LIN Interrupt is related to the Stop mode. If the LIN interrupt is enabled (LINIE = 1) in Stop mode, an interrupt is asserted if a rising edge is detected, and the bus was dominant longer than t_{PROPWL}. After the wake-up / interrupt, the LINIF is indicating the reason for the wake-up / interrupt.

Power Stage Fail Interrupt

The power stage fail flag indicates an error condition on any of the power stages (see Figure 14, page 28).

In case the power stage fail interrupt is enabled (PSFIE = 1), an interrupt will be initiated if:

During Stop and Sleep mode, the PSFI circuitry is disabled.

HO Input Interrupt

The H0 interrupt flag H0IF is set in run mode by a state change of the H0F flag (rising or falling edge on the enabled input). The interrupt function is available if the input is selected as General Purpose, or as 2-pin Hall sensor input. The interrupt is maskable with the H0IE bit in the Interrupt Mask Register.

During Stop and Sleep mode the H0I circuitry is disabled.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP, and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

If the LIN interrupt is enabled (LINIE bit in the Interrupt Mask register is set), a dominant level longer than t_{PROPWL} followed by an rising edge will set the LINIF flag and generate an interrupt which causes a system wake-up (see Figure 8, page 18)

SLEEP Mode and Wake-up Feature

During SLEEP mode operation, the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP. A small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset), and set the LINWF flag in the Reset Status register (RSR). Also see Figure 9, page 18).

A0 INPUT AND ANALOG MULTIPLEXER

A0 - Analog Input

Input A0 is an analog input used for reading switches or as analog inputs for potentiometers, NTC, etc.

A0 is internally connected to the analog multiplexer. This pin offers a switchable current source. To read the Analog Input the pin, it has to be selected with the SS[3:0] bits in the A0MUCTL register.

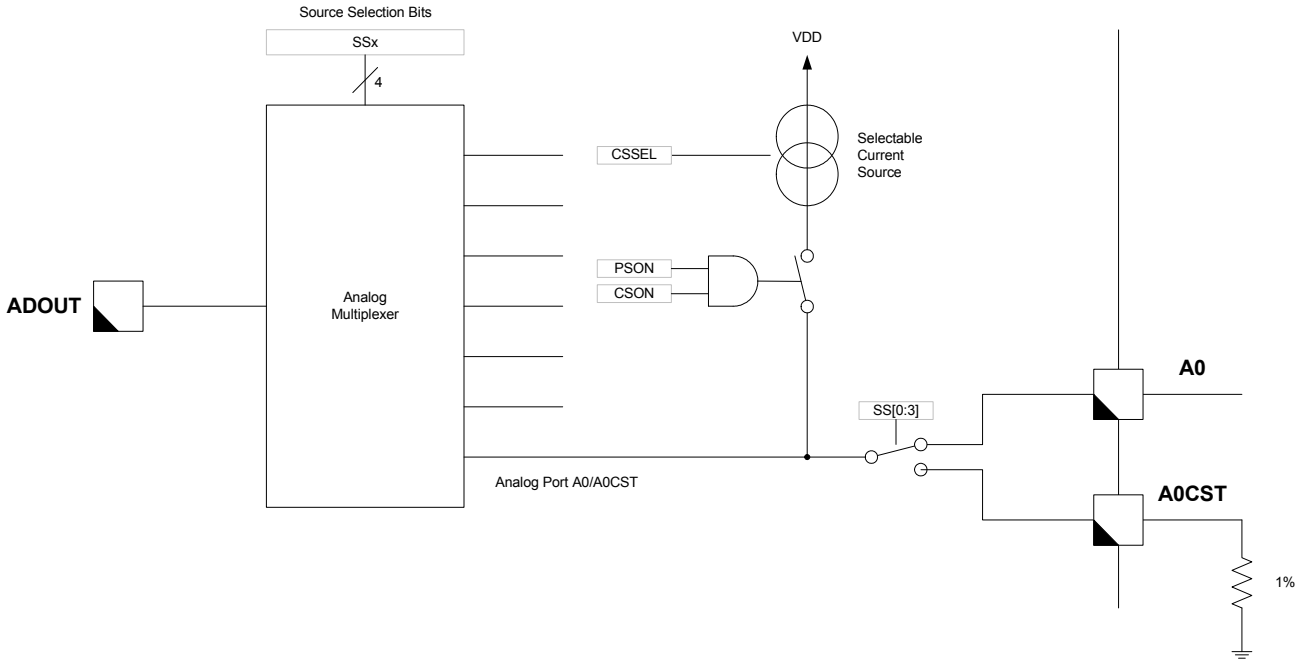


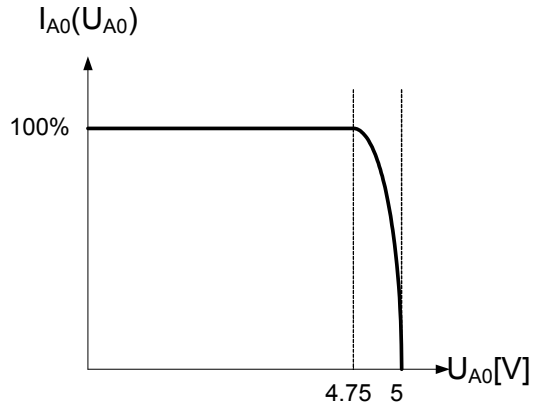
Figure 17. Analog Input and Multiplexer

A0 Current Source

The pin A0 provides a switchable current source, to be able to read in switches, NTC, etc., without the need of an additional supply line for the sensor. The overall enable of this feature is done by setting the PSON bit in the System Control register. In addition, the pin has to be selected with the SS[3:0] bits. The current source can be enabled with the CSON Bit, and adjusted with the bits CSSEL[1:0].

The CSSEL[1:0] bit's four different current values can be selected (40, 120, 320 and 800µA). This function is halted during STOP and SLEEP mode operations.

The current source is derived from the V_{DD} voltage and is constant up to an output voltage of ~4.75 V.



To calibrate the current sources an extra pin (A0CST) is envisioned. On this pin, an accurate resistor can to be connected. Switching the current sources to this resistor allows the user to measure the current, and use the measured value for calculating the current on A0.

Analog Multiplexer / ADOUT Pin

The ADOUT pin is the analog output interface to the Analog-to-digital converter of the MCU. To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog die. This multiplexer has twelve different sources, which can be selected with the SS[3:0] bits in the A0MUCTL register.

Half-bridge (HB1:HB4) Current Recopy

The multiplexer is connected to the four current sense circuits on the low side FET of the half bridges. This sense circuits offers a voltage proportional to the current through the MOSFET. The resolution is depending on the CSA bit in the A0 and Multiplexer control register (A0MUCTL).

High Side (HS1:HS3) Current Recopy

The multiplexer is connected to the three high side switches. These sense circuits offer a voltage proportional to the current through the transistor.

Analog Input A0 and A0CST

A0 and A0CST are directly connected to the analog multiplexer. It offers the possibility to read analog values from the periphery.

Temperature Sensor

The analog die includes an on chip temperature sensor. This sensor offers a voltage which is proportional to the actual mean chip junction temperature.

VSUP Prescaler

The VSUP prescaler offers a possibility to measure the external supply voltage. The output of this voltage is V_{SUP} / $RATIO_{VSUP}$.

EC Output

The EC output is directly connected to the multiplexer to be able to read the actual voltage on the EC pin.

A0 and Multiplexer Control Register (A0MUCTL)

Register Name and Address: A0MUCTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read Write	CSON	CSSEL 1	CSSEL 0	CSA	SS3	SS2	SS1	SS0
Reset	0	0	0	0	0	0	0	0

CSON — Current Source on/off

This read/write bit enables the current source for the A0 or A0CST inputs. Reset clears CSON bit.

1 = Current Source enabled
0 = Current Source disabled

CSSEL[1:0] — Current Source Select Bits

These read/write bits select the current source values for A0 or A0CST input. Reset clears CSSEL[1:0] bits.

Table 7. A0 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	40 µA
0	1	120 µA
1	0	320 µA
1	1	800 µA

CSA — H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-bridges HB1:HB4 current recopy. Reset clears the CSA bit.

1 = low current sense amplification
0 = high current sense amplification

SS[3:0] — Analog Source Input Select Bits

These read/write bits selects the analog input source for the ADOUT pin. Reset clears the SS[3:0] bits

Table 8. Analog Multiplexer Configuration Bits

SS3	SS2	SS1	SS0	Channel
0	0	0	0	current recopy HB1
0	0	0	1	current recopy HB2
0	0	1	0	current recopy HB3
0	0	1	1	current recopy HB4
0	1	0	0	current recopy HS1

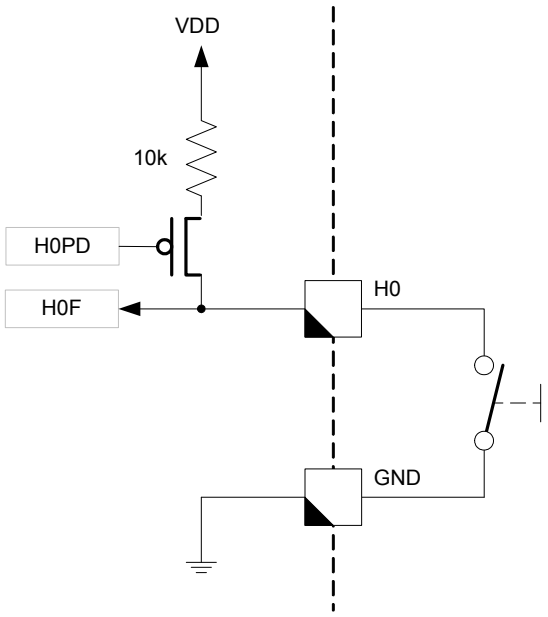


Figure 21. H0 Used to Read in Standard Switches

H0 Interrupt

The interrupt functionality on this pin is only available in RUN mode. H0 interrupt flag H0IF is set in run mode by a state change of the H0 flag (rising or falling edge on the enabled input). The interrupt function is available if the input is selected as General Purpose, or as a 2-pin Hall sensor input. The interrupt can be masked with the H0IE bit in the interrupt mask register.

Wake-up Input L0

The device provides one wake-up capable input for reading VSUP or VDD related signals.

RUN Mode

The actual input state is reflected in the L0F bit of the H0/L0 Status and Control register (HLSCTL).

The L0 pin offers an interrupt capability on rising and falling edge. The interrupt can be enabled with the L0IE bit in the Interrupt Mask register.

STOP/SLEEP Mode

During STOP and SLEEP mode, the pin can be used to wake-up the device.

Before entering the STOP or SLEEP mode, the actual state of the input is stored. If the state is changing during in the STOP or SLEEP mode, a wake-up is initiated.

H0 / L0 Status and Control Register (HLSCTL)

Register Name and Address: HLSCTL - $07

	Bit7	6	5	4	3	2	1	Bit0
Read	L0F	0	0	H0OCF	H0F	H0EN	H0PD	H0MS
Write								
Reset	0	0	0	0	0	0	0	0

L0F — L0 Flag Bit

This read only flag reflects the state of the L0 input

1 = L0 input high
0 = L0 input low

H0OCF — H0 Over-current Flag Bit

This read/write flag is set with an over-current condition on H0 during 2pin Hall sensor mode. Clear H0OCF by writing a logic [1] to H0OCF. Reset clears the H0OCF bit.

1 = over-current condition on H0 pin has occurred
0 = no over-current condition on H0 pin has occurred

H0F — H0 Flag Bit

This read only flag reflects the state of the H0 input

1 = Hallport sensed high / current below threshold detected
0 = Hallport sensed low / current above threshold detected

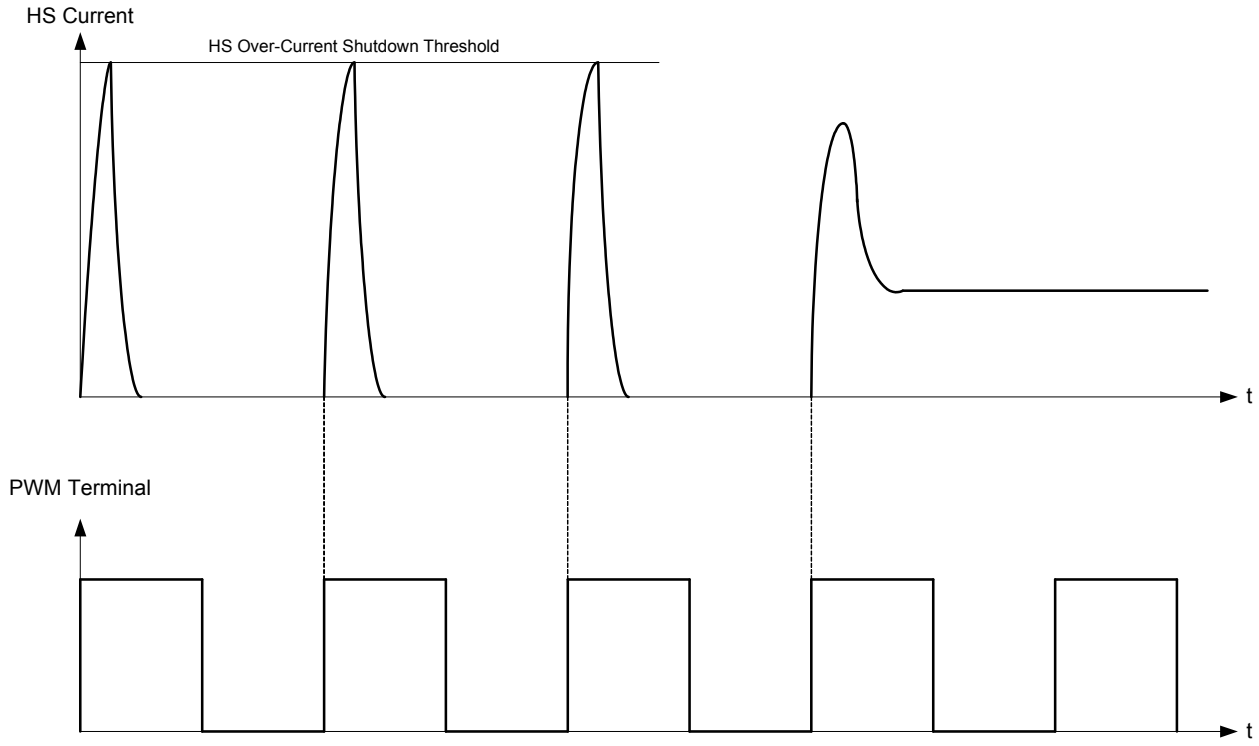


Figure 24. Inrush Current Limitation on HS Outputs

High Side Current Recopy

Each high side has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the Analog Multiplexer.

Switchable HVDD Outputs

The HVDD pin is a switchable 5.0 V output pin. It can be used for driving external circuitry which requires a 5.0 V voltage. The output is enabled with the PSON bit in the System Control register and can be switched on / off with the HVDD_ON bit in the High Side Out register. Low or high voltage conditions (LVIF / HVIF) will have no influence on this circuitry.

HVDD Over-temperature Protection

The output is protected against over-temperature conditions.

HVDD Over-current Protection

The HVDD output is protected against over-current. In case the current reach the over-current limit, the output current will be limited and the HVDDOCF over-current flag in the System Status register is set.

High Side Out Register (HSOUT)

Register Name and Address: HSOUT - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	HVDD ON	0	HS3P WM	HS2P WM	HS1P WM	HS3O N	HS2O N	HS1O N
Write								
Reset	0	0	0	0	0	0	0	0

HVDD-ON — HVDD On Bit

This read/write bit enables the HVDD output. Reset clears the HVDDON bit.

1 = HVDD enabled
0 = HVDD disabled

HSxON — High Side on/off Bits

These read/write bits turn on the High Side FETs permanently. Reset clears the HSxON bits.

1 = High Side x is turned on
0 = High Side x is turned off

HSxPWM — High Side PWM on/off Bits

These read/write bits enable the PWM control of the High Side FETs. Reset clears the HSxPWM bits.

1 = High Side x is controlled by PWM input signal
0 = High Side x is not controlled by PWM input signal

High Side Status Register (HSSTAT)

Register Name and Address: HSSTAT - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	HVDD OCF	0	0	0	0	HS3O CF	HS2O CF	HS1O CF
Write								
Reset	0	0	0	0	0	0	0	0

HSxOCF — High Side Over-current Flag Bit

This read/write flag is set by an over-current condition at the high side drivers x. Clear HSxOCF and enable the HS Driver by writing a logic [1] to HSxOCF. Writing a logic [0] to HSxOCF has no effect. Reset clears the HSxOCF bit.

1 = over-current condition on high side drivers has occurred
0 = no over-current condition on high side drivers has occurred

HVDDOCF — HVDD Output Over-current Flag Bit

This read/write flag is set by an over-current condition at the HVDD pin. Clear HVDDOCF and enable the output by writing a logic [1] to the HVDDOCF Flag. Writing a logic [0] to HVDDOCF has no effect. Reset clears the HVDDOCF bit.

1 = over-current condition on VDD output has occurred
0 = no over-current condition on VDD output has occurred

Electrochrome Circuitry

The EC glass is controlled by two transistors. T1 switches the EC glass on/off, and T2 controls the EC output voltage given by the 6-Bit DA Converter.

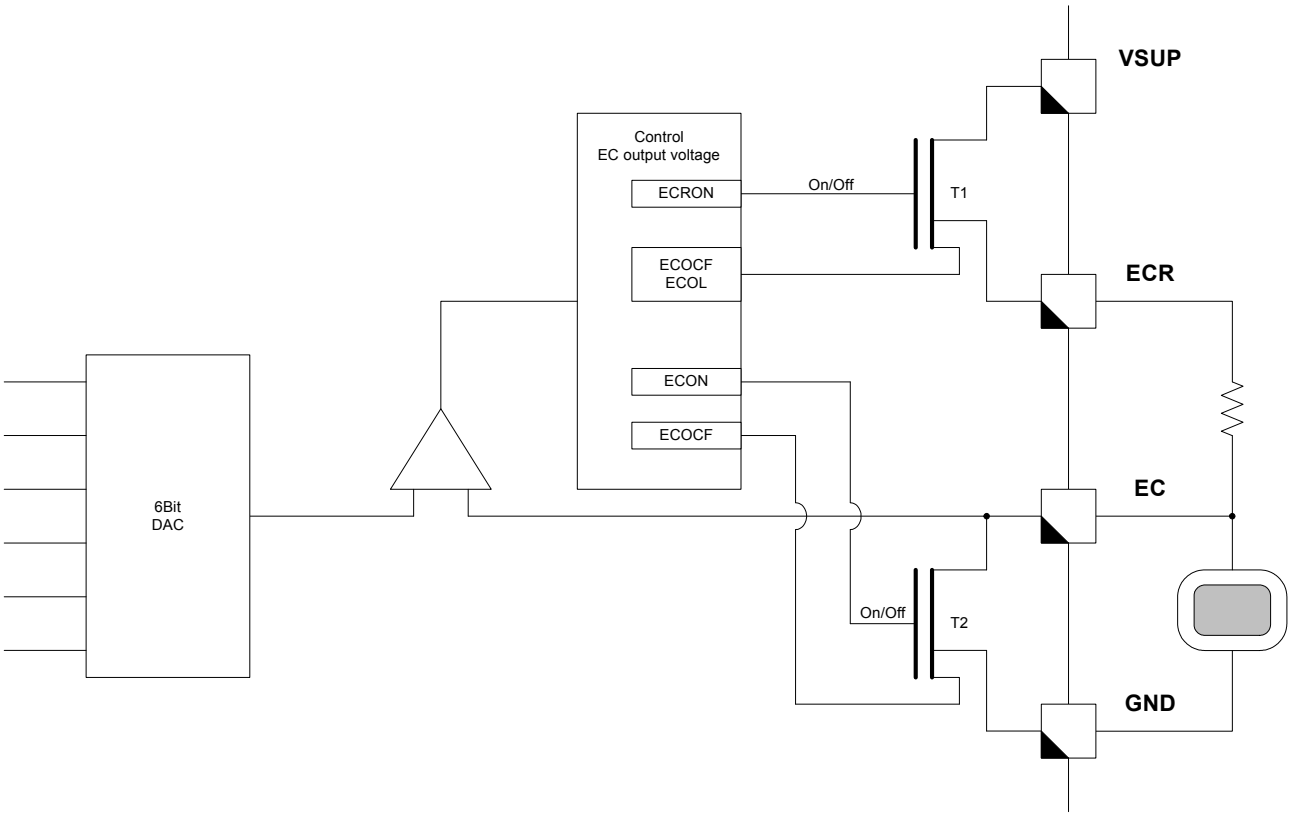


Figure 25. EC Circuitry

EC Open Load Detection

Open Load can be detected by setting ECOLT. A small current source sources a typical 200 μA on the EC pin, and the voltage on the pin is measured. If the voltage is above the typical 2.0 V (typical 10 k threshold), the ECOLF bit in the EC Status and Control Register ECSCTL is set, indicating the open load condition.

If the Open load circuitry is activated (ECOLT=1), the EC glass is disabled.

EC Short-circuit Protection

The EC output is protected against shorts to VSUP. In case of a short-circuit, the ECOCF in the EC Status and the Control Register (ECSCTL) are set, and the EC circuitry is disabled.

Table 13. SPI Register Overview

$08	A0 and Multiplexer Control (A0MUCTL)	R	CSON	CSSEL1	CSSEL0	CSA	SS3	SS2	SS1	SS0
		W								
$09	Interrupt Mask (IMR)	R	L0IE	H0IE	LINIE	HTRD	HTIE	LVIE	HVIE	PSFIE
		W								
$0A	Interrupt Flag (IFR)	R	L0IF	H0IF	LINIF	0	HTIF	LVIF	HVIF	PSFIF
		W								
$0B	Watchdog Control (WDCTL)	R	WDRE	WDP1	WDP0	0	0	0	0	0
		W								WDRST
$0C	System Status (SYSSTAT)	R	LINCL	HTIF	VF	H0F	HVDDF	HSF	HBF	ECF
		W								
$0D	Reset Status (RSR)	R	POR	PINR	WDR	HTR	LVR	0	LINWF	L0WF
		W								
$0E	System Test (SYSTEST)	R	reserved							
		W								
$0F	System Trim 1 (SYSTRIM1)	R	HVDDT1	HVDDT0	reserved	reserved	itrim3	itrim2	itrim1	itrim0
		W								
$10	System Trim 2 (SYSTRIM2)	R	0	0	0	0	0	0	0	0
		W	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
$11	System Trim 3 (SYSTRIM3)	R	0	0	0	0	0	0	0	0
		W	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0

Factory TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E622, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” ($FF) state:

- $FD80:$FDDF Trim and Calibration Values
- $FFFE:$FFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values located in the flash memory is explained by the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller, without using any external components. The untrimmed frequency of the low frequency base clock (IBASE) will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate these dependencies, a ICG trim value is located at address $FDC2. After trimming, the ICG is in a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100 nF), and stabilized (4.7 μF) V_{DD} = 5.0 V, $T_{AMBIENT}$~25°C), and will vary over temperature and voltage (V_{DD}), as indicated in the 68HC908EY16 datasheet.

To trim the ICG, this value has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to copied after every reset.

Watchdog Period Range Value (AWD Trim)

The window watchdog supervises device recovery (e.g. from code runaways).

The application software has to clear the watchdog within the open window. Due to the high variation of the watchdog period, and therefore the reduced width of the watchdog window, a value is stored at address $FDCF. This value classifies the watchdog period into 3 ranges (Range 0, 1, 2). It allows the application software to select one of three time intervals to clear the watchdog based on the stored value. The classification is done in a way that the application software can have up to ±19% variation of the of optimal clear interval, e.g. caused by ICG variation.

Effective Open Window

Having a variation in the watchdog period in conjunction with a 50% open window, results in an effective open window, which can be calculated by:

latest window open time: t_open = t_wd max / 2

earliest window closed time: t_closed = t_wd min

Optimal Clear Interval

The optimal clear interval, meaning the clear interval with the biggest possible variation to latest window open time, and to the earliest window closed time, can be calculated with the following formula:

t_opt = t_open + (t_open+t_closed) / 2

See Table 14 to select the optimal clear interval for the watchdog based on the Window No. and chosen period.

Table 14. Window Clear Interval

Window Range	Period Select bits	Watchdog Period t_wd			Effective Open Window			Optimal Clear Interval		
$FDCF	WDP1:0	min.	max.	Unit	t_open	t_closed	Unit	t_opt	Unit	max. variation
0	00	68	92	ms	46	68	ms	57	ms	±19.3%
	01	34	46		23	34		28.5		
	10	17	23		11.5	17		14.25		
	11	8.5	11.5		5.75	8.5		7.125		
1	00	92	124	ms	62	92	ms	77	ms	±19.5%
	01	46	62		31	46		38.5		
	10	23	31		15.5	23		19.25		
	11	11.5	15.5		7.75	11.5		9.625		
2	00	52	68	ms	34	52	ms	43	ms	±20.9%
	01	26	34		17	26		21.5		
	10	13	17		8.5	13		10.75		
	11	6.5	8.5		4.25	6.5		5.375		

Analog Die System Trim Values

For improved application performance, and to ensure the outlined datasheet values, the analog die needs to be trimmed. For this purpose, 3 trim values are stored in the Flash memory at addresses $FDC4 - $FDC6. These values have to be copied into the analog die SPI registers:

- copy $FDC4 into SYSTRIM1 register $0F
- copy $FDC5 into SYSTRIM2 register $10
- copy $FDC6 into SYSTRIM3 register $11

Note: These values have to be copied to the respective SPI register after a reset, to ensure proper trimming of the device.

System Test Register (SYSTEST)

Register Name and Address: SYSTEST - $0E

	Bit7	6	5	4	3	2	1	Bit0
Read Write	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0

Note: do not write to the reserved bits

The System Test Register is reserved for production testing and is not allowed to be written into.

System Trim Register 1 (SYSTRIM1)

Register Name and Address: IBIAS - $0F

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HVDDT1	HVDDT0	0 reserved	0 reserved	ITRIM3	ITRIM2	ITRIM1	ITRIM0
Reset	0	0	0	0	0	0	0	0

Note: do not change (set) the reserved bits

HVDDT1:0 - HVDD Over-current Shutdown Delay Bits

These read/write bits allow changing the filter time (for capacitive load) for the HVDD over-current detection. Reset clears the HVDDT1:0 bits an sets the delay to the maximum value.

System Trim Register 3 (SYSTRIM3)

Register Name and Address: IFBHSTRIM - $11

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0
Reset	0	0	0	0	0	0	0	0

CRHBHC3:2 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC3:2 bits.

Table 20. Current Recopy Trim for HB3:4 (CSA=0)

CRHBHC3	CRHBHC2	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHS5:3 - Current Recopy HS2:3 Trim Bits

These write only bits are for trimming the current recopy of the high side HS2 and HS3. The provided trim values have to be copied into these bits after every reset. Reset clears the CRHS5:3 bits.

Table 21. Current Recopy Trim for HS2:3

CRHS5	CRHS4	CRHS3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHS2:0 - Current Recopy HS1 Trim Bits

These write only bits are for trimming the current recopy of the high side HS1. The provided Trim values have to be copied into these bits after every reset. Reset clears the CRHS2:0 bits.

Table 22. Current Recopy Trim for HS1

CRHS2	CRHS1	CRHS0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E622 has the MC68HC908EY16 MCU embedded, typically all the development tools available for the MCU also apply for this device. However, due to the additional analog die circuitry and the nominal +12 V supply voltage, some additional items have to be considered:

- nominal 12 V rather than 5.0 or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin
- MCU monitoring (Normal request timeout) has to be disabled

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process, first on chip level, before the IC is soldered onto a pcb board, and second after the IC is soldered onto the pcb board.

Chip Level Programming

At the Chip level, the easiest way is to only power the MCU with +5.0 V (see Figure 32), and not to provide the analog chip with VSUP. In this setup, all the analog pins should be left open (e.g. VSUP[1:8]), and interconnections between the MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

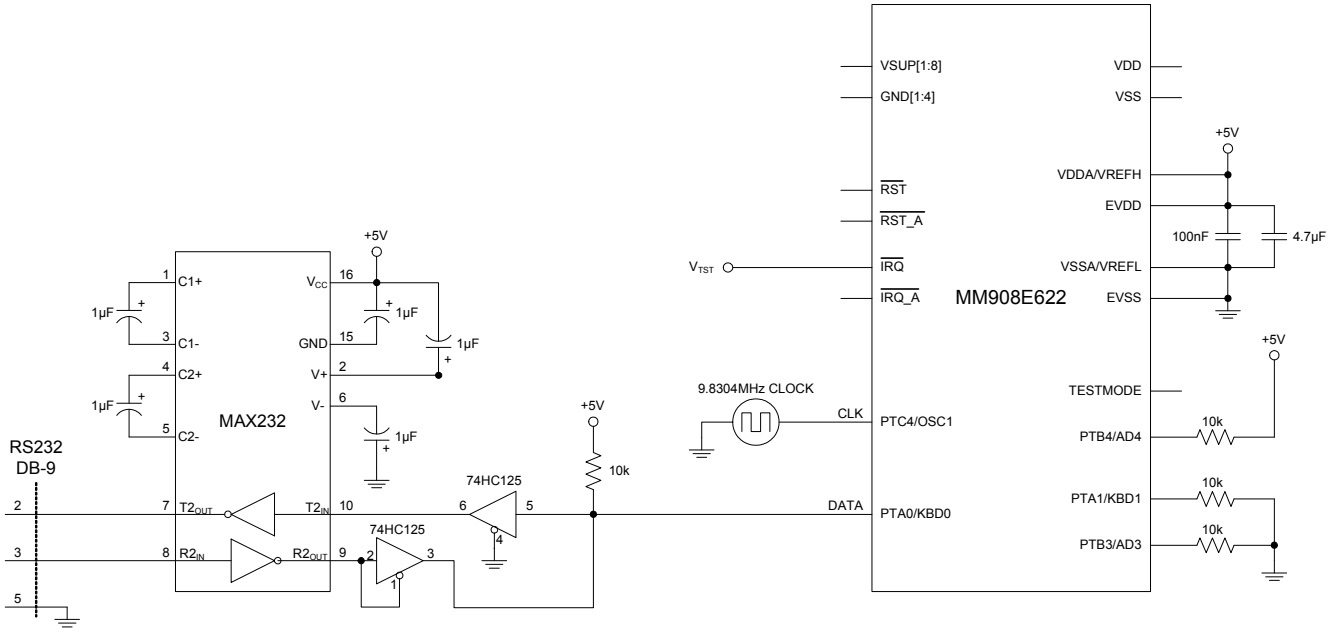


Figure 32. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with V_{SUP} instead (12 V), as described in Figure 33, page 53.

PCB Level Programming

If the IC is soldered onto the pcb board, its typically not possible to separately power the MCU with +5.0 V. The whole system has to be powered up and providing V_{SUP} (see Figure 33).

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	6/2008	• Added Revision History • Changed STOP Mode Total Output Current on page 9 from 850 to 1100μA • Changed Sense Current Hysteresis on page 13 from 800 to 650μA • Changed Normal Request Timeout on page 16 from 124 to 150ms • Updated Freescale form and style to the current format • Updated package drawing • Added Functional Internal Block Description section
3.0	4/2012	• Added MM908E622ACPEK/R2 to the ordering information • Removed MM908E622ACDWB/R2 from the ordering information • Updated Freescale form and style to the current format