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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive Mirror Control
Core Processor	HC08
Program Memory Type	FLASH (16kB)
Controller Series	908E
RAM Size	512 x 8
Interface	SCI, SPI
Number of I/O	12
Voltage - Supply	9V ~ 16V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	54-SSOP (0.295", 7.50mm Width) Exposed Pad
Supplier Device Package	54-SOIC-EP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm908e622acpek

Table 1. Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 20.

Die	Pin	Pin Name	Formal Name	Definition
Analog	40	L0	Wake-up Input	This pin provides an high voltage input, which is wake-up capable.
Analog	41	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g. potentiometers.
Analog	42	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	43	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions(1) MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 5.5	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins except VDD, VSS, PTA0:PTA4 PTA0:PTA4	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 17)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
ESD Voltage Human Body Model(2) H0 pin Human Body Model(2) all other pins Machine Model(2) Charge Device Model(2)	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3}	 ±1000 ±2000 ±200 ±750	V

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Ambient Temperature[3]	T_A	-40 to 85	°C
Operating Junction Temperature[4]	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C

Notes

3. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
4. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150 °C under these conditions.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP1}	9.0	—	16	V
Extended Operating Voltage (LIN only 8…18 V)(8)	V_{SUP2}	7.5	—	20	V
SUPPLY CURRENT RANGE					
Normal Mode(8) V_{SUP} = 12 V, Analog Chip in Normal Mode (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	25	—	mA
Stop Mode(8), (9) V_{SUP} = 12 V, Voltage Regulator with limited current capability	I_{STOP}	—	40	50	µA
Sleep Mode(8), (9) V_{SUP} = 12 V, Voltage Regulator off	I_{SLEEP}	—	12	20	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output pins $\overline{RST\_A}$, $\overline{IRQ\_A}$, RXD (MISO probe only)					V
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High-state Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	–	–	
Output pin RXD - Capacitance(10)	C_{OUT}	–	4.0	–	pF
Input pins $\overline{RST\_A}$, PWM ($\overline{SS}$, MOSI, TXD probe only)					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input pins - Capacitance(10)	C_{IN}	–	4.0	–	pF
Pins $\overline{IRQ\_A}$, $\overline{RST\_A}$ - Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pins $\overline{SS}$ - Pull-up Resistor	$R_{PULLUP2}$	–	100	–	kΩ
Pins MOSI, SPSCK, PWM - Pull-down Resistor	$R_{PULLDOWN}$	–	100	–	kΩ
Pin TXD - Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

7. Device is fully functional, but some of the parameters might be out of spec.
8. Total current measured at GND pins.
9. Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
10. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pull-up Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pull-up Resistor to VSUP	R_{PU}	20	30	47	kΩ
Stop, Sleep Mode Pull-up Current Source	I_{PU}	—	20	—	µA
Output Current Shutdown Threshold	I_{BLIM}	100	230	280	mA
Output Current Shutdown Timing	I_{BLS}	5.0	–	40	µs
Leakage Current to GND					
V_{SUP} Disconnected, V_{BUS} at 18 V	I_{BUS}	–	1.0	10	µA
Recessive state, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V ≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}	$I_{BUS\text{-}PAS\text{-}REC}$	0.0	3.0	20	µA
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V	$I_{BUS\text{-}NOGND}$	-1.0	–	1.0	mA
LIN Receiver					VSUP
Receiver Threshold Dominant	V_{BUS_DOM}	–	–	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	–	–	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	–	–	0.175	
HIGH SIDE OUTPUT HS1					
Switch On Resistance					mΩ
T_J = 25 °C, I_{LOAD} = 1.0 A	$R_{DS(ON)\text{-}HS1}$	–	185	225	
Over-current Shutdown	I_{HSOC1}	6.0	–	9.0	A
Over-current Shutdown blanking time[14]	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio[15]	$CR_{RATIOHS1}$	0.84	1.2	1.56	V/A
V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2.0 A)					
High Side Switching Frequency[14]	f_{PWMHS}	–	–	25	kHz
High Side Freewheeling Diode Forward Voltage	V_{HSF}	–	0.9	–	V
T_J = 25 °C, I_{LOAD} = 1.0 A					
Leakage Current	I_{LeakHS}	–	<0.2	10	µA

Notes

14. This parameter is guaranteed by process monitoring but is not production tested.
15. This parameter is guaranteed only if correct trimming was applied.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUT A0, A0CST					
Current Source A0, A0CST[23], [24]					µA
CSSEL1:0 = 00	I_{CS1}	–	40	–	
CSSEL1:0 = 01	I_{CS2}	–	120	–	
CSSEL1:0 = 10	I_{CS3}	–	320	–	
CSSEL1:0 = 11	I_{CS4}	–	800	–	
WAKE-UP INPUT L0					
Input Voltage Threshold Low	V_{LT}	–	–	1.5	V
Input Voltage Threshold High	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{LH}	0.5	–	–	V
Input Current	I_N	-10	–	10	µA
Wake-up Filter Time[25]	t_{WUP}	–	20	–	µs

Notes

23. This parameter is guaranteed only if correct trimming was applied
24. The current values are optimized to read a NTC temperature sensor, e.g. EPCOS type B57861 (R25 = 3000 Ω, R/T characteristic 8016)
25. This parameter is guaranteed by process monitoring but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40 °C ≤ T_J ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate[26], [27]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.0 V…18 V	D1	0.396	–	–	
Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.6 V…18 V	D2	–	–	0.581	
Driver Characteristics for Slow Slew Rate[26], [28]					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.0 V…18 V	D3	0.417	–	–	
Duty Cycle4: D4 = $t_{BUS\_REC(MAX)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.6 V…18 V	D4	–	–	0.590	
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	20	—	V/µs
Receiver Characteristics and Wake-up Timings					
Receiver Dominant Propagation Delay[29]	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay[29]	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-up Deglitcher	t_{PROPWL}	30	50	150	µs
Bus Wake-up Event Reported [30]	t_{WAKE}	—	20	—	µs

Notes

26. V_{SUP} from 7.0 to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
27. See Figure 6, page 17.
28. See Figure 7, page 18.
29. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
30. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 9 and Figure 8, page 18. In Sleep mode, the V_{DD} rise time is strongly dependent upon the decoupling capacitor at the VDD pin.

POWER SUPPLY PINS (VSUP1:VSUP8)

VSUP1:VSUP8 are device power supply pins. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1:GND4)

GND1:GND4 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high side output drivers, multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E622 device includes power MOSFETs configured as four half-bridge driver outputs. The HB3:HB4 have a lower $R_{DS(ON)}$, to run higher currents (e.g. fold motor), than the HB1:B2 outputs.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy. Over-current protection is done on both high side and low side FET's. The current recopy are done on the low side MOSFETs.

HIGH SIDE OUTPUT PINS (HS1:HS3)

The HS output pins are a low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM or feature a real PWM capability using the PWM input.

The HS1 has a lower $R_{DS(ON)}$, to run higher currents (e.g. heater) than the HS2 and HS3 outputs.

For the HS1 two pins (HS1a:HS1b) are necessary for the current capability and have to be connected externally.

Important: The HS3 can be only used to drive resistive loads.

EC GLASS PINS (ECR, EC)

These pins are used to drive the electrochrome function on EC glass mirrors. The ECR pin is used to connect an external ballast resistor. The EC pin provides the mirror with an regulated output voltage up to 1.4 V. The output voltage can be selected by an integrated DA converter.

HALL-EFFECT SENSOR INPUT PIN (H0)

The Hall-effect sensor input pin H0 provides an input for Hall-effect sensors (2-pin or 3-pin) or a switch.

ANALOG INPUT PINS (A0, A0CST)

These pins are analog inputs with selectable current source values. The A0CST is intent to trim the A0 input.

WAKE-UP INPUT PIN (L0)

This pin is 40 V rated input. It can be used as wake-up source for a system wake-up. The input is falling or rising edge sensitive.

Important: If unused, this pin should be connected to VSUP or GND to avoid parasitic transitions. In Low Power mode, this could lead to random wake-up events.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable VDD output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-pin Hall-effect sensors or potentiometers. The output is short-circuit protected.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

+5.0 V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD and VDDA/VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors). **Important** VSS, EVSS and VSSA/VREFL pins must be connected together.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

ADC SUPPLY/REFERENCE PINS (VDDA/VREFH AND VSSA/VREFL)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC).

VREFH and VREFL are the reference voltage pins for the ADC.

The supply and reference signals are internally connected.

It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

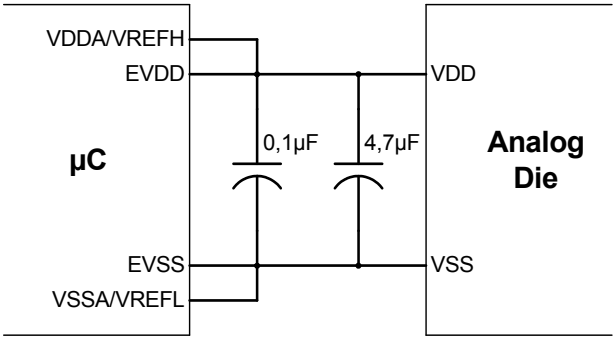
For details, refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 datasheet.



TEST MODE PIN (TESTMODE)

This pin is for test purpose only. In the application this pin must be forced to GND.

For Programming/Test this pin has to be forced to V_{DD} to bring the analog die into Test mode. In Test mode, the Reset Timeout (80 ms) is disabled and the LIN receiver is disabled

NOTE: After detecting a RESET (internal or external), the PSON bit needs to be set within 80 ms. If not the device will automatically enter sleep mode.

MCU TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or can be connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance, the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

CONTROL & INTERFACE:

HALL SENSOR INTERFACE

This interface can be configured to support an input pin as a general purpose input, or as a hall-effect sensor input to be able to read 3-pin / 2-pin hall sensors or switches.

SPI INTERFACE & PWM CONTROL

The SPI and PWM interfaces are mastered by the core IC (CPU), and are used to control the output functions of the Analog IC, as well as to report status and failure information of the Analog IC.

LIN INTERFACE

The LIN interface function supports the single wire bus transmit and receive capabilities. It is suited for automotive bus systems, and is based on the LIN bus/physical layer specification. The LIN driver is a low side MOSFET with slope control, internal current limitation, and thermal shutdown.

ANALOG MULTIPLEXER

To be able to have different sources for the MCU with one single signal, an analog multiplexer is integrated in the analog IC. This multiplexer has eleven different sources on the Analog IC, which can be selected with the SS[3:0] bits (through SPI communication) in the A0MUCTL register.

ANALOG INPUT W/INTEGRATED CURRENT SOURCE

The A0 pin provides a switchable current source to allow the reading of switches, NTC, etc., without the need for an additional supply line for the sensor (single wire). There are four different selectable current source values.

OUTPUTS:

HIGH SIDE DRIVERS & DIAGNOSTICS

The HS outputs are low $R_{DS(ON)}$ high side switches. Each HS switch is protected against over-temperature and over-current. The output is capable of limiting the inrush current with an automatic PWM, or feature a real PWM capability using the PWM input.

H-BRIDGE DRIVERS & DIAGNOSTICS

The device includes power MOSFETs configured as four half-bridge driver outputs. These outputs are short-circuit and over-temperature protected. Over-current protection is done on both high side and low side MOSFETs.

ELECTROCHROME GLASS DRIVER & DIAGNOSTICS

The driver provides a controlled voltage, in order to adjust the transparency of an electrochrome glass, and to control the reflection of a rear view mirror. The value of the voltage can be adjusted by the use of an on-chip DA converter.

MM68HC908EY16 CORE IC -

M68HC08 CPU W/ALU, RAM, FLASH ROM

This possesses the functionality of the CPU08 architecture, along with 512 bytes of RAM and 15,872 bytes of FLASH memory, with in-circuit programming.

POWER MODULE W/P0WER-ON-RESET

This block of circuitry manages the power supplied to the core IC, as well as providing POR, LVI, Watchdog timer, and MCU supervision circuitry (COP).

INTERNAL CLOCK MODULE

This module provides the clocks needed by the core IC functions, without the need for external components. Software selectable bus frequencies are available. It also provides a clock monitor function.

10-BIT ADC MODULE

This module provides an 8-channel, 10-bit successive approximation analog-to-digital converter (ADC).

I/O PORTS A, B, C, D, E

There are many I/O pins that are controlled by the CPU through the several I/O ports of the core IC.

TIMER MODULES

There are two 16-bit, 2 channel timer interface modules with selectable input capture, output compare, and PWM capabilities for each channel.

COMMUNICATION MODULES

There are several communication functions supported by the core IC, including an enhanced serial communication interface module (ESCI) for the LIN communication, and an SPI module for inter-IC communication.

RESET & IRQ

There are interrupt and reset connections between the Analog IC and the core IC, for concise control and error/ exception management.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E622 ANALOG DIE MODES OF OPERATION

The 908E622 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

The different modes can be selected by the STOP and SLEEP bits in the System Control Register.

Figure 11 describes how transitions are done between the different operating modes, and Table 6, page 27 gives an overview of the operating modes.

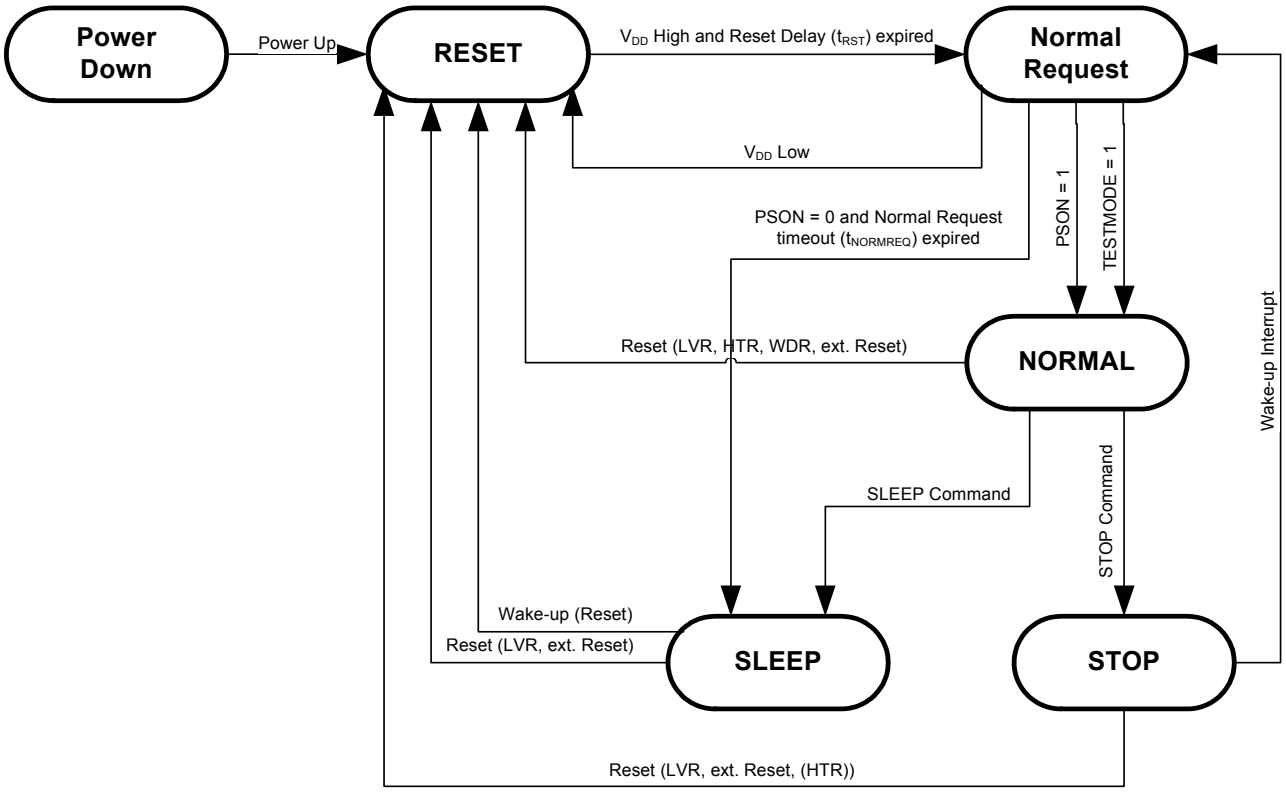


Figure 11. Operating Modes and Transitions

Normal Mode

This Mode is normal operating mode of the device. All functions and power stages are active and can be enabled/disabled. The voltage regulator provides the +5.0 V V_{DD} to the MCU.

After a reset (e.g. Power On Reset, Wake-up from Sleep), the MCU sets the PSON bit in the System Control Register within 80 ms typical ($t_{NORMREQ}$). This is to ensure the MCU has started up and is operating correctly. If the PSON bit is not set within the required time frame, the device enters SLEEP mode to reduce power consumption (fail safe).

This MCU monitoring can be disabled, e.g. for programming by applying V_{DD} on the TESTMODE pin.

Stop Mode

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability). To enter the Stop mode, the STOP bit in the System Control Register has to be set and the MCU has to be stopped (see the 908EY16 datasheet for details).

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0, and is maskable with the LINIE and/or L0IE bits in the Interrupt Mask Register. The analog die is generating an interrupt on $\overline{IRQ\_A}$ pin to wake-up the MCU. The wake-up / interrupt source can be evaluated with the L0IF and LINIF bits in the Interrupt Flag Register.

Stop mode has a higher current consumption than Sleep mode, but allows a quicker wake-up. Additionally, the wake-

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-up Capabilities	$\overline{\text{RST\_A}}$ Output	MCU monitoring/ Watchdog Function	Power Stages	LIN Interface
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Disabled
Normal Request	V_{DD} ON	N/A	HIGH	$t_{NORMREQ}$ (80 ms typical) time out to set PSON bit in System Control Register	Disabled	Disabled
Normal (Run)	V_{DD} ON	N/A	HIGH	Window Watchdog active if enabled	Enabled	Enabled
Stop	V_{DD} ON with limited current capability	LIN wake-up, L0 state change (SPI PSON=1)(33)	HIGH	Disabled	Disabled	Recessive state with wake-up capability
Sleep	V_{DD} OFF	LIN wake-up L0 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability

Notes

33. The SPI is still active in Stop mode. However, due to the limited current capability of the voltage regulator in Stop mode, the PSON bit has to be set before the increased current caused from a running MCU causes an LVR.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 datasheet.

INTERRUPTS

The 908E622 has seven different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ pin is generated to report an event or fault to the MCU. All interrupts are maskable and can be enabled/disabled via the SPI (Interrupt Mask Register). After reset all interrupts are automatically disabled.

Low Voltage Interrupt

Low voltage interrupt (LVI) is related to external supply voltage V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVIF bit in the Interrupt Flag Register. In case the low voltage interrupt is enabled (LVIE = 1), an interrupt will be initiated.

During Sleep and Stop mode the low voltage interrupt circuitry is disabled.

High Voltage Interrupt

The high voltage interrupt (HVI) is related to the external supply voltage V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVIF bit in the Interrupt Flag Register. If the high voltage interrupt is enabled (HVIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HVI circuitry is disabled.

High Temperature Interrupt

The high temperature interrupt (HTI) is generated by the on chip temperature sensors. If the chip temperature is above the HTI threshold, the HTIF bit in the Interrupt Flag Register will be set. If the high temperature interrupt is enabled (HTIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HTI circuitry is disabled.

LIN Interrupt

The LIN Interrupt is related to the Stop mode. If the LIN interrupt is enabled (LINIE = 1) in Stop mode, an interrupt is asserted if a rising edge is detected, and the bus was dominant longer than t_{PROPWL}. After the wake-up / interrupt, the LINIF is indicating the reason for the wake-up / interrupt.

Power Stage Fail Interrupt

The power stage fail flag indicates an error condition on any of the power stages (see Figure 14, page 28).

In case the power stage fail interrupt is enabled (PSFIE = 1), an interrupt will be initiated if:

During Stop and Sleep mode, the PSFI circuitry is disabled.

HO Input Interrupt

The H0 interrupt flag H0IF is set in run mode by a state change of the H0F flag (rising or falling edge on the enabled input). The interrupt function is available if the input is selected as General Purpose, or as 2-pin Hall sensor input. The interrupt is maskable with the H0IE bit in the Interrupt Mask Register.

During Stop and Sleep mode the H0I circuitry is disabled.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP, and a small current source keeps the LIN pin in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

If the LIN interrupt is enabled (LINIE bit in the Interrupt Mask register is set), a dominant level longer than t_{PROPWL} followed by an rising edge will set the LINIF flag and generate an interrupt which causes a system wake-up (see Figure 8, page 18)

SLEEP Mode and Wake-up Feature

During SLEEP mode operation, the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP. A small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by an rising edge will generate a system wake-up (reset), and set the LINWF flag in the Reset Status register (RSR). Also see Figure 9, page 18).

A0 INPUT AND ANALOG MULTIPLEXER

A0 - Analog Input

Input A0 is an analog input used for reading switches or as analog inputs for potentiometers, NTC, etc.

A0 is internally connected to the analog multiplexer. This pin offers a switchable current source. To read the Analog Input the pin, it has to be selected with the SS[3:0] bits in the A0MUCTL register.

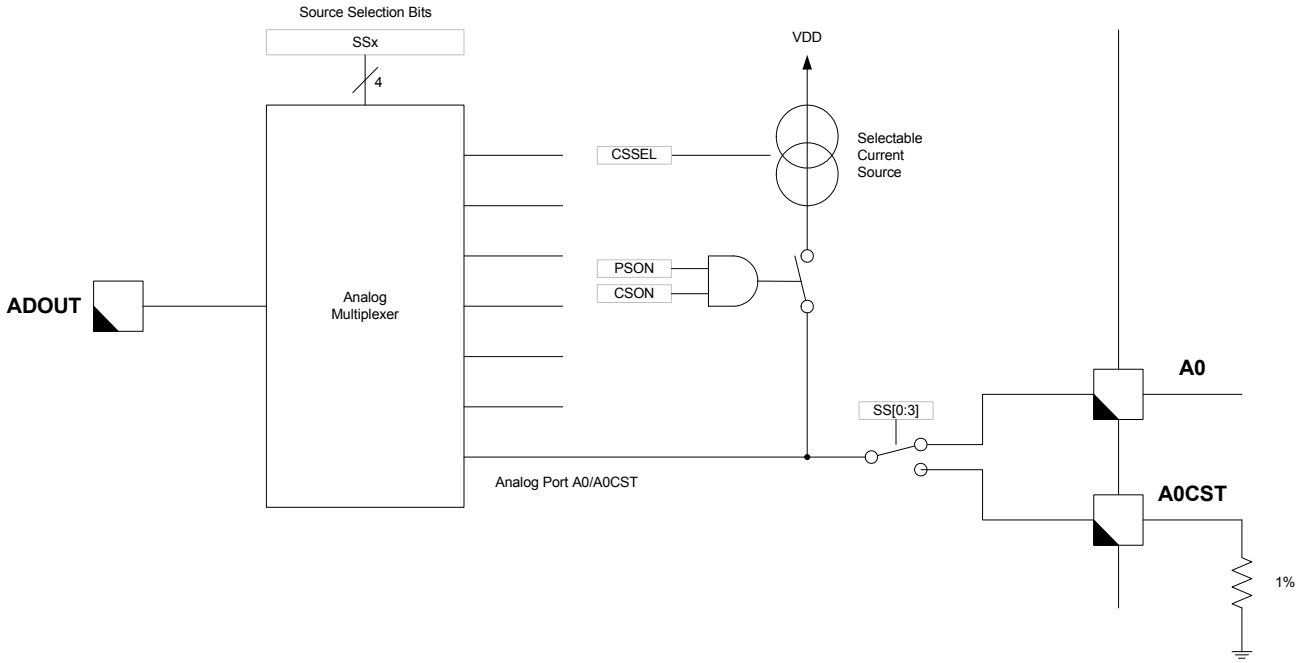


Figure 17. Analog Input and Multiplexer

A0 Current Source

The pin A0 provides a switchable current source, to be able to read in switches, NTC, etc., without the need of an additional supply line for the sensor. The overall enable of this feature is done by setting the PSON bit in the System Control register. In addition, the pin has to be selected with the SS[3:0] bits. The current source can be enabled with the CSON Bit, and adjusted with the bits CSSEL[1:0].

The CSSEL[1:0] bit's four different current values can be selected (40, 120, 320 and 800µA). This function is halted during STOP and SLEEP mode operations.

The current source is derived from the V_{DD} voltage and is constant up to an output voltage of ~4.75 V.

Table 8. Analog Multiplexer Configuration Bits

SS3	SS2	SS1	SS0	Channel
0	1	0	1	current recopy HS2
0	1	1	0	current recopy HS3
0	1	1	1	not used
1	0	0	0	Chip temperature
1	0	0	1	VSUP prescaler
1	0	1	0	Pin A0
1	0	1	1	Pin A0CST

Table 8. Analog Multiplexer Configuration Bits

SS3	SS2	SS1	SS0	Channel
1	1	0	0	Pin EC
1	1	0	1	not used
1	1	1	0	not used
1	1	1	1	not used

Hall-Effect Sensor Input Pin H0

The H0 pin can be configured as general purpose input (H0MS = 0), or as hall-effect sensor input (H0MS = 1), to be able to read 3-pin / 2-pin hall sensors or switches.

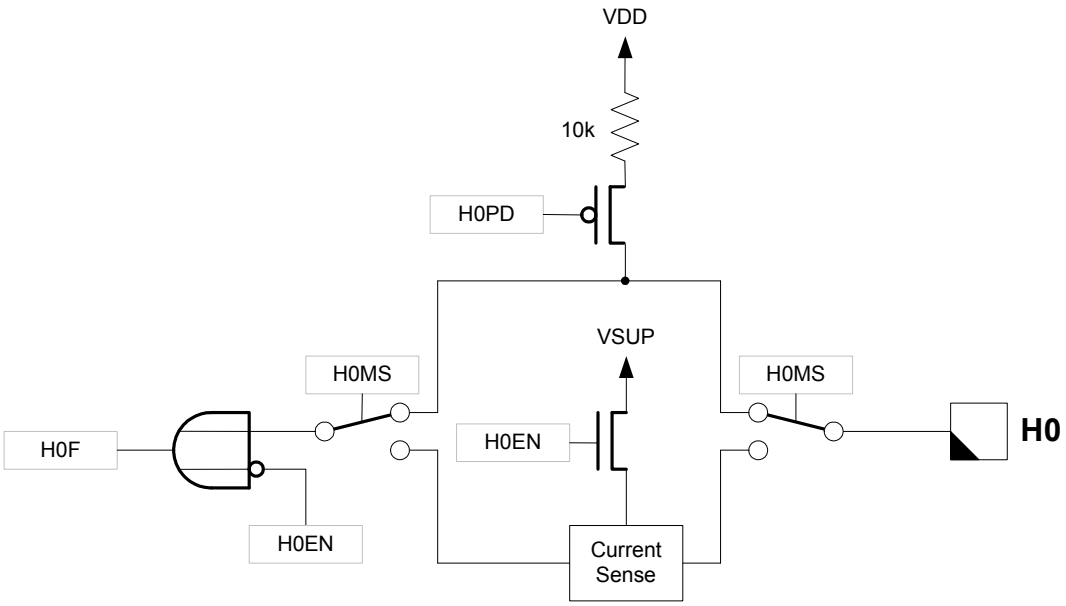


Figure 18. General Purpose / Hall-effect Sensor Input (H0)

Current Coded Hall sensor Input

H0 is selected as “2-pin Hall sensor input”, if the corresponding H0MS bit in the H0/L0 Status and Control Register (HLSCTL) is set. In this mode, the pin current to GND is monitored by a special sense circuitry. Setting the H0EN bit in the H0/L0 Status and Control Register, switches the output to VSUP and enables the sense circuitry. The result of the sense operation is given by the H0F flag. The flag is low if the sensed current is higher than the sense current threshold I_{HSCT}. In this configuration, the HO pin is protected (current limitation) against a short circuit to GND.

After switching on the hallport (H0EN = “1”), the Hall sensor needs some time to stabilize the output. In RUN mode, the software has to take care about waiting for a few µs (40) before sensing the hallflags.

The hallport output current is sensed. In case of an over-current (short to GND), the hallport over-current flag (H0OCF) is set and the current is limited. For proper operation of the current limitation, an external capacitor (>100 nF) close to the H0 pin is required.

Table 15. HVDD Over-current Shutdown Selection Bits

HVDDT1	HVDDT0	typical Delay
0	0	950µs
0	1	536µs
1	0	234µs
1	1	78µs

ITRIM3:0 - IRef Trim Bits

These write only bits are for trimming the internal current references IRef (also A0, A0CST). The provided trim values have to be copied into these bits after every reset. Reset clears the ITRIM3:0 bits.

Table 16. IRef Trim Bits

itrim3	itrim2	itrim2	itrim0	Adjustment
0	0	0	0	0
0	0	0	1	2%
0	0	1	0	4%
0	0	1	1	8%
0	1	0	0	12%
0	1	0	1	-2%
0	1	1	0	-4%
0	1	1	1	-8%
1	0	0	0	-12%

System Trim Register 2 (SYSTRIM2)

Register Name and Address: IFBHBTRIM - $10

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
Reset	0	0	0	0	0	0	0	0

CRHBHC1:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB1 and HB2 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC1:0 bits.

Table 17. Current Recopy Trim for HB1:2 (CSA=0)

CRHBHC1	CRHBHC0	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHB5:3 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB5:3 bits.

Table 18. Current Recopy Trim for HB3:4 (CSA=1)

CRHB5	CRHB4	CRHB3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHB2:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming of the current recopy of the half-bridge HB1 and HB2 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB2:0 bits.

Table 19. Current Recopy Trim for HB1:2 (CSA=1)

CRHB2	CRHB1	CRHB0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

System Trim Register 3 (SYSTRIM3)

Register Name and Address: IFBHSTRIM - $11

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0
Reset	0	0	0	0	0	0	0	0

CRHBHC3:2 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming the current recopy of the half-bridge HB3 and HB4 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC3:2 bits.

Table 20. Current Recopy Trim for HB3:4 (CSA=0)

CRHBHC3	CRHBHC2	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHS5:3 - Current Recopy HS2:3 Trim Bits

These write only bits are for trimming the current recopy of the high side HS2 and HS3. The provided trim values have to be copied into these bits after every reset. Reset clears the CRHS5:3 bits.

Table 21. Current Recopy Trim for HS2:3

CRHS5	CRHS4	CRHS3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHS2:0 - Current Recopy HS1 Trim Bits

These write only bits are for trimming the current recopy of the high side HS1. The provided Trim values have to be copied into these bits after every reset. Reset clears the CRHS2:0 bits.

Table 22. Current Recopy Trim for HS1

CRHS2	CRHS1	CRHS0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E622 has the MC68HC908EY16 MCU embedded, typically all the development tools available for the MCU also apply for this device. However, due to the additional analog die circuitry and the nominal +12 V supply voltage, some additional items have to be considered:

- nominal 12 V rather than 5.0 or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin
- MCU monitoring (Normal request timeout) has to be disabled

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process, first on chip level, before the IC is soldered onto a pcb board, and second after the IC is soldered onto the pcb board.

Chip Level Programming

At the Chip level, the easiest way is to only power the MCU with +5.0 V (see Figure 32), and not to provide the analog chip with VSUP. In this setup, all the analog pins should be left open (e.g. VSUP[1:8]), and interconnections between the MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

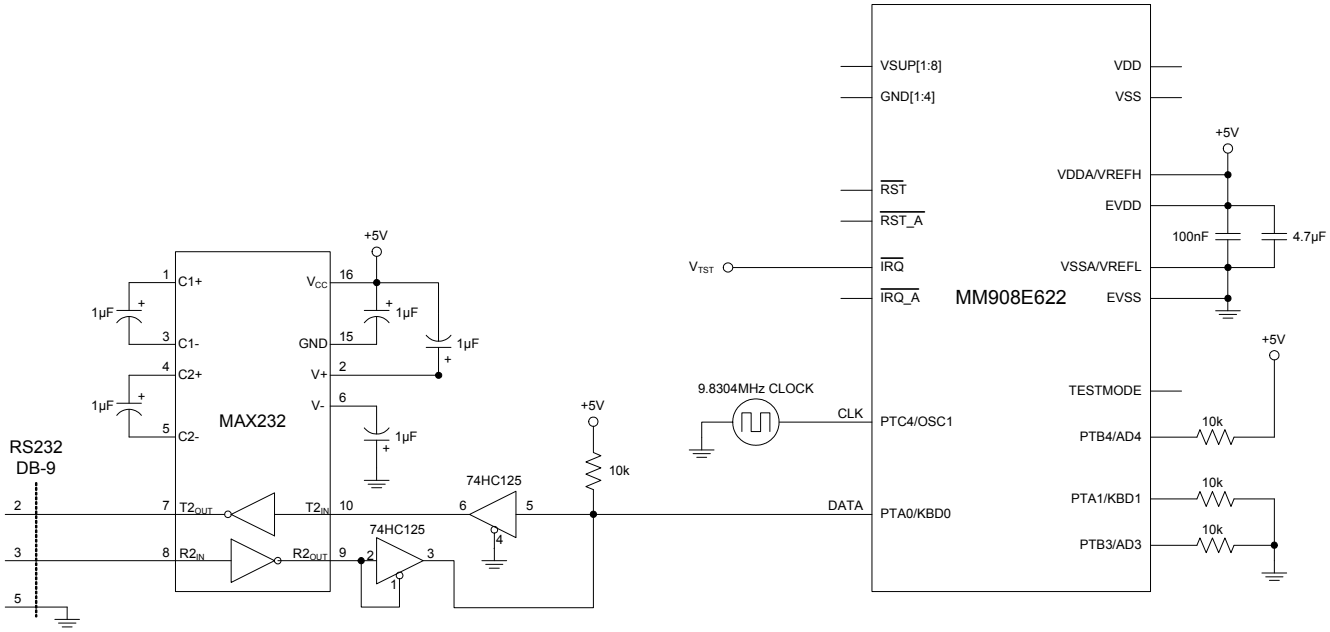
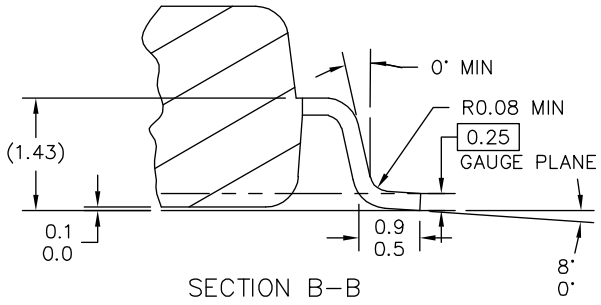


Figure 32. Normal Monitor Mode Circuit (MCU only)

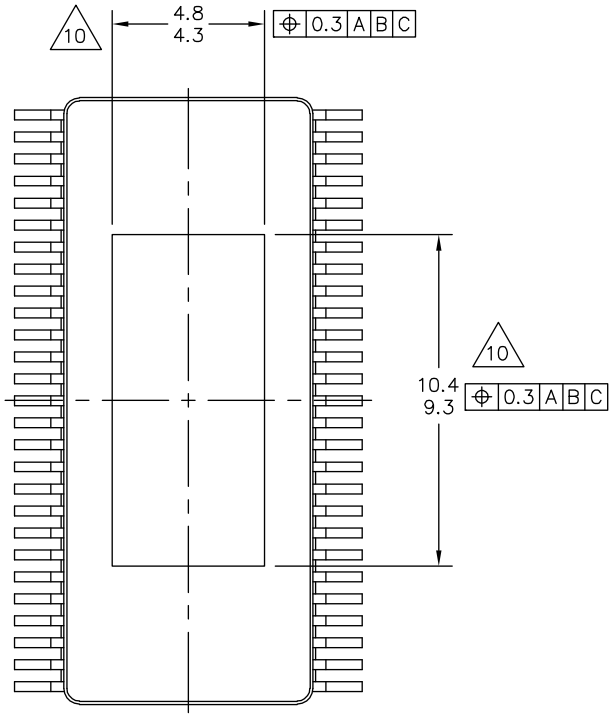
Of course its also possible to supply the whole system with V_{SUP} instead (12 V), as described in Figure 33, page 53.

PCB Level Programming

If the IC is soldered onto the pcb board, its typically not possible to separately power the MCU with +5.0 V. The whole system has to be powered up and providing V_{SUP} (see Figure 33).



SECTION B–B



VIEW C–C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D	REV: O
	CASE NUMBER: 1823–01	17 NOV 2005
	STANDARD: NON–JEDEC	

EK SUFFIX (Pb-free)
54-PIN SOICW-EP
98ASA10712D
ISSUE 0

908E622

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS DEFINE THE PRIMARY SOLDERABLE SURFACE AREA.

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TITLE: 54LD SOIC W/B, 0.65 PITCH 4.5 X 9.8 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10712D	REV: O
	CASE NUMBER: 1823–01	17 NOV 2005
	STANDARD: NON–JEDEC	

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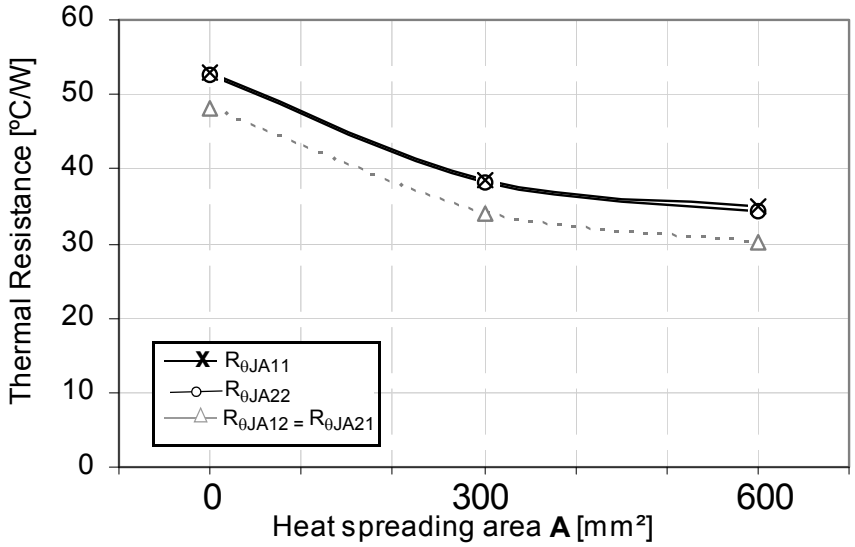

Figure 38. Device on Thermal Test Board $R\theta_{JA}$

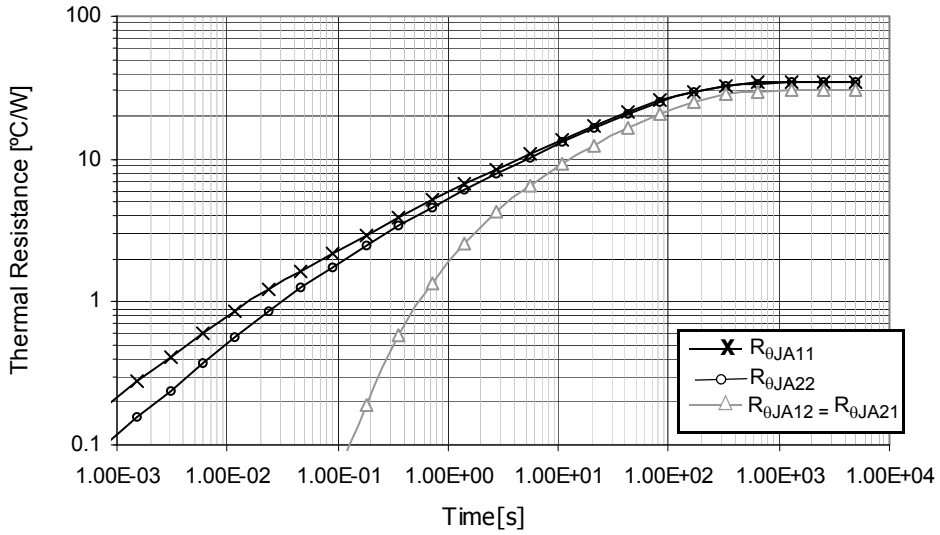

Figure 39. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 ($mm^{2)}$