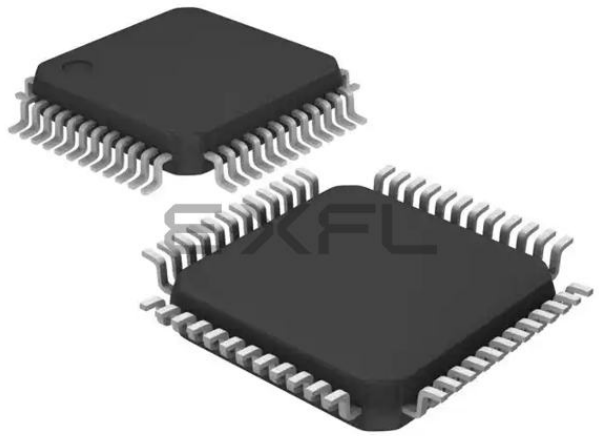

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	42
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058slan

LIST OF TABLES

- Multiple clock sources
- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected

- WWDT (Window Watchdog Timer)
  - 6-bit down counter with 11-bit prescale for wide range window selected
- PWM
  - Up to two built-in 16-bit PWM generators, providing four PWM outputs or two complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
  - Additional functions
    - Internal 10 kHz to PWM clock source
    - Polar inverse function
    - Center-aligned type function
    - Timer duty interrupt enable function
    - Two kinds of PWM interrupt period/duty type selection
    - Period/duty trigger ADC function
- UART
  - Programmable baud-rate generator
  - Buffered receiver and transmitter, each with 16 bytes FIFO
  - Optional flow control function (CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS485 function
  - Supports LIN function
- SPI
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Provides 3 wire function
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Supports Byte Suspend mode in 32-bit transmission
  - Additional functions
    - PLL clock source
    - 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode
- I^2C
  - Up to two sets of I2C device
  - Supports master/slave mode
  - Bidirectional data transfer between master and slave
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via

4.2.2 QFN 33-pin

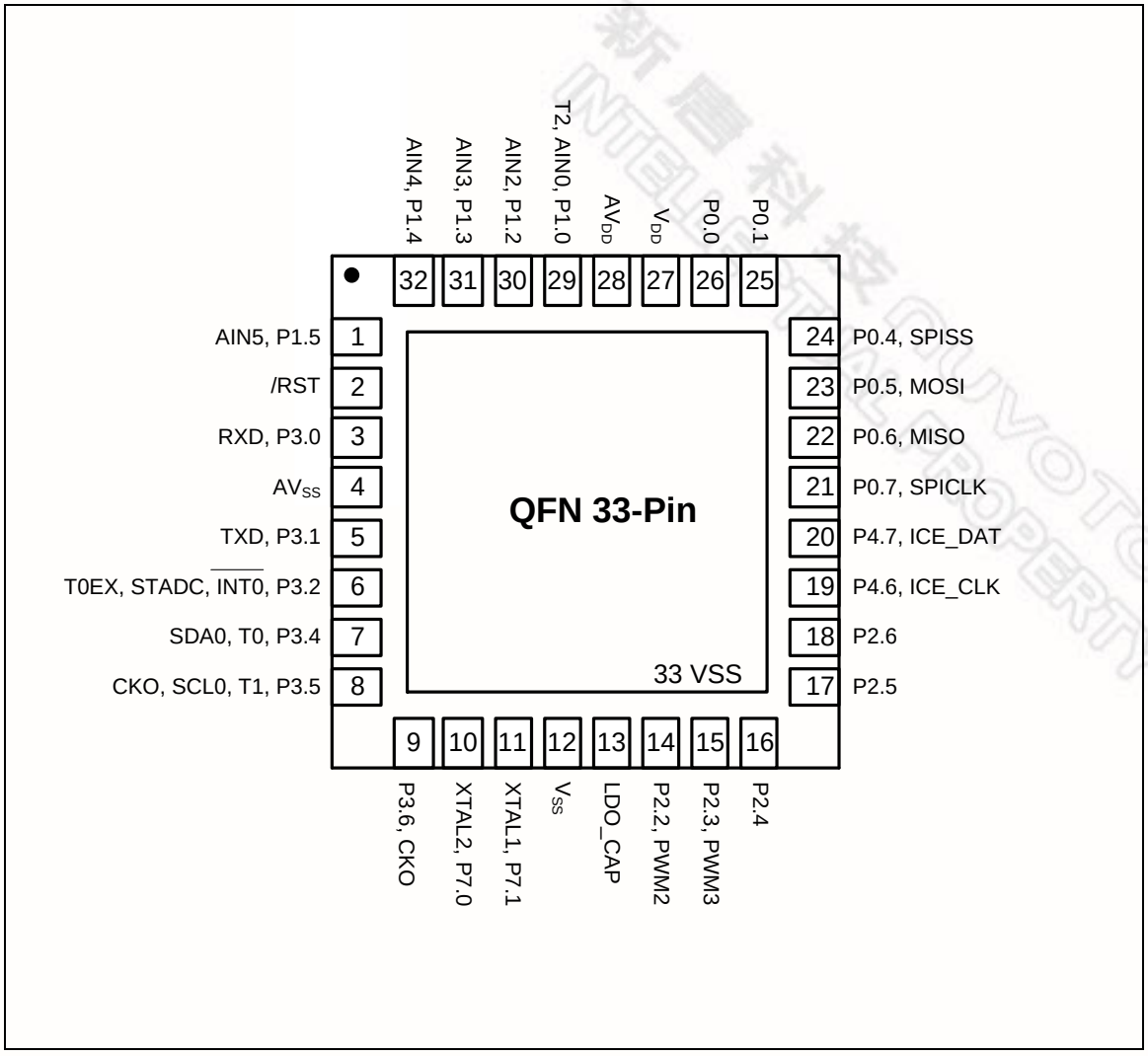


Figure 4.2-2 NuMicro™ M058S Series QFN-33 Pin Diagram

4.2.3 LQFP 48-pin

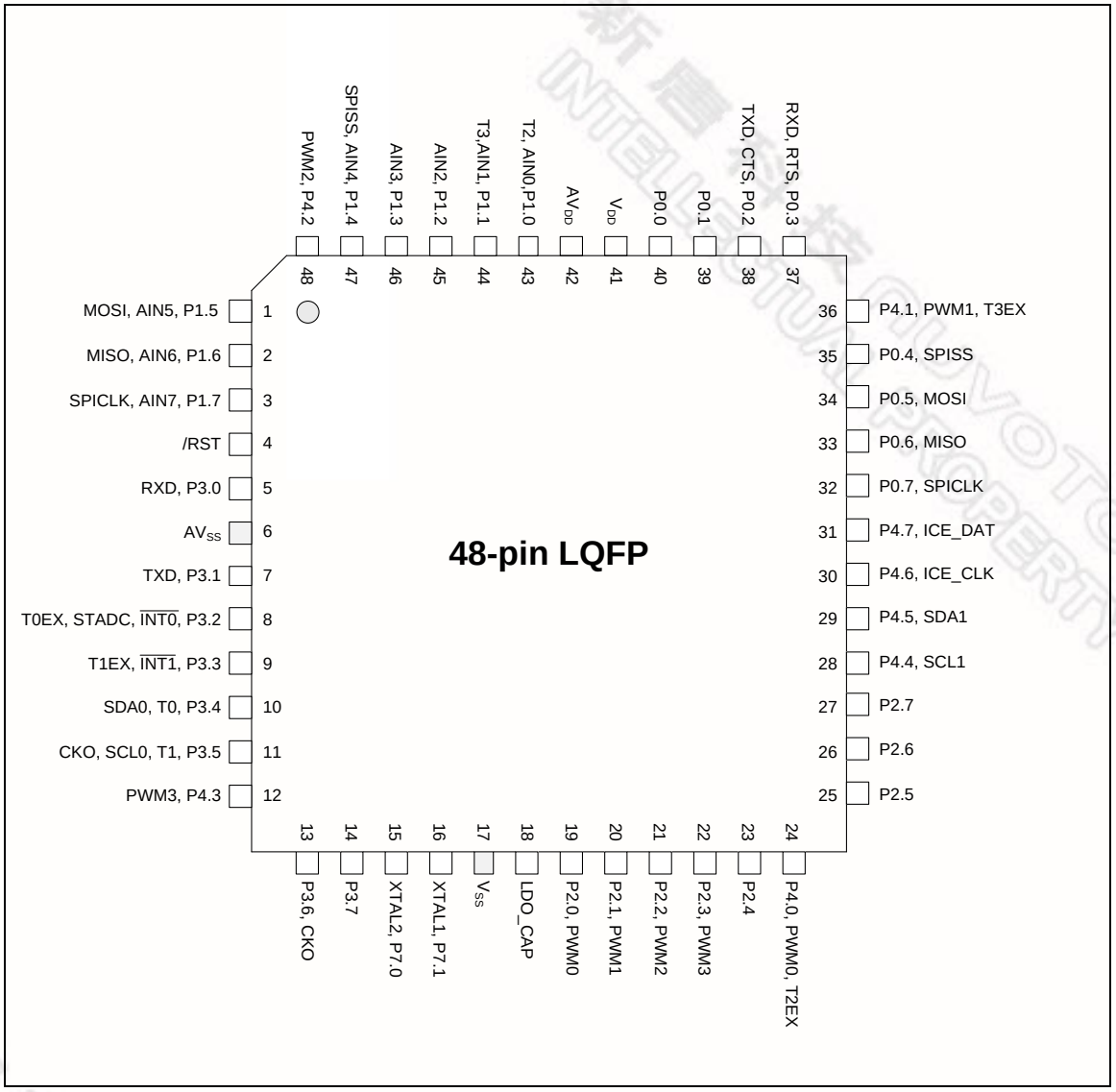


Figure 4.2-3 NuMicro™ M058S Series LQFP-48 Pin Diagram

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
17	22	33	45	P0.6	MISO[2]			I/O	for UART RTS: Request to Send output pin for UART The RXD/TXD pins are for UART function use.
16	21	32	44	P0.7	SPICLK[2]			I/O	
1	29	43	59	P1.0	T2	AIN0		I/O	**PORT1:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T2, T3, SPISS0, MOSI, MISO, and SPICLK. The pins SPISS0, MOSI, MISO, and SCLK are for the SPI function use. The pins AIN0~AIN7 are for the 12 bits ADC function use. The T2/T3 pins are for Timer2/3 external event counter input.
	NC	44	60	P1.1	T3	AIN1		I/O	
	30	45	61	P1.2		AIN2		I/O	
	31	46	62	P1.3		AIN3		I/O	
2	32	47	63	P1.4	SPISS[2]	AIN4		I/O	
	1	1	1	P1.5	MOSI[2]	AIN5		I/O	
	NC	2	2	P1.6	MISO[2]	AIN6		I/O	
	NC	3	3	P1.7	SPICLK[2]	AIN7		I/O	
	NC	19	27	P2.0	PWM0[2]			I/O	**PORT2:** General purpose I/O port, which can be configured by software in four modes. It has an alternative function. The pins PWM0~PWM3 are for the PWM function use.
	NC	20	28	P2.1	PWM1[2]			I/O	
	14	21	29	P2.2	PWM2[2]			I/O	
13	15	22	30	P2.3	PWM3[2]			I/O	
	16	23	31	P2.4				I/O	
	17	25	33	P2.5				I/O	
	18	26	34	P2.6				I/O	
	NC	27	35	P2.7				I/O	
4	3	5	5	P3.0	RXD[2]			I/O	**PORT3:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for RXD, TXD, /INT0, /INT1, T0 and T1. The RXD/TXD pins are for
6	5	7	10	P3.1	TXD[2]			I/O	
	6	8	11	P3.2	/INT0	STADC	T0EX	I/O	
	NC	9	12	P3.3	/INT1		T1EX	I/O	

5 BLOCK DIAGRAM

5.1 NuMicro™ M058S Block Diagram

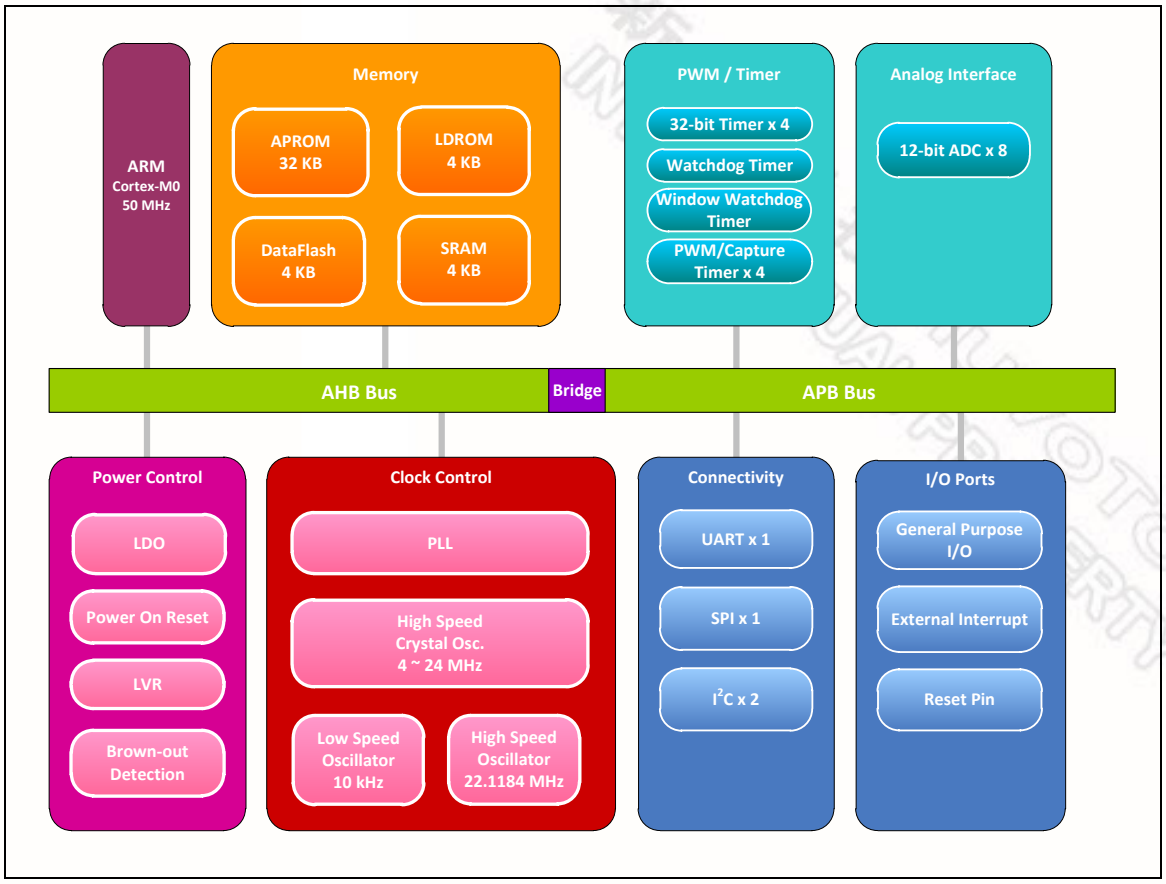


Figure 5.1-1 NuMicro™ M058S Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

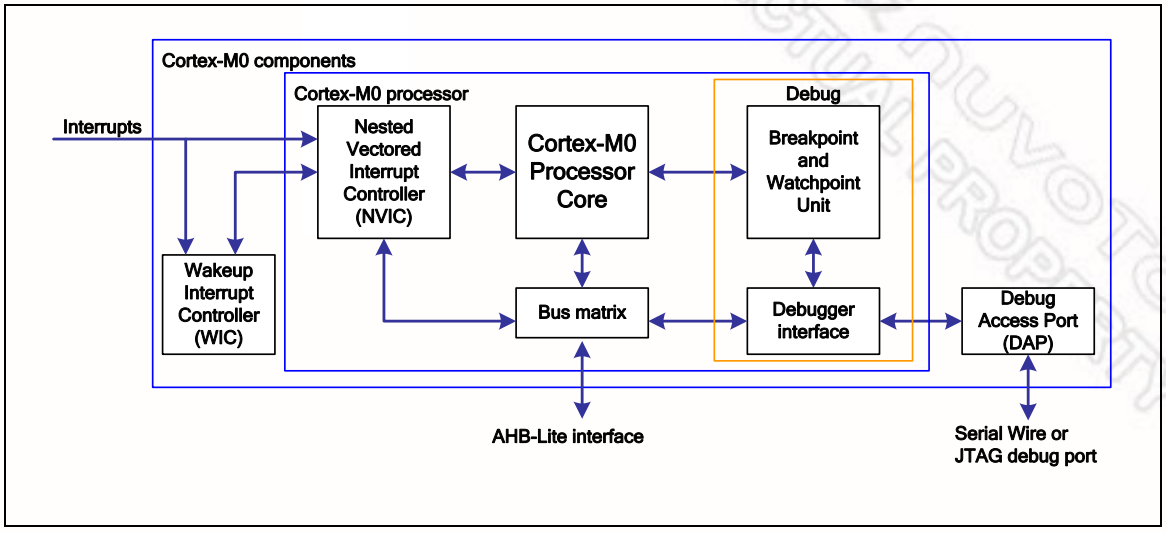


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- **A low gate count processor the features:**
  - The ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - ARMv6-M compliant 24-bit SysTick timer.
  - A 32-bit hardware multiplier.
  - The system interface supports little-endian data accesses.
  - The ability to have deterministic, fixed-latency, interrupt handling.
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
  - C Application Binary Interface compliant exception model.
    This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset Pin (nRST)
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.3 System Power Architecture

In this device, the power architecture is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8 V power for digital operation.

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the M058S series.

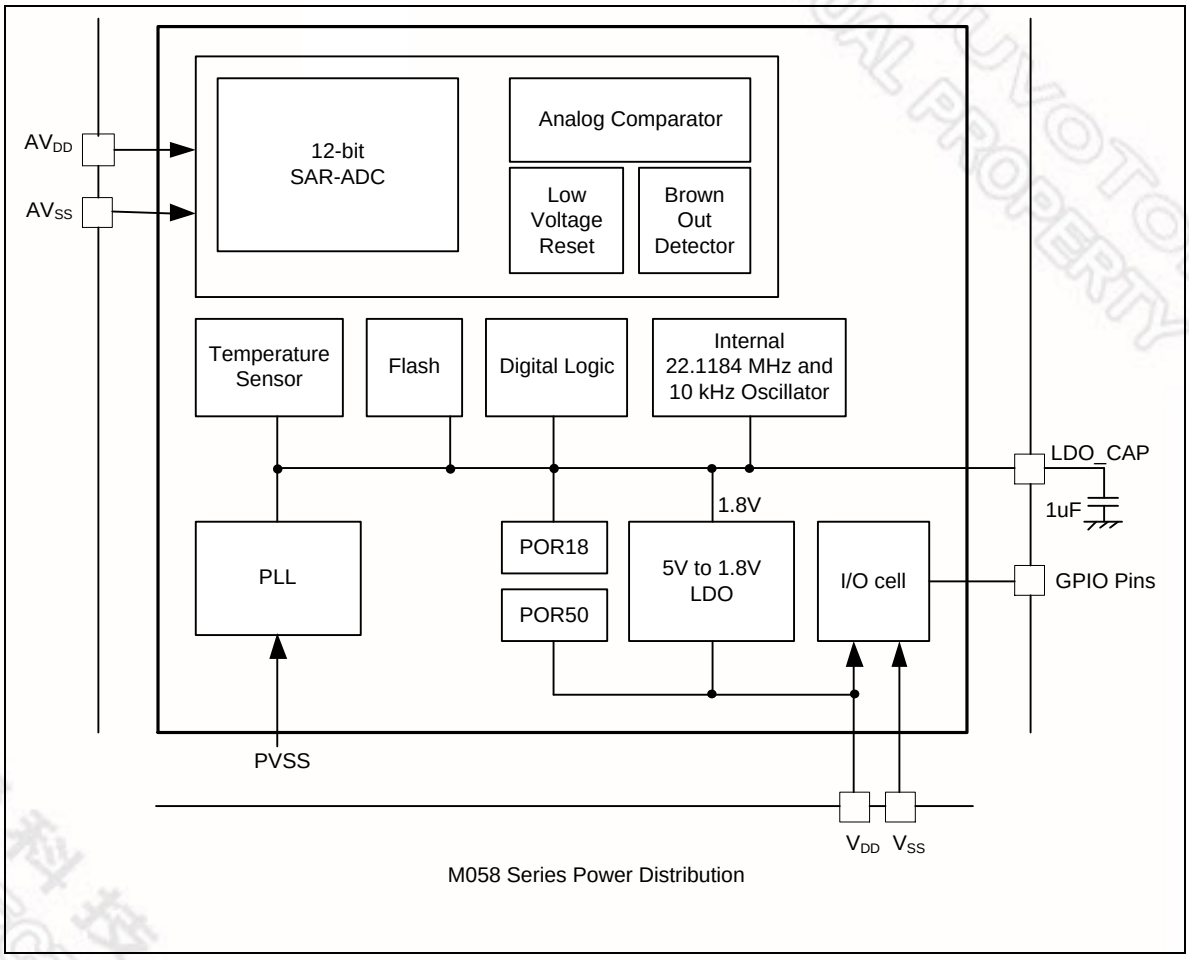


Figure 6.2-1 NuMicro™ M058S Power Architecture Diagram

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-4 Vector Figure Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

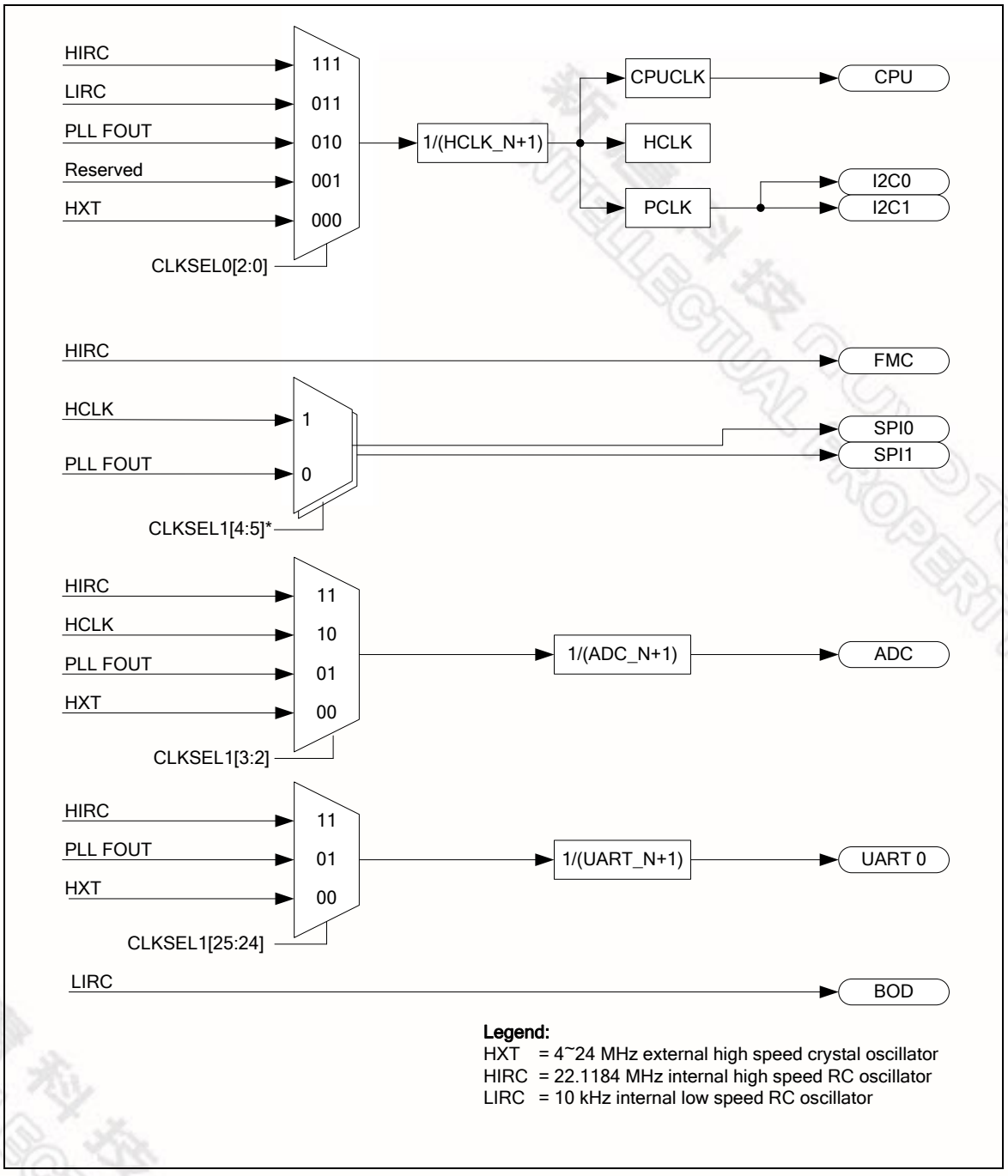
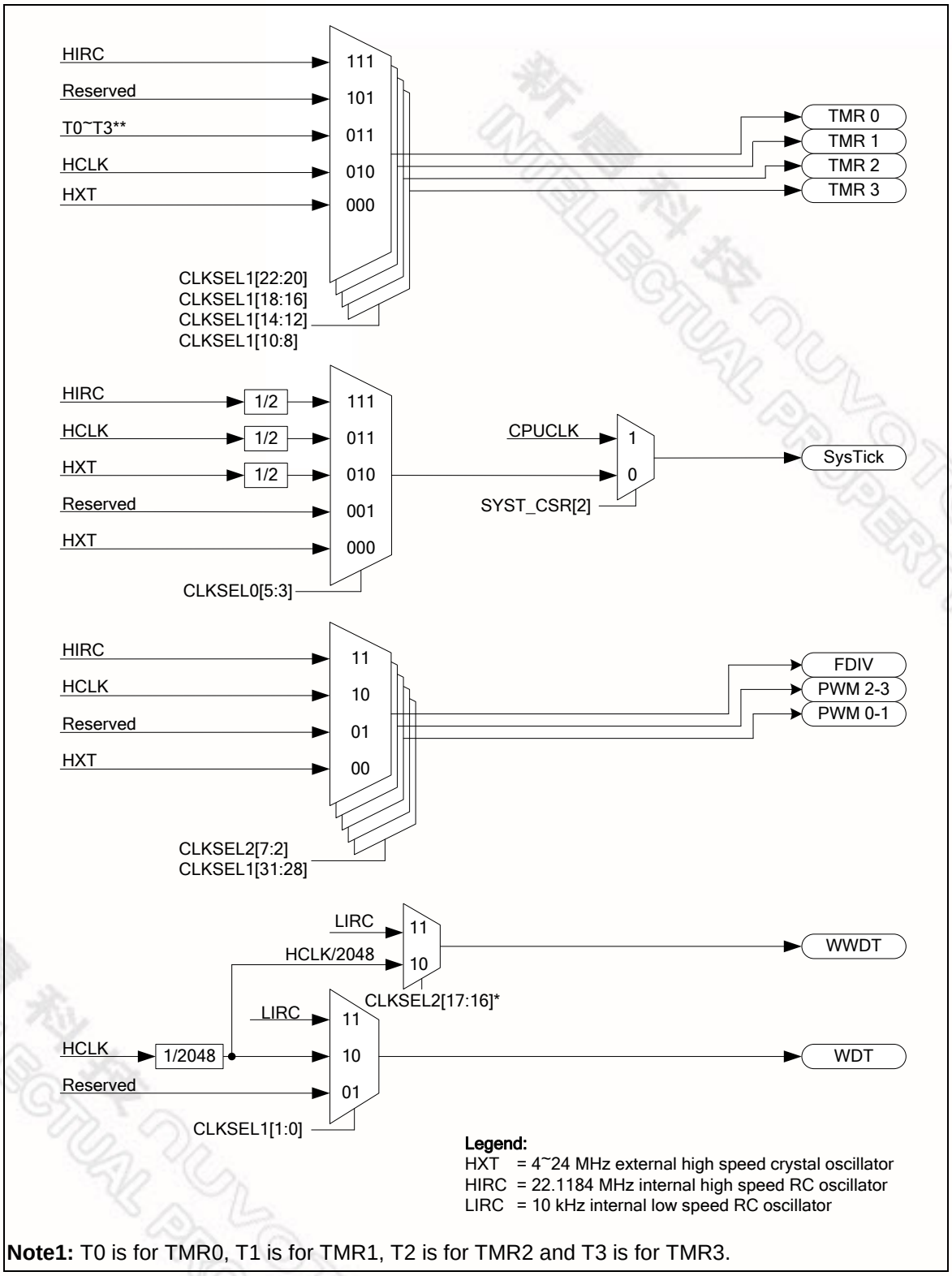


Figure 6.3-2 Clock Source Controller Overview (1/2)



Note1: T0 is for TMR0, T1 is for TMR1, T2 is for TMR2 and T3 is for TMR3.

Figure 6.3-3 Clock Source Controller Overview (2/2)

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The M058S Series are equipped with 64/32/16/8 KB on chip embedded Flash memory for application program (APROM) that can be updated through ISP registers. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, it also provides additional 4 KB DATA Flash for user to store some application depended data before chip power off in 64/32/16/8 KB APROM model.

It provides more settings in CONFIG0 to support more advanced functions, including power-on with tri-state I/O, default to enable WDT after booting, enable WDT in Power-down mode, and IAP functions. The following table shows the added functions of M058S Series.

	M058S Series
CONFIG[6]	To support IAP function and Multi-Boot function
CONFIG[10]	Select I/O state after booting
CONFIG[30]	To support WDT in Power-Down mode when WDT is default on after booting
CONFIG[31]	To support WDT default on after booting

Table 6.4-1 M058S Series Function Difference List (FMC)

6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- 32 KB application program memory (APROM)
- 4 KB in system programming (ISP) loader program memory (LDROM)
- Fixed 4 KB Data Flash
- All embedded flash memory supports 512 bytes page erase

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

There are 58 General Purpose I/O pins shared with special feature functions in this MCU. The 58 pins are arranged in 9 ports named with P0, P1… to P7. Each port equips maximum 8 pins except P7[1:0]. Each one of the 58 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be software configured individually as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} which is from 5.0V to 2.5V.

6.5.2 Features

- Four I/O modes:
  - Input only with high impedance
  - Push-pull output
  - Open-drain output
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- Configurable default I/O mode of all pins after reset by CIOINI(CONFIG[10]) setting
  - CIOINI = 0, all GPIO pins in Input tri-state mode after chip reset
  - CIOINI = 1, all GPIO pins in Quasi-bidirectional mode after chip reset

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD} –V_{SS}	-0.3	+7.0	V
Input Voltage	VIN	V_{SS}-0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

Operating Current Normal Run Mode @ 4 MHz	IDD13		3.4		mA	V_{DD} = 5.5V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD14		2.6		mA	V_{DD} = 5.5V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
	IDD15		2.0		mA	V_{DD} = 3.3V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD16		1.3		mA	V_{DD} = 3.3V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
Operating Current Normal Run Mode @10 KHz	IDD17		98.7		uA	V_{DD} = 5.5V@ 10 KHz, enable all peripherals and IRC10 KHz, disable PLL
	IDD18		97.4		uA	V_{DD} = 5.5V@ 10 KHz, disable all peripherals and enable IRC 10KHz, disable PLL
	IDD19		86.4		uA	V_{DD} = 3.3V@ 10 KHz, enable all peripherals and IRC 10 KHz, disable PLL
	IDD20		85.2		uA	V_{DD} = 3.3V@ 10 KHz, disable all peripherals and enable IRC 10 KHz, disable PLL
Operating Current Idle Mode @ 50 MHz	IIDLE1		16.2		mA	V_{DD} = 5.5V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE2		10.0		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IIDLE3		14.6		mA	V_{DD} = 3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE4		8.5		mA	V_{DD} = 3V@50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 22 MHz	IIDLE5		4.3		mA	V_{DD} = 5.5V@ 22MHz, enable all peripherals and IRC 22MHz, disable PLL
	IIDLE6		1.5		mA	V_{DD} =5.5V@ 22MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
	IIDLE7		4.2		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IIDLE8		1.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22MHz, disable PLL
Operating Current Idle Mode @ 12 MHz	IIDLE9		4.3		mA	V_{DD} = 5.5V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12MHz
	IIDLE10		2.6		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12MHz

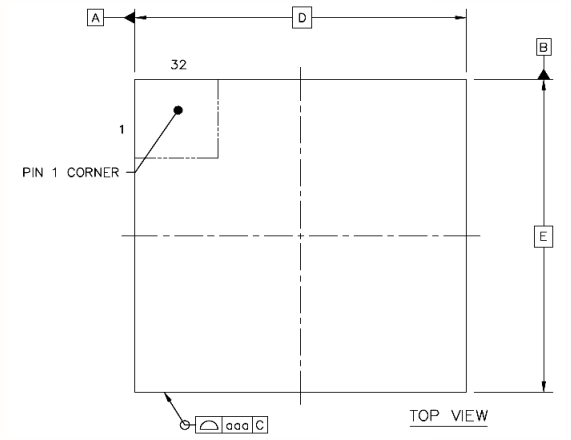
7.4.2 LDO Specification

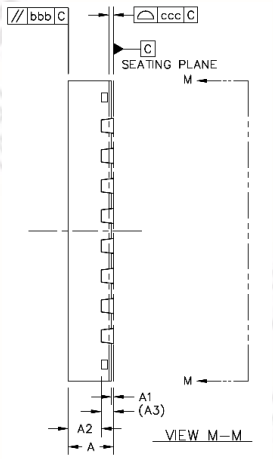
RAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5		5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	℃	
C	-	1	-	uF	Resr=1ohm

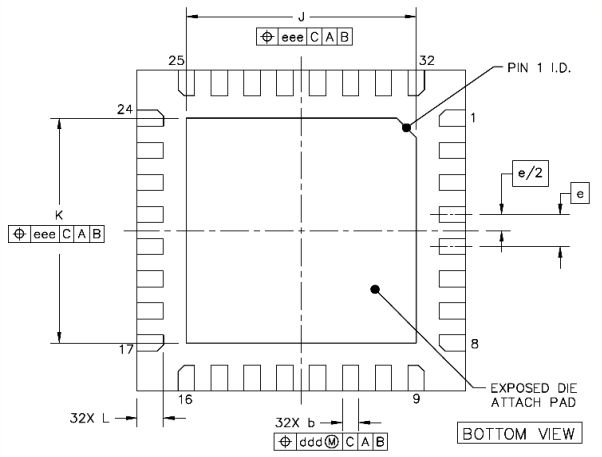
Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

8.2 QFN-33 (5X5 mm^2, Thickness 0.8mm, Pitch 0.5 mm)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	