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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	55
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058ssan

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

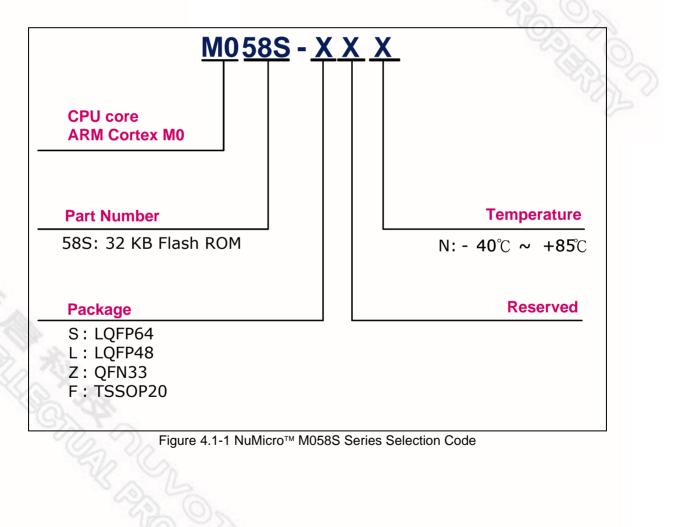
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4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro[™] M058S Series Selection Guide

	Connectivi		vity													
Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	0/1	Timer (32-Bit)	UART	IdS	I²C	PWM (16-bit)	ADC (12-bit)	WDT	WWDT	ISP/ICP/IAP	Package	Operating Temperature Range(୯)
M058SFAN	32	4	4	4	14	4	1	1	1	1	2	\checkmark	\checkmark	\checkmark	TSSOP20	-40 to +85
M058SZAN	32	4	4	4	26	4	1	1	1	2	5	\checkmark	\checkmark	\checkmark	QFN33	-40 to +85
M058SLAN	32	4	4	4	42	4	1	1	2	4	8	\checkmark	\checkmark	\checkmark	LQFP48	-40 to +85
M058SSAN	32	4	4	4	55	4	1	1	2	4	8	\checkmark	\checkmark	\checkmark	LQFP64	-40 to +85

Table 4.1-1 NuMicro™ M058S Series Selection Guide



4.3 Pin Description

	Pin Nu	mber			Alterna	te Funct	ion		
TSSOP 20	QFN 33	LQFP 48	LQFP 64	Symbol	1	2	3	Type ^[1]	Description
19	27	41	21	V _{dd}		7	X.	P	Power supply to I/O ports and LDO source for internal PLL and
			54				13	a.	digital circuit.
11	12	. 17	20	V _{ss}				P	Ground pin for digital circuit.
	33		53						SAL
20	28	42	55	AV_{DD}				Р	Power supply to internal analog circuit.
5	4	6	6	AV _{SS}				Ρ	Analog Ground pin for analog circuit.
	NC	NC	56	V _{ref}				Ρ	Voltage reference input for ADC
				LDO					LDO output pin
12	13	18	22	_CAP				Ρ	Note: This pin needs to be connected with a 1uF capacitor.
3	2	4	4	/RST				l (ST)	/RST pin is a Schmitt trigger input pin for hardware device reset. A " Low " on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
S.	26	40	52	P0.0				I/O	PORT0: General purpose I/O port, which can be configured
S	25	39	51	P0.1				I/O	by software in four modes. Its multifunction pins are for
9	NC	38	50	P0.2	CTS		TXD ^[2]	I/O	CTS1, RTS1, CTS0, RTS0, SPISS, MOSI, MISO, and SPICLK.
	NC	37	49	P0.3	RTS		RXD ^[2]	I/O	The pins SPISS, MOSI, MISO, and SPICLK are for
	24	35	47	P0.4	SPISS ^[2]			I/O	the SPI function use.
18	23	34	46	P0.5	MOSI ^[2]			I/O	CTS: Clear to Send input pin

	Pin Nu	mber			Alterna	ate Functi	on		
TSSOP 20	QFN 33	LQFP 48	LQFP 64	Symbol	1	2	3	Type ^[1]	Description
17	22	33	45	P0.6	MISO ^[2]	V?		I/O	for UART
16	21	32	44	P0.7	SPICLK ^[2]	2	Y	I/O	RTS: Request to Send output pin for UART The RXD/TXD pins are for UART function use.
1	29	43	59	P1.0	T2	AINO		I/O	PORT1: General purpose I/O
	NC	44	60	P1.1	Т3	AIN1		I/O	port, which can be configured by software in four modes. Its multifunction pins are for T2,
	30	45	61	P1.2		AIN2		I/O	T3, SPISS0, MOSI, MISO, and SPICLK.
	31	46	62	P1.3		AIN3		I/O	The pins SPISS0, MOSI, MISO, and SCLK are for the
2	32	47	63	P1.4	P1.4 SPISS ^[2] AIN4 I/O SPI function use.	SPI function use. The pins AIN0~AIN7 are for			
	1	1	1	P1.5	MOSI ^[2]	AIN5		I/O	the 12 bits ADC function use. The T2/T3 pins are for
	NC	2	2	P1.6	MISO ^[2]	AIN6		I/O	Timer2/3 external event counter input.
	NC	3	3	P1.7	SPICLK ^[2]	AIN7		I/O	
	NC	19	27	P2.0	PWM0 ^[2]			I/O	PORT2: General purpose I/O port, which can be configured
	NC	20	28	P2.1	PWM1 ^[2]			I/O	by software in four modes. It has an alternative function.
	14	21	29	P2.2	PWM2 ^[2]			I/O	The pins PWM0~PWM3 are for the PWM function use.
13	15	22	30	P2.3	PWM3 ^[2]			I/O	
	16	23	31	P2.4				I/O	
、龙	17	25	33	P2.5				I/O	
S.	18	26	34	P2.6				I/O	
S	NC	27	35	P2.7				I/O	
4	3	5	5	P3.0	RXD ^[2]			I/O	PORT3: General purpose I/O port, which can be configured
6	5	7	10	P3.1	TXD ^[2]			I/O	by software in four modes. Its multifunction pins are for
	6	8	11	P3.2	/INT0	STADC	T0EX	I/O	RXD, TXD, /INT0, /INT1, T0 and T1.
	NC	9	12	P3.3	/INT1		T1EX	I/O	The RXD/TXD pins are for



5 BLOCK DIAGRAM

5.1 NuMicro™ M058S Block Diagram

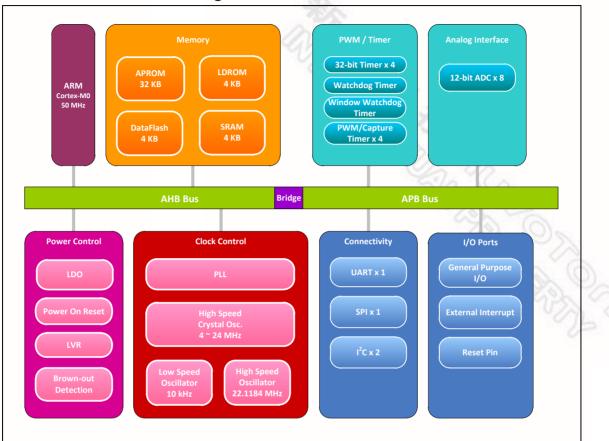


Figure 5.1-1 NuMicro™ M058S Block Diagram

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
 - Power-on Reset (POR)
 - Low level on the Reset Pin (nRST)
 - Watchdog Timer Time-out Reset (WDT)
 - Low Voltage Reset (LVR)
 - Brown-out Detector Reset (BOD)
- Software Reset
 - MCU Reset SYSRESETREQ(AIRCR[2])
 - Cortex-M0 Core One-shot Reset CPU_RST(IPRSTC1[1])
 - Chip One-shot Reset CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

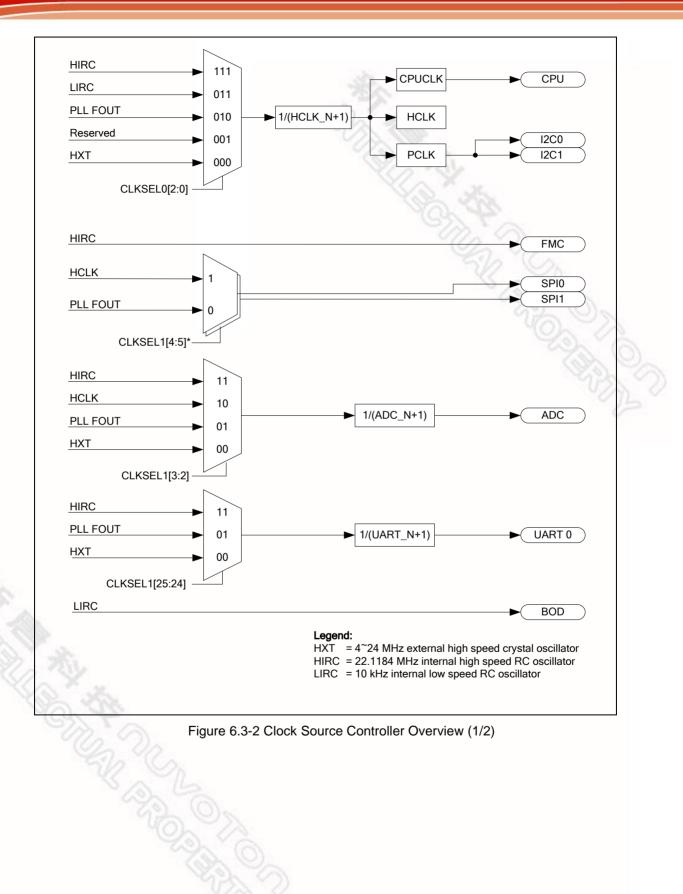


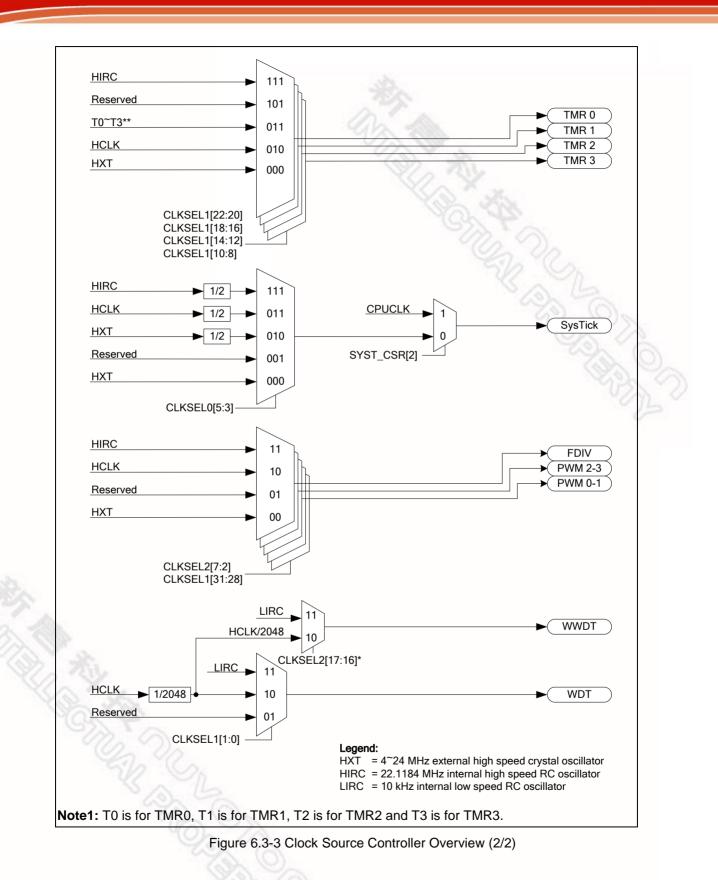


	M058S					
GB		0xFFFF_FFFF				
	Reserved	I		System Control		
		0xE000_F000		System Control Block	0xE000_ED00	SCB_BA
	System Control	0xE000_EFFF		External Interrupt Controller	0xE000_E100	NVIC_BA
	System Control	0×E000_E000		System Timer Control	0xE000_E010	SYST_BA
		0xE000_DFFF		System Control Space	0xE000_E000	SCS_BA
	Reserved	I		•		
		0x6002_0000				
	EBI	0x6001_FFFF				
		0x6000_0000				
		0x5FFF_FFF				
	Reserved	l I		AHB peripherals		
		0x5020_0000		FMC	0x5000_C000	FLASH_BA
	АНВ	0x501F_FFFF		GPIO Control	0x5000_4000	GPIO_BA
	АПБ	0x5000_0000		Interrupt Multiplexer Control	0x5000_0300	INT_BA
		0x4FFF_FFFF	7	Clock Control	0x5000_0200	CLK_BA
				System Global Control	0x5000_0000	GCR_BA
	Reserved					
		0x4020_0000		APB peripherals		
		0x401F_FFFF	- (I2C1 Control	0x4012_0000	I2C1_BA*
		_		Timer2/Timer3 Control		TMR23_BA
	APB	I	◀	ADC Control	0x400E_0000	ADC_BA
GB		0x4000_0000		UART0 Control	0x4005_0000	UART0_BA
		0x3FFF_FFFF	-	PWM0/1/2/3 Control	0x4004_0000	PWMA_BA
				SPI0 Control	0x4003_0000	SPI0_BA
	Reserved	I		I2C Control	0x4002_0000	12C0_BA
		0x2000_1000		Timer0/Timer1 Control	0x4001_0000	TMR01_BA
		0x2000_0FFF	-	WDT Control	0x4000_4000	WDT_BA
				WWDT Control	0x4000_4100	WWDT_BA
	4 KB SRAM	1				
	(M052/M054/M058/M0516)					
5 GB		0x2000_0000				
		0x1FFF_FFFF	-			
	Reserved	I				
		0x0001_0000				
		0x0000_7FFF				
	32 KB on-chip Flash					
GB		0x0000_0000				

6.2.5 Whole System Memory Mapping

See New





6.11 I²C Serial Interface Controller (I²C)

6.11.1 Overview

 I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There are two sets of I^2C which supports Power-down wake up function.

6.11.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I^2C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between master and slave
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down Wake-up function

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V _{DD} –V _{SS}	-0.3	+7.0	V
Input Voltage	VIN	V _{SS} -0.3	V _{DD} +0.3	V
Oscillator Frequency	1/t _{CLCL}	4	24	MHz
Operating Temperature	ТА	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25° C, F_{OSC} = 50 MHz unless otherwise specified.)

 DADAMETED	0)/14		SPECIF	ICATION		TEAT CONDITIONS
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operation voltage	V _{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V _{LDO}	1.7	1.8	1.9	v	$V_{DD} \ge 2.5V$
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V _{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	V _{DD}		V _{DD}	V	C Dr
	IDD1		20.6		mA	$V_{DD} = 5.5V$ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
Operating Current Normal Run Mode	IDD2		14.4		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
@ 50 MHz	IDD3		18.9		mA	V_{DD} = 3.3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IDD5		6.2		mA	$V_{DD} = 5.5V@$ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
Operating Current	IDD6		3.4		mA	V _{DD} =5.5V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
Normal Run Mode @ 22 MHz	IDD7		6.1		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
S	IDD8		3.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
N.	IDD9		5.3		mA	$V_{DD} = 5.5V@$ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
Operating Current	IDD10		3.7		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz
Normal Run Mode @ 12 MHz	IDD11		4.0		mA	V_{DD} = 3.3V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
S CON	IDD12		2.3		mA	V_{DD} = 3.3V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz

Positive going threshold (Schmitt input), /RST	VIHS	$0.7 V_{DD}$	-	V _{DD} +0.5	V	
Internal /RST pin pull up resistor	RRST	40		150	KΩ	
Negative going threshold (Schmitt input), P0/1/2/3/4	VILS	-0.5	-	$0.3 V_{DD}$	v	
Positive going threshold (Schmitt input), P0/1/2/3/4	VIHS	$0.7 V_{DD}$	-	V _{DD} +0.5	v	N.
Source Current	ISR11	-300	-370	-450	μA	$V_{DD} = 4.5V, VS = 2.4V$
P0/1/2/3/4 (Quasi- bidirectional Mode)	ISR12	-50	-70	-90	μA	$V_{DD} = 2.7V, VS = 2.2V$
bidirectional mode)	ISR13	-40	-60	-80	μA	V _{DD} = 2.5V, VS = 2.0V
	ISR21	-20	-24	-28	mA	$V_{DD} = 4.5V, VS = 2.4V$
Source Current P0/1/2/3/4 (Push-pull	ISR22	-4	-6	-8	mA	V _{DD} = 2.7V, VS = 2.2V
Mode)	ISR23	-3	-5	-7	mA	V _{DD} = 2.5V, VS = 2.0V
Sink Current P0/1/2/3/4	ISK11	10	16	20	mA	V _{DD} = 4.5V, VS = 0.45V
(Quasi-bidirectional and	ISK12	7	10	13	mA	V _{DD} = 2.7V, VS = 0.45V
Push-pull Mode)	ISK13	6	9	12	mA	V _{DD} = 2.5V, VS = 0.45V
Brown-Out voltage with BOV_VL [1:0] =00b	VBO2.2	2.0	2.2	2.4	V	V _{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =01b	VBO2.7	2.5	2.7	2.9	V	V _{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =10b	VBO3.7	3.5	3.7	3.9	V	V _{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =11b	VBO4.4	4.2	4.4	4.6	V	V _{DD} =5.5V
Hysteresis range of BOD voltage	VBH	30	-	150	mV	V _{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.

2. XTAL1 is a CMOS input.

3. Pins of P0 - P7 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} =5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V.

7.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	22	22.1184		MHz
	+25°C; V _{DD} =5V	-3	-	+3	%
Calibrated Internal Oscillator Frequency	-40°C~+85°C; V _{DD} =2.5V~5.5V	-5	S.	+5	%
Operating current	V _{DD} =5V	- X	500	-	uA

7.3.5 Internal 10 kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	NON N	kHz
	+25°C; V _{DD} =5V	-30	-	+30	%
Calibrated Internal Oscillator Frequency	-40°C~+85°C; V _{DD} =2.5V~5.5V	-50	-	+50	%
Operating current	V _{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes from LDO.

Nov. 27, 2014

7.4 Analog Characteristics

7.4.1 12-bit SARADC Specification

SYMBOL	PARA	METER	MIN.	TYP.	MAX.	UNIT	
-	Resolution			-	12	Bit	
DNL	Differential nonlinearity erro	or 💦	20	-1~2.0	-1~4.0	LSB	
INL	Integral nonlinearity error	X	SQ 3	±2	±4	LSB	
Eo	Offset error		NON.	3	-	LSB	
E _G	Gain error (Transfer gain)						
E _F	Full scale error			±2	Sh	LSB	
EA	Absolute error	AV _{DD} =5V		5	150	LSB	
LA		AV _{DD} =3V		4	3		
-	Monotonic			Guaranteed			
F _{ADC}	ADC clock frequency	AV _{DD} =5V			16	MHz	
L UC	ADC Clock nequency	AV _{DD} =3V		-	-1~4.0 ±4 - 1.005	IVIT 12	
Fs	Sample rate		-	-	760	K SPS	
Ts	Sampling time			7		ADC clock	
V _{DDA}	Supply voltage		3	-	5.5	V	
I _{DD}	Supply current (Avg.)		-	0.5	-	mA	
I _{DDA}	Supply current (Avg.) @ AV	4 _{DD} =3.0V	-	2.5	-	mA	
V _{IN}	Analog Input voltage		0	-	V _{ref} ^[1]	V	

Note[1]: V_{ref} is connected to AV_{DD} for LQFP48/QFN33 package.

7.4.2 LDO Specification

RAMETER	MIN	ТҮР	МАХ	UNIT	NOTE
Input Voltage	2.5	4	5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	°C	
С	-	1	-	uF	Resr=1ohm

Note:

- 1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
- 2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature		-40	25	85	°C
Quiescent current	V _{DD} =5.5V	(B)		5	uA
	Temperature=25°	1.7	2.0	2.3	V
Threshold voltage	Temperature=-40°	-	2.3	a C	V
	Temperature=85°	-	1.8	2°C	V
Hysteresis	-	0	0	0	v

7.4.3 Low Voltage Reset Specification

7.4.4 Brown-Out Detector Specification

Parameter	Condition	Min.	Тур.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV _{DD} =5.5V	-	-	140	μA
Temperature	-	-40	25	85	°C
	BOV_VL[1:0]=11	4.2	4.4	4.6	V
Brown-Out voltage	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

7.4.5 Power-On Reset Specification (5V)

Parameter	Condition	Min.	Тур.	Max.	Unit
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.6 Temperature Sensor Specification

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]		1.62	1.8	1.98	V
Temperature		-40	-	85	°C
Gain		-1.72	-1.76	-1.80	mV/°C

9 REVISION HISTORY

Revision	Date	Description	
1.00	Jun. 12, 2014	First version	
1.01	Jul. 24, 2014	Corrected 7.5 Flash DC Electrical Characteristics.	
1.02	Sep. 12, 2014	 Adjusted the format of Table 4.1-1 NuMicro™ M058S Series Selection Guide. Updated Figure 4.1-1 NuMicro™ M058S Series Selection Code. Added Chapter 3 ABBREVIATIONS. Added 7.6 SPI Dynamic Characteristics. Changed the order of Chapter 5 BLOCK DIAGRAM and Chapter 6 FUNCTIONAL DESCRIPTION. Fixed typos and obscure descriptions. 	
1.03	Nov. 27, 2014	1. Fixed typos of Table 4.1-1 NuMicro™ M058S Series Selection Guide	



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