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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058szan

one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
  - Supports 2' complement/un-signed format in differential mode conversion results
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion started either by software trigger or external pin trigger
  - Additional functions
    - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
    - PWM trigger delay function
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1℃ resolution
- BOD (Brown-out Detector)
  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-Out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - 64-pin LQFP, 48-pin LQFP, 33-pin QFN, 20-pin TSSOP

4.2 Pin Configuration

4.2.1 TSSOP20 pin

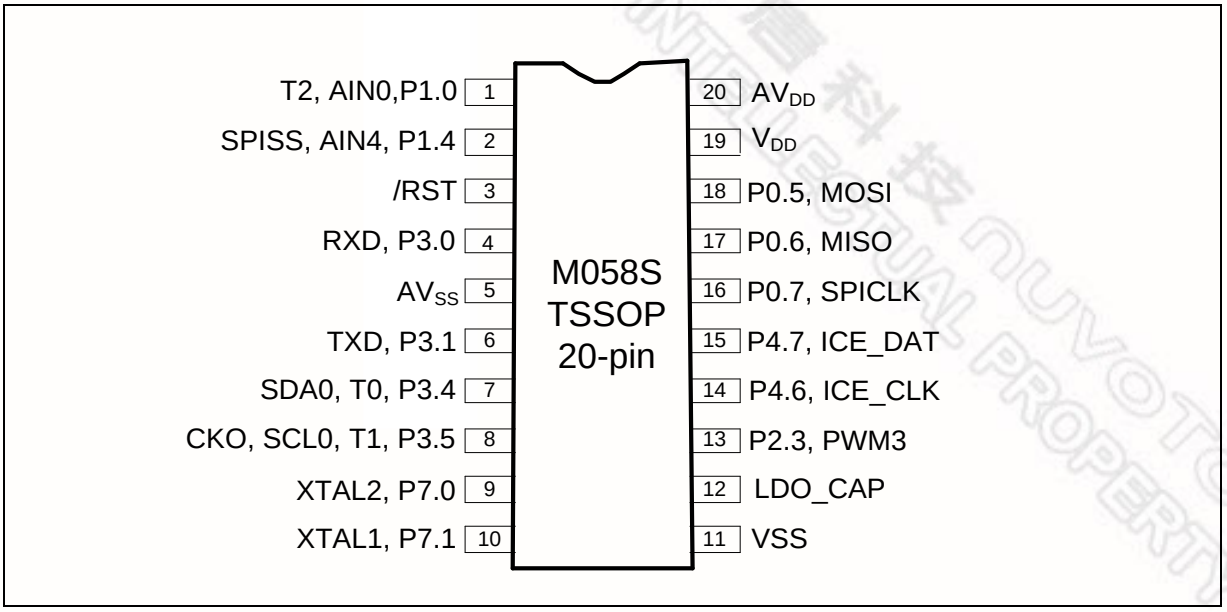

Figure 4.2-1 NuMicro™ M058S TSSOP20 Pin Diagram

4.2.2 QFN 33-pin

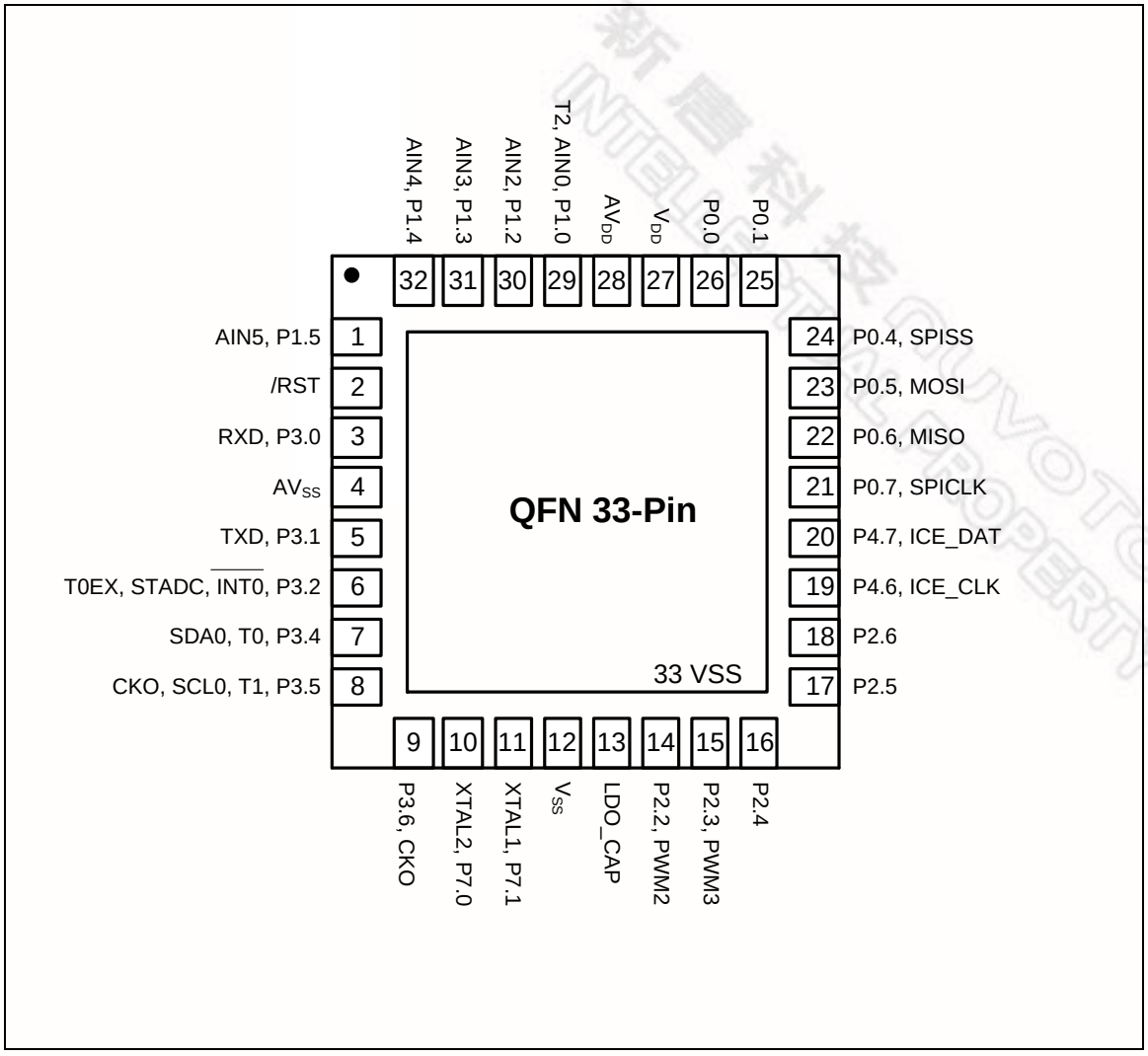

Figure 4.2-2 NuMicro™ M058S Series QFN-33 Pin Diagram

4.2.3 LQFP 48-pin

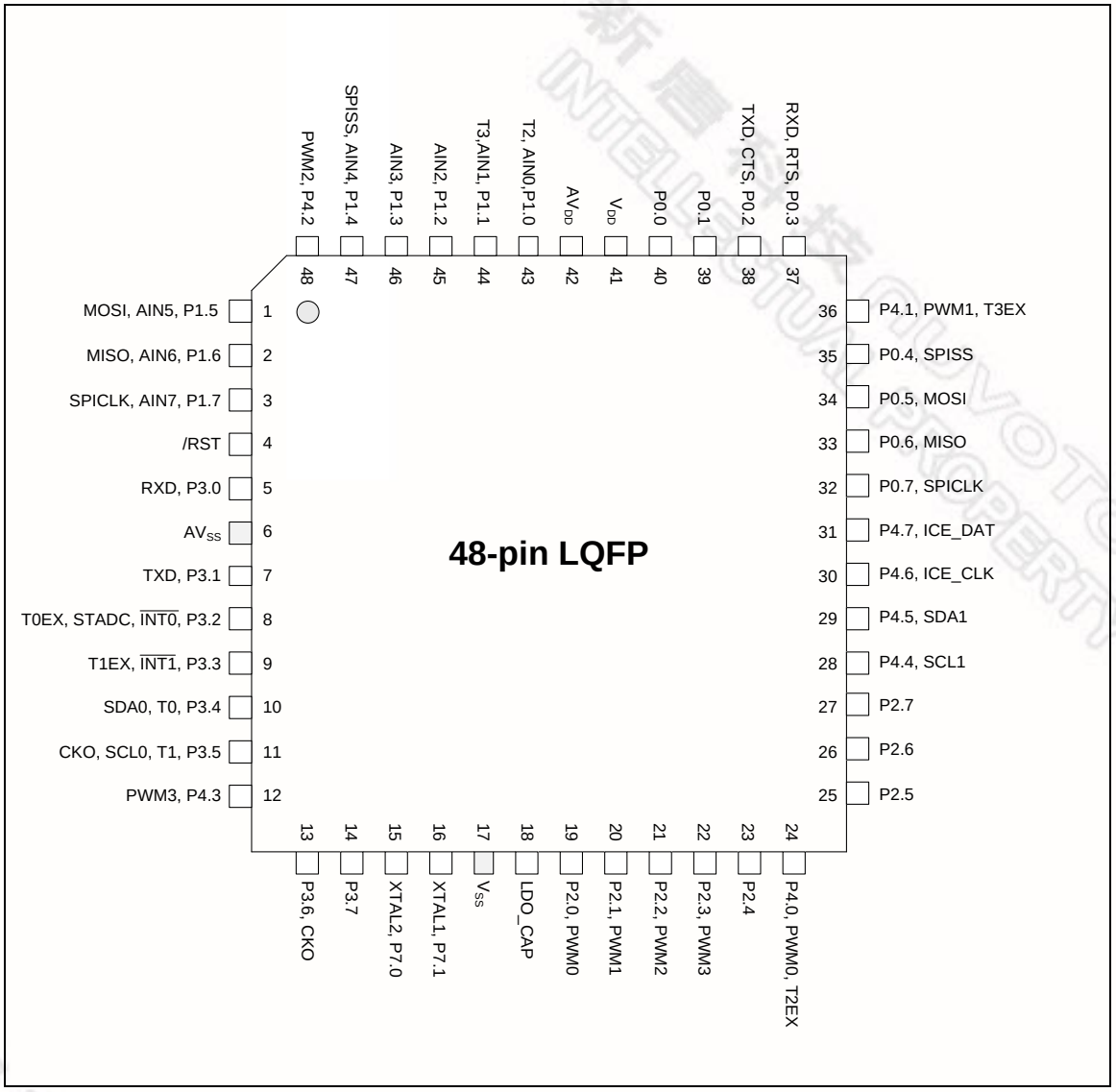

Figure 4.2-3 NuMicro™ M058S Series LQFP-48 Pin Diagram

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
17	22	33	45	P0.6	MISO[2]			I/O	for UART RTS: Request to Send output pin for UART The RXD/TXD pins are for UART function use.
16	21	32	44	P0.7	SPICLK[2]			I/O	
1	29	43	59	P1.0	T2	AIN0		I/O	**PORT1:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T2, T3, SPISS0, MOSI, MISO, and SPICLK. The pins SPISS0, MOSI, MISO, and SCLK are for the SPI function use. The pins AIN0~AIN7 are for the 12 bits ADC function use. The T2/T3 pins are for Timer2/3 external event counter input.
	NC	44	60	P1.1	T3	AIN1		I/O	
	30	45	61	P1.2		AIN2		I/O	
	31	46	62	P1.3		AIN3		I/O	
2	32	47	63	P1.4	SPISS[2]	AIN4		I/O	
	1	1	1	P1.5	MOSI[2]	AIN5		I/O	
	NC	2	2	P1.6	MISO[2]	AIN6		I/O	
	NC	3	3	P1.7	SPICLK[2]	AIN7		I/O	
	NC	19	27	P2.0	PWM0[2]			I/O	**PORT2:** General purpose I/O port, which can be configured by software in four modes. It has an alternative function. The pins PWM0~PWM3 are for the PWM function use.
	NC	20	28	P2.1	PWM1[2]			I/O	
	14	21	29	P2.2	PWM2[2]			I/O	
13	15	22	30	P2.3	PWM3[2]			I/O	
	16	23	31	P2.4				I/O	
	17	25	33	P2.5				I/O	
	18	26	34	P2.6				I/O	
	NC	27	35	P2.7				I/O	
4	3	5	5	P3.0	RXD[2]			I/O	**PORT3:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for RXD, TXD, /INT0, /INT1, T0 and T1. The RXD/TXD pins are for
6	5	7	10	P3.1	TXD[2]			I/O	
	6	8	11	P3.2	/INT0	STADC	T0EX	I/O	
	NC	9	12	P3.3	/INT1		T1EX	I/O	

5 BLOCK DIAGRAM

5.1 NuMicro™ M058S Block Diagram

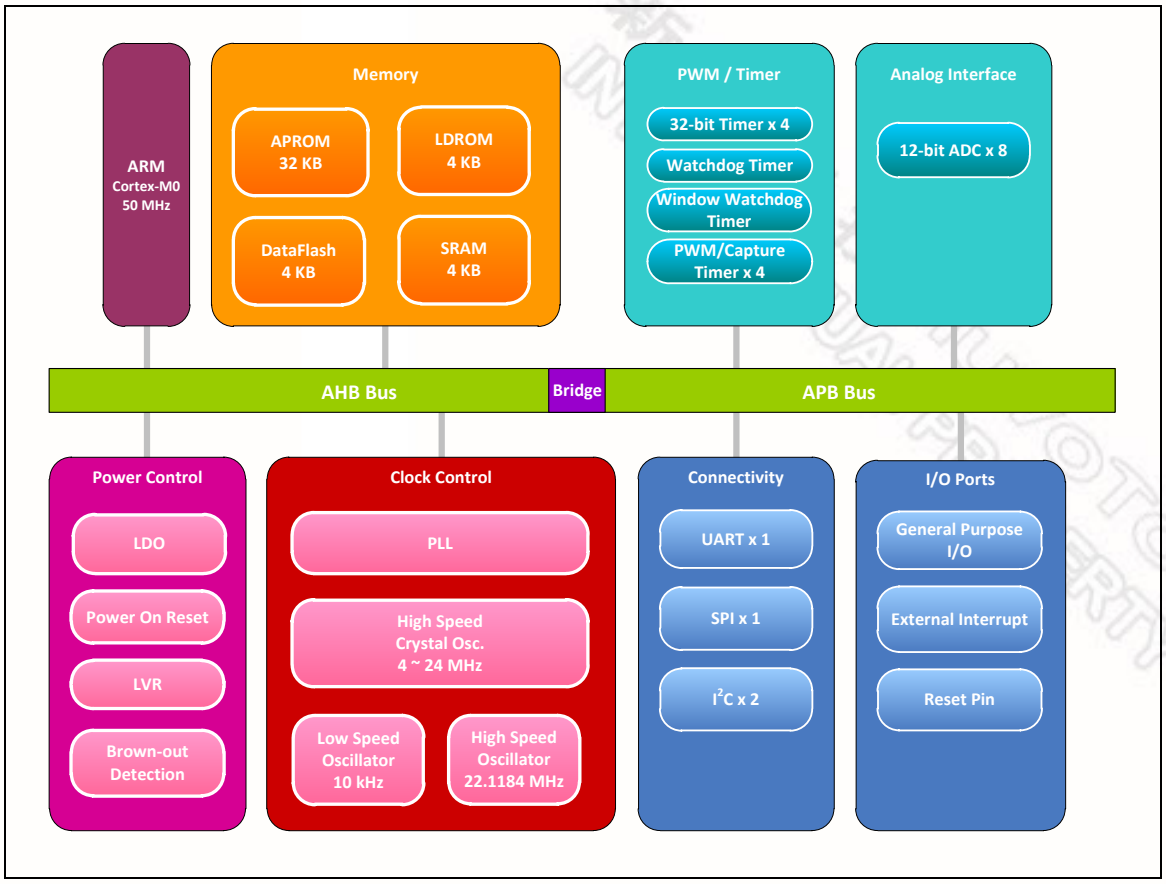

Figure 5.1-1 NuMicro™ M058S Block Diagram

- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

- **NVIC features:**
  - 32 external interrupt inputs, each with four levels of priority.
  - Dedicated non-Maskable Interrupt (NMI) input.
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and provides Ultra-low Power Sleep mode
- **Debug support:**
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- **Bus interfaces:**
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset Pin (nRST)
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

22	0x58	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt	No
23	0x5C	7	Reserved	-	-	-
24	0x60	8	TMR0_INT	TMR0	Timer 0 interrupt	No
25	0x64	9	TMR1_INT	TMR1	Timer 1 interrupt	No
26	0x68	10	TMR2_INT	TMR2	Timer 2 interrupt	No
27	0x6C	11	TMR3_INT	TMR3	Timer 3 interrupt	No
28	0x70	12	UART0_INT	UART0	UART0 interrupt	Yes
29	0x74	13	Reserved	-	-	-
30	0x78	14	SPI0_INT	SPI0	SPI0 interrupt	No
31	0x7C	15	Reserved	-	-	-
32	0x80	16	GP5_INT	GPIO	External signal interrupt from P5[7:0]	Yes
33	0x84	17	GP67_INT	GPIO	External signal interrupt from P6[7:0] / P7[1:0]	Yes
34	0x88	18	I2C0_INT	I^2C0	I^2C0 interrupt	Yes
35	0x8C	19	I2C1_INT	I^2C1	I^2C1 interrupt	Yes
36	0x90	20	CAP0_INT	PWM	PWM0 capture in interrupt	No
37	0x94	21	CAP1_INT	PWM	PWM1 capture in interrupt	No
38	0x98	22	CAP2_INT	PWM	PWM2 capture in interrupt	No
39	0x9C	23	CAP3_INT	PWM	PWM3 capture in interrupt	No
40-43	0x90-0xAC	20-27	Reserved	-	-	-
44	0xB0	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	0xB4	29	ADC_INT	ADC	ADC interrupt	No
46-47	0xB8-0xBC	30-31	Reserved	-	-	

Table 6.2-3 System Interrupt Map Vector Table

6.2.7.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

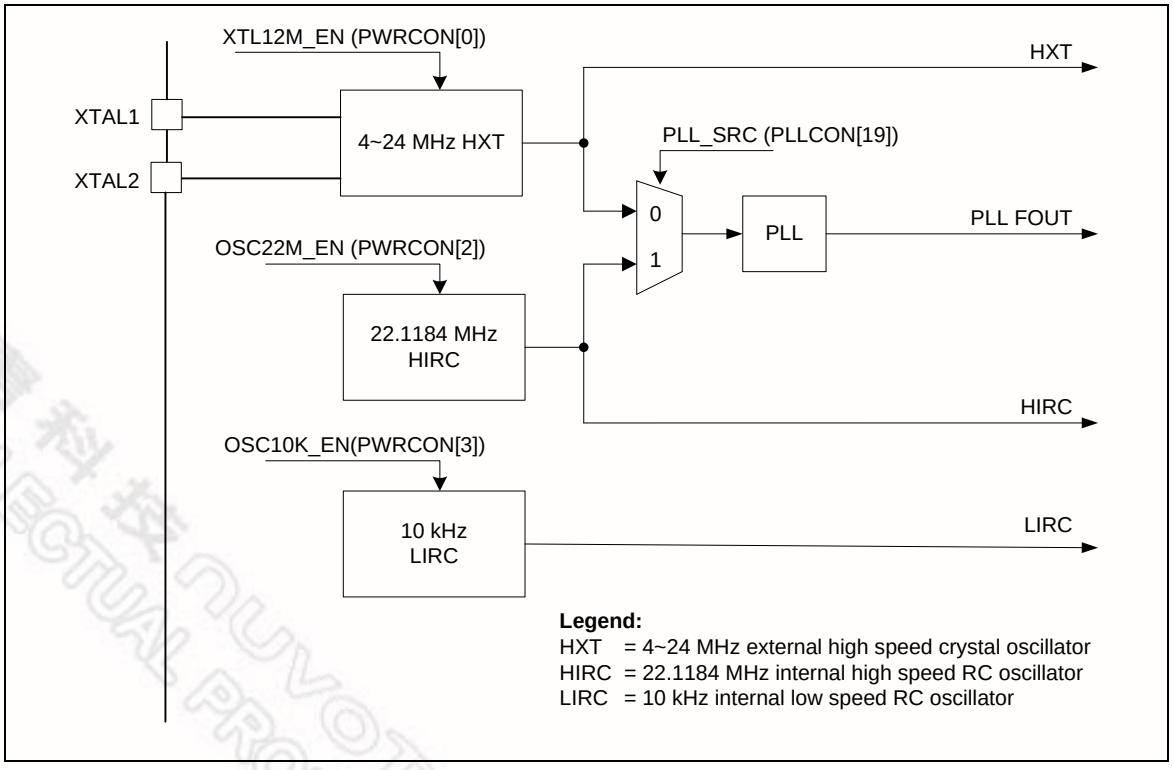

Figure 6.3-1 Clock Generator Block Diagram

6.3.4 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator clock
- Peripherals Clock (when 10 kHz low speed oscillator is adopted as clock source)

6.3.5 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

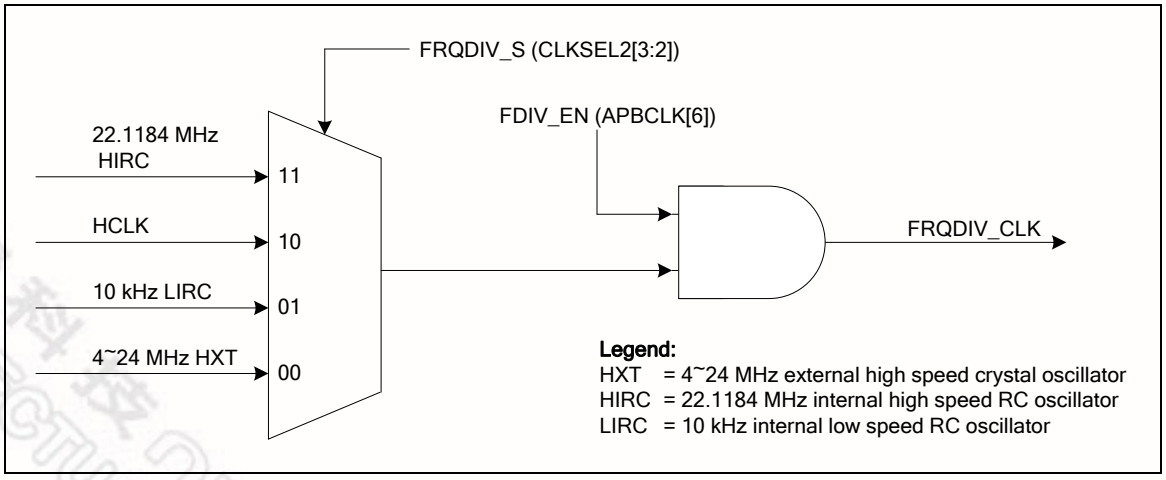

Figure 6.3-6 Clock Source of Frequency Divider

6.6 Timer Controller (TMR)

6.6.1 Overview

The Timer Controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features:

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period time of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period time of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the input event from external counter pin (T0~T3)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX~T3EX) for interval measurement
- Supports external capture pin (T0EX~T3EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Inter-Timer trigger mode

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The NuMicro™ M058S has one sets of PWM groups supporting a total of two sets of PWM generators, which can be configured as four independent PWM outputs, PWM0~PWM3, or as two complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 2 sets of PWM generators provide four independent PWM period interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM period interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-zone are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3) are controlled by PWM2 timers and Dead-zone generator 2. Refer to figures below for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-Timer is set as Auto-reload mode when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically and then starts decreasing repeatedly. If the PWM-Timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-Timer is digital input Capture function. If Capture function is enabled, the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must set the PWM-Timer before enabling the Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). The capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable reset delay period 3/18/130/1026 * WDT_CLK
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

Operating Current Normal Run Mode @ 4 MHz	IDD13		3.4		mA	V_{DD} = 5.5V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD14		2.6		mA	V_{DD} = 5.5V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
	IDD15		2.0		mA	V_{DD} = 3.3V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD16		1.3		mA	V_{DD} = 3.3V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
Operating Current Normal Run Mode @10 KHz	IDD17		98.7		uA	V_{DD} = 5.5V@ 10 KHz, enable all peripherals and IRC10 KHz, disable PLL
	IDD18		97.4		uA	V_{DD} = 5.5V@ 10 KHz, disable all peripherals and enable IRC 10KHz, disable PLL
	IDD19		86.4		uA	V_{DD} = 3.3V@ 10 KHz, enable all peripherals and IRC 10 KHz, disable PLL
	IDD20		85.2		uA	V_{DD} = 3.3V@ 10 KHz, disable all peripherals and enable IRC 10 KHz, disable PLL
Operating Current Idle Mode @ 50 MHz	IIDLE1		16.2		mA	V_{DD} = 5.5V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE2		10.0		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IIDLE3		14.6		mA	V_{DD} = 3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE4		8.5		mA	V_{DD} = 3V@50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 22 MHz	IIDLE5		4.3		mA	V_{DD} = 5.5V@ 22MHz, enable all peripherals and IRC 22MHz, disable PLL
	IIDLE6		1.5		mA	V_{DD} =5.5V@ 22MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
	IIDLE7		4.2		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IIDLE8		1.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22MHz, disable PLL
Operating Current Idle Mode @ 12 MHz	IIDLE9		4.3		mA	V_{DD} = 5.5V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12MHz
	IIDLE10		2.6		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12MHz

Positive going threshold (Schmitt input), /RST	VIHS	0.7 V_{DD}	-	V_{DD} +0.5	V	
Internal /RST pin pull up resistor	RRST	40		150	KΩ	
Negative going threshold (Schmitt input), P0/1/2/3/4	VILS	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), P0/1/2/3/4	VIHS	0.7 V_{DD}	-	V_{DD} +0.5	V	
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	ISR11	-300	-370	-450	μA	V_{DD} = 4.5V, VS = 2.4V
	ISR12	-50	-70	-90	μA	V_{DD} = 2.7V, VS = 2.2V
	ISR13	-40	-60	-80	μA	V_{DD} = 2.5V, VS = 2.0V
Source Current P0/1/2/3/4 (Push-pull Mode)	ISR21	-20	-24	-28	mA	V_{DD} = 4.5V, VS = 2.4V
	ISR22	-4	-6	-8	mA	V_{DD} = 2.7V, VS = 2.2V
	ISR23	-3	-5	-7	mA	V_{DD} = 2.5V, VS = 2.0V
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	ISK11	10	16	20	mA	V_{DD} = 4.5V, VS = 0.45V
	ISK12	7	10	13	mA	V_{DD} = 2.7V, VS = 0.45V
	ISK13	6	9	12	mA	V_{DD} = 2.5V, VS = 0.45V
Brown-Out voltage with BOV_VL [1:0] =00b	VBO2.2	2.0	2.2	2.4	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =01b	VBO2.7	2.5	2.7	2.9	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =10b	VBO3.7	3.5	3.7	3.9	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =11b	VBO4.4	4.2	4.4	4.6	V	V_{DD} =5.5V
Hysteresis range of BOD voltage	VBH	30	-	150	mV	V_{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0 - P7 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V.

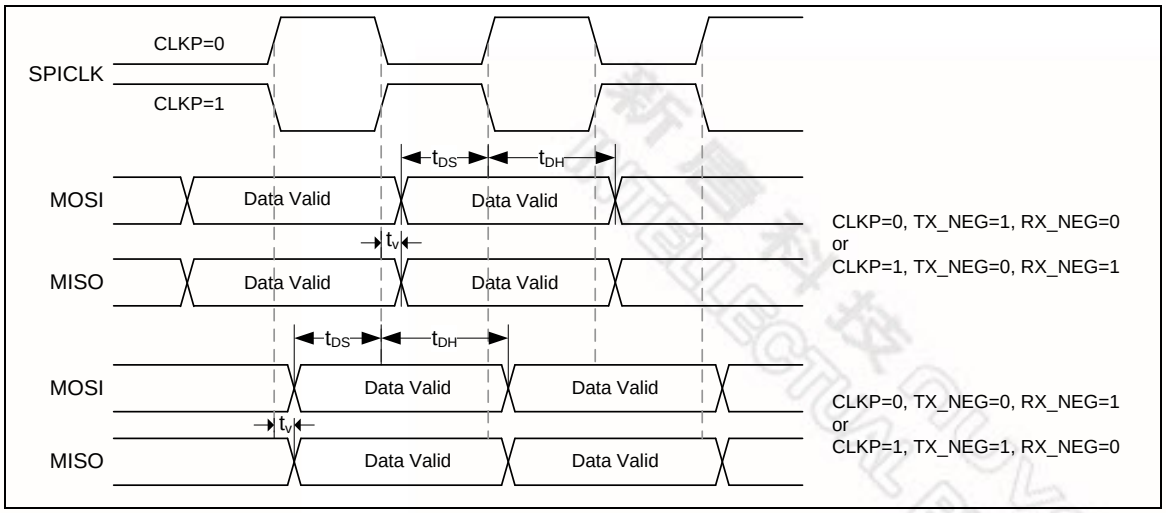

Figure 7.6-2 SPI Slave Mode Timing

9 REVISION HISTORY

Revision	Date	Description
1.00	Jun. 12, 2014	First version
1.01	Jul. 24, 2014	Corrected 7.5 Flash DC Electrical Characteristics.
1.02	Sep. 12, 2014	1. Adjusted the format of Table 4.1-1 NuMicro™ M058S Series Selection Guide. 2. Updated Figure 4.1-1 NuMicro™ M058S Series Selection Code. 3. Added Chapter 3 ABBREVIATIONS. 4. Added 7.6 SPI Dynamic Characteristics. 5. Changed the order of Chapter 5 BLOCK DIAGRAM and Chapter 6 FUNCTIONAL DESCRIPTION. 6. Fixed typos and obscure descriptions.
1.03	Nov. 27, 2014	1. Fixed typos of Table 4.1-1 NuMicro™ M058S Series Selection Guide

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