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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 1x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5365axi-043

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1. Architectural Overview

Introducing the CY8C53 family of ultra low-power, flash Programmable System-on-Chip (PSoC[®]) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C53 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.



Figure 1-1. Simplified Block Diagram

Figure 1-1 illustrates the major components of the CY8C53 family. They are:

- ARM Cortex-M3 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. The designer can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.



The CY8C53 family supports a wide supply operating range from 2.7 to 5.5 V. This allows operation from regulated supplies such as $3.3 \text{ V} \pm 10\%$ or $5.0 \text{ V} \pm 10\%$, or directly from a wide range of battery types.

PSoC supports a wide range of low power modes. These include a 300-nA hibernate mode with RAM retention and a 2- μ A sleep mode.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 6 mA when the CPU is running at 6 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 22 of this data sheet.

PSoC uses a SWD interface for programming, debug, and test. Using this standard interface enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include FPB, DWT, and ITM. These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 53 of this data sheet.

2. Pinouts

The VDDIO pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 and Figure 2-2. Using the VDDIO pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each VDDIO may sink up to 20 mA total to its associated I/O pins and opamps, and each set of VDDIO associated pins may sink up to 100 mA.



- Bit-band support for the SRAM region. Atomic bit-level write and read operations for SRAM addresses.
- Unaligned data storage and access. Contiguous storage of data of different byte lengths.
- Operation at two privilege levels (privileged and user) and in two modes (thread and handler). Some instructions can only be executed at the privileged level. There are also two stack pointers: Main (MSP) and Process (PSP). These features support a multitasking operating system running one or more user-level processes.
- Extensive interrupt and system exception support.

4.1.2 Cortex-M3 Operating Modes

The Cortex-M3 operates at either the privileged level or the user level, and in either the thread mode or the handler mode. Because the handler mode is only enabled at the privileged level, there are actually only three states, as shown in Table 4-1.

Table 4-1. Operational Level

Condition	Privileged	User
Running an exception	Handler mode	Not used
Running main program	Thread mode	Thread mode

At the user level, access to certain instructions, special registers, configuration registers, and debugging components is blocked. Attempts to access them cause a fault exception. At the privileged level, access to all instructions and registers is allowed.

The processor runs in the handler mode (always at the privileged level) when handling an exception, and in the thread mode when not.

4.1.3 CPU Registers

The Cortex-M3 CPU registers are listed in Table 4-2. Registers R0-R15 are all 32 bits wide.

Table 4-2. Cortex M3 CPU Registers

Register	Description
R0-R12	General purpose registers R0-R12 have no special architecturally defined uses. Most instructions that specify a general purpose register specify R0-R12.
	Low Registers: Registers R0-R7 are accessible by all instructions that specify a general purpose register.
	High Registers: Registers R8-R12 are accessible by all 32-bit instructions that specify a general purpose register; they are not accessible by all 16-bit instructions.

Register	Description
R13	R13 is the stack pointer register. It is a banked register that switches between two 32-bit stack pointers: the Main Stack Pointer (MSP) and the Process Stack Pointer (PSP). The PSP is used only when the CPU operates at the user level in thread mode. The MSP is used in all other privilege levels and modes. Bits[0:1] of the SP are ignored and considered to be 0, so the SP is always aligned to a word (4 byte) boundary.
R14	R14 is the Link Register (LR). The LR stores the return address when a subroutine is called.
R15	R15 is the Program Counter (PC). Bit 0 of the PC is ignored and considered to be 0, so instructions are always aligned to a half word (2 byte) boundary.
xPSR	The Program status registers are divided into three status registers, which are accessed either together or separately:
	Application Program Status Register (APSR) holds program execution status bits such as zero, carry, negative, in bits[27:31].
	 Interrupt Program Status Register (IPSR) holds the current exception number in bits[0:8].
	Execution Program Status Register (EPSR) holds control bits for interrupt continuable and IF-THEN instructions in bits[10:15] and [25:26]. Bit 24 is always set to 1 to indicate Thumb mode. Trying to clear it causes a fault exception.
PRIMASK	A 1-bit interrupt mask register. When set, it allows only the nonmaskable interrupt (NMI) and hard fault exception. All other exceptions and interrupts are masked.
FAULTMASK	A 1-bit interrupt mask register. When set, it allows only the NMI. All other exceptions and interrupts are masked.
BASEPRI	A register of up to nine bits that define the masking priority level. When set, it disables all interrupts of the same or higher priority value. If set to 0 then the masking function is disabled.
CONTROL	A 2-bit register for controlling the operating mode. Bit 0: 0 = privileged level in thread mode, 1 = user level in thread mode.
	Bit 1: 0 = default stack (MSP) is used, 1 = alternate stack is used. If in thread mode or user level then the alternate stack is the PSP. There is no alternate stack for handler mode; the bit must be 0 while in handler mode.

Table 4-2. Cortex M3 CPU Registers (continued)



Table 4-6. Interrupt Vector Table

Interrupt #	Cortex-M3 Exception #	Fixed Function	DMA	UDB
0	16	Low voltage detect (LVD)	phub_termout0[0]	udb_intr[0]
1	17	Cache	phub_termout0[1]	udb_intr[1]
2	18	Reserved	phub_termout0[2]	udb_intr[2]
3	19	Pwr Mgr	phub_termout0[3]	udb_intr[3]
4	20	PICU[0]	phub_termout0[4]	udb_intr[4]
5	21	PICU[1]	phub_termout0[5]	udb_intr[5]
6	22	PICU[2]	phub_termout0[6]	udb_intr[6]
7	23	PICU[3]	phub_termout0[7]	udb_intr[7]
8	24	PICU[4]	phub_termout0[8]	udb_intr[8]
9	25	PICU[5]	phub_termout0[9]	udb_intr[9]
10	26	PICU[6]	phub_termout0[10]	udb_intr[10]
11	27	PICU[12]	phub_termout0[11]	udb_intr[11]
12	28	PICU[15]	phub_termout0[12]	udb_intr[12]
13	29	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	30	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	31	I ² C	phub_termout0[15]	udb_intr[15]
16	32	Reserved	phub_termout1[0]	udb_intr[16]
17	33	Reserved	phub_termout1[1]	udb_intr[17]
18	34	Reserved	phub_termout1[2]	udb_intr[18]
19	35	Reserved	phub_termout1[3]	udb_intr[19]
20	36	Reserved	phub_termout1[4]	udb_intr[20]
21	37	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	38	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	39	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	40	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	41	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	42	Reserved	phub_termout1[10]	udb_intr[26]
27	43	Reserved	phub_termout1[11]	udb_intr[27]
28	44	Reserved	phub_termout1[12]	udb_intr[28]
29	45	Decimator Int	phub_termout1[13]	udb_intr[29]
30	46	phub_err_int	phub_termout1[14]	udb_intr[30]
31	47	eeprom_fault_int	phub_termout1[15]	udb_intr[31]





5. Memory

5.1 Static RAM

CY8C53 static RAM (SRAM) is used for temporary data storage. Code can be executed at full speed from the portion of SRAM that is located in the code space. This process is slower from SRAM above 0x20000000. The device provides up to 64 KB of SRAM. The CPU or the DMA controller can access all of SRAM. The SRAM can be accessed simultaneously by the Cortex-M3 CPU and the DMA controller if accessing different 32-KB blocks.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data and bulk data storage. The main flash memory area contains up to 256 KB of user program space.

Up to an additional 32 KB of flash space is available for storing device configuration data and bulk user data. User code may not be run out of this flash memory section. The flash output is 9 bytes wide with 8 bytes of data and 1 additional byte.

The flash programming interface performs flash erasing, programming and setting code protection levels. Flash In System Serial Programming (ISSP), typically used for production programming, is possible through the SWD interface. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I²C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of configuration or general-purpose data.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 55). For more information on how to take full advantage of the security features in PSoC, see the PSoC 5 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	-
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C53 has 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into two sections, each containing 64 rows of 16 bytes each.

The CPU cannot execute out of EEPROM.





Figure 6-1. Clocking Subsystem

6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from $\pm 5\%$ at 3 MHz, up to $\pm 10\%$ at 48 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency. The IMO provides clock outputs at 3, 6, 12, 24, and 48 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the MHzECO or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz,

where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 μ s (verified by bit setting). It can be configured to use a clock from the IMO, MHZECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to long sleep intervals using the central timewheel (CTW). The central timewheel is a free running counter clocked by the ILO 1 kHz output. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the RTC capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low-power system clock to



Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.8 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.9 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

7.2.2.10 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.11 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-9. Example FIFO Configurations



7.2.2.12 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.13 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

7.2.2.14 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-10. Status and Control Registers



The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

7.2.3.15 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a "compare true" condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.



7.2.3.16 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-11 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-11. Digital System Interface Structure



7.3.1 UDB Array Programmable Resources

Figure 7-12 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions. An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-12. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-13 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.









Figure 8-4. Analog Comparator

8.3.2 LUT

The CY8C53 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-1.

Table 8-1. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	В
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')



8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-7. The schematic in Figure 8-7 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-2.

Table 8-2. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-7. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 K Ω and 1 M Ω through a configuration register. Table 8-3 shows the possible values of Rfb and associated configuration settings.

Configuration Word	Nominal $R_{fb}(K\Omega)$
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Table 8-3. Feedback Resistor Settings

Figure 8-8. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C53 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels





- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane x 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization
- LCD driver configurable to be active when PSoC is in limited active mode

Figure 8-9. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.9 DAC

The CY8C53 parts contain two Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- 5.5 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Note that a write of a new value to the DAC may result in an indeterminate value on the DAC output. To output the desired value, write or strobe the DAC twice with the same value. Since the first write may result in an indeterminate output, the time between the two writes should be minimized. This applies to writes by CPU, DMA, and strobe.



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
V _{DDA}	Input voltage		2.7	_	5.5	V
V _{CCA}	Output voltage		-	1.80	-	V
	Regulator output capacitor ^[24]	±10%, X5R ceramic or better	-	1	10	μF

Figure 11-4. Analog Regulator PSRR vs Frequency and V_{DD}



11.4 Inputs and Outputs

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.4.1 GPIO

Table 11-6. GPIO DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
V _{IH}	Input voltage high threshold	CMOS Input, PRT[x]CTL = 0	$0.7 \times V_{DDIO}$	_	_	V
V _{IL}	Input voltage low threshold	CMOS Input, PRT[x]CTL = 0	-	-	0.3 ×	V
					■ DDIO	
V _{IH}	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1	2.0	-	-	V
V _{IL}	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1	-	-	0.8	V
V _{OH}	Output voltage high	I _{OH} = 4 mA at 3.3 V _{DDIO}	$V_{DDIO} - 0.6$	-	-	V
V _{OL}	Output voltage low	I _{OL} = 8 mA at 3.3 V _{DDIO}	_	-	0.6	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I _{IL}	Input leakage current (absolute value) ^[22]	25 °C, V _{DDIO} = 3.0 V	-	_	2	nA

Notes

- 22. Based on device characterization (Not production tested).
- 23. For information on designing with PSoC 3 oscillators, refer to the application note, AN54439 $PSoC^{\textcircled{B}}$ 3 and PSoC 5 External Oscillator. 24. 10 µF is required for sleep mode. See Table 11-3.



Table 11-6. GPIO DC Specifications (continued)

Parameter	Description	Conditions	Min	Тур	Max	Units
C _{IN}	Input capacitance ^[22]	GPIOs not shared with opamp outputs or kHzECO or SAR ADC external reference input	_	4	7	pF
		GPIOs shared with kHzECO ^[23]	-	5	7	pF
		GPIOs shared with opamp outputs	-	-	18	pF
		GPIO shared with SAR ADC external reference input	_	_	30	pF
V _H	Input voltage hysteresis (Schmitt-Trigger) ^[22]		-	150	Ι	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		_	_	100	μA
Rglobal	Resistance pin to analog global bus	25 °C, V _{DDIO} = 3.0 V	_	320	_	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V _{DDIO} = 3.0 V	—	220	_	Ω









Table 11-7. GPIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
TriseF	Rise time in Fast Strong Mode ^[25]	3.3 V V _{DDIO} Cload = 25 pF	_	-	12	ns
TfallF	Fall time in Fast Strong Mode ^[25]	3.3 V V _{DDIO} Cload = 25 pF	-	-	12	ns
TriseS	Rise time in Slow Strong Mode ^[25]	3.3 V V _{DDIO} Cload = 25 pF	-	-	60	ns
TfallS	Fall time in Slow Strong Mode ^[25]	3.3 V V _{DDIO} Cload = 25 pF	-	-	60	ns
	GPIO output operating frequency					
	Fast strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	33	MHz
Fgpioout	$3.3 \text{ V} \le \text{V}_{\text{DDIO}} \le 5.5 \text{ V}$, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	7	MHz
	$2.7 \text{ V} \leq \text{V}_{\text{DDIO}} < 3.3 \text{ V}$, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	3.5	MHz
Fgpioin	GPIO input operating frequency					
	2.7 V ≤ V _{DDIO} ≤ 5.5 V	90/10% V _{DDIO}	_	-	66	MHz



Table 11-9. SIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%) ^[28]	Cload = 25 pF, V _{DDIO} = 3.3 V	_	-	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%) ^[28]	Cload = 25 pF, V _{DDIO} = 3.3 V	_	-	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%) ^[28]	Cload = 25 pF, V _{DDIO} = 3.0 V	_	-	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%) ^[28]	Cload = 25 pF, V _{DDIO} = 3.0 V	_	-	60	ns
	SIO output operating frequency	1		l	L	1
	Unregulated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	_	_	33	MHz
	$3.3 \text{ V} < \text{V}_{\text{DDIO}} < 5.5 \text{ V}$, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	5	MHz
Fsioout	2.7 V < V _{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	4	MHz
	Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	_	20	MHz
	Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	-	-	2.5	MHz
Fsioin	SIO input operating frequency	90/10% V _{DDIO}	_	_	66	MHz

Figure 11-12. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Figure 11-13. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load





Figure 11-26. SAR ADC I_{DD} vs sps, V_{DDA} = 5 V, Continuous Sample Mode, External Reference Mode



Table 11-19. SAR ADC AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Sample rate ^[33]	With bypass capacitor	-	-	700	ksps
		Without bypass capacitor	-	-	100	
	Startup time ^[33]		-	_	10	μs
SINAD	Signal-to-noise ratio ^[33]	$V_{DDA} \leq 3.6 \text{ V}, V_{REF} \leq 3.6 \text{ V}$	57	-	-	dB
		$3.6 \text{ V} < \text{V}_{\text{DDA}} \le 5.5 \text{ V}$ $\text{V}_{\text{REF}} < 1.3 \text{ V} \text{ or } \text{V}_{\text{REF}} > 1.8 \text{ V}$	57	_	_	
THD	Total harmonic distortion ^[33]	$V_{DDA} \leq 3.6 \text{ V}, V_{REF} \leq 3.6 \text{ V}$	-	-	0.1	%
		$3.6 V < V_{DDA} \le 5.5 V$ $V_{REF} < 1.3 V \text{ or } V_{REF} > 1.8 V$	-	-	0.1	

Figure 11-27. SAR ADC Noise Histogram, 1000 samples, 700 ksps, Internal Reference No Bypass, $V_{IN} = VREF/2$



Figure 11-28. SAR ADC Noise Histogram, 1000 samples, 700 ksps, Internal Reference Bypassed, V_{IN} = VREF/2



Note

33. Based on device characterization (Not production tested).



11.9 Clocking

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 kHz External Crystal Oscillator (kHzECO)

For more information on crystal selection for the kHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-57. kHz ECO DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{DD}	Oscillator operating current	Low power mode; CL = 6 pF	-	0.25	-	μA
C _{IN}	Capacitance at Pins kHz-XTAL:Xi and kHz-XTAL:Xo ^[42]		_	5	7	pF

Table 11-58. kHz ECO Crystal Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
F	Crystal frequency		-	32.768	-	kHz
CL	Crystal load capacitance	Recommended values	_	6 or 12.5	-	pF
DL	Crystal drive level tolerance		1	-	-	μW

11.9.2 Internal Main Oscillator

Table 11-59. IMO DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Supply current				•	
	48 MHz		-	465	850	μA
	24 MHz		-	195	500	μA
	12 MHz		-	150	450	μA
	6 MHz		-	120	400	μA
	3 MHz		-	105	300	μA

42. Based on device characterization (Not production tested).



11.9.3 Internal Low Speed Oscillator

Table 11-61. ILO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Startup time, all frequencies	Turbo mode	-	-	2.5	ms
	ILO frequencies (trimmed)					
	100 kHz		45	100	200	kHz
E	1 kHz		0.5	1	2	kHz
LIC	ILO frequencies (untrimmed)					
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz

Figure 11-63. ILO Frequency Variation vs. Temperature



Figure 11-64. ILO Frequency Variation vs. V_{DD}





11.9.4 MHz External Crystal Oscillator (MHzECO)

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-62. MHzECO Crystal Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
F	Crystal frequency		4	-	25	MHz
CL	Crystal load capacitance		_	_	20	pF
C0	Crystal shunt capacitance		_	_	7	pF
ESR	Crystal effective series resistance	4 MHz ≤ F < 8 MHz	_	_	125	Ω
		8 MHz ≤ F < 12 MHz	-	_	75	Ω
		12 MHz ≤ F ≤ 25 MHz	_	_	50	Ω
DL	Crystal drive level tolerance	No Rs, see AN54439	500	_	_	μW
C _{IN}	Capacitance at Pins MHz-XTAL:Xi and MHz-XTAL:Xo ^[44]		-	4	_	pF

11.9.5 External Clock Reference

Table 11-63. External Clock Reference AC Specifications^[45]

Parameter	Description	Conditions	Min	Тур	Max	Units
	External frequency range		0	_	33	MHz
	Input duty cycle range	Measured at V _{DDIO} /2	30	50	70	%
	Input edge rate	V _{IL} to V _{IH}	0.5	_	_	V/ns

11.9.6 Phase-Locked Loop

Table 11-64. PLL DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	-	400	_	μA
		In = 3 MHz, Out = 24 MHz	_	200	_	μA

Table 11-65. PLL AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Fpllin	PLL input frequency ^[45]		1	-	48	MHz
	PLL intermediate frequency ^[46]	Output of prescaler	1	-	3	MHz
Fpllout	PLL output frequency ^[45]		24	-	67	MHz
	Lock time at startup		-	-	250	μs
Jperiod-rms	Jitter (rms) ^[47]		-	-	400	ps

Notes

- 44. Based on device characterization (Not production tested).
 45. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
 46. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

47. Based on device characterization (Not production tested).



Figure 13-2. 100-Pin TQFP (14 × 14 × 1.4 mm) Package Outline

