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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30833fjfp-u3

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85ºC Version)

Please contact our sales office for V version information.

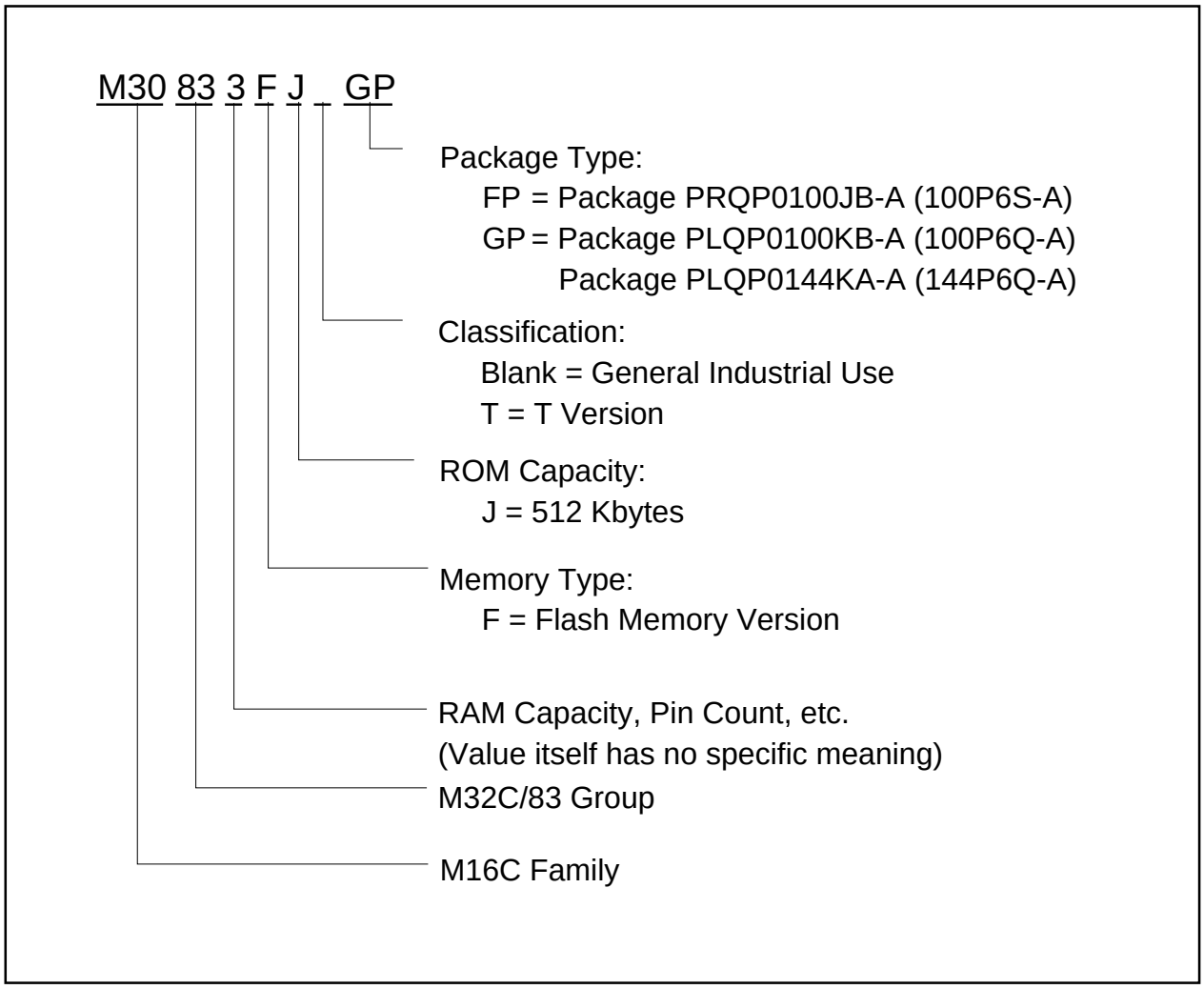


Figure 1.2 Product Numbering System

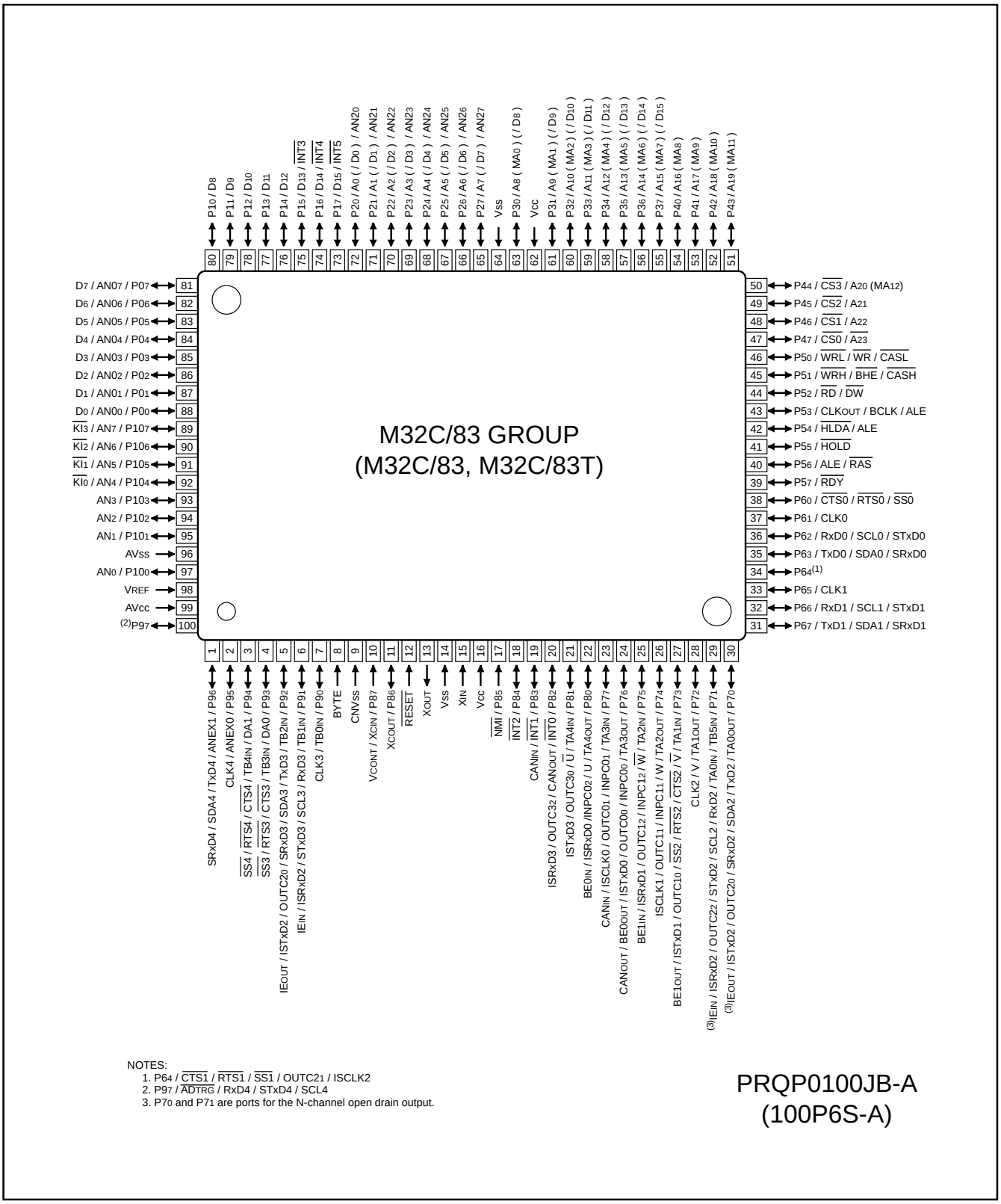


Figure 1.4 Pin Assignment for 100-Pin Package

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Function
Power Supply	VCC VSS	I	Apply 3.0 to 5.5V to both VCC pin. Apply 0V to the VSS pin. (1)
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS
Reset Input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Switches processor mode. Connect the CNVSS pin to VSS to start up in single-chip mode or to VCC to start up in microprocessor mode
Input to Switch External Data Bus Width(2)	BYTE	I	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to VSS to use the microcomputer in single-chip mode
Bus Control Pins(2)	D0 to D7	I/O	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	Outputs address bits A0 to A22
	$\overline{\text{A23}}$	O	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	Outputs $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ that are chip-select signals specifying an external space
	$\overline{\text{WRL}}$ / $\overline{\text{WR}}$ $\overline{\text{WRH}}$ / $\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$) and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{WR}}$ and $\overline{\text{BHE}}$ by program ■ $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{\text{WRL}}$ is held "L". Data is written to an odd address when $\overline{\text{WRH}}$ is held "L". Data is read when $\overline{\text{RD}}$ is held "L". ■ $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ selected: Data is written to external memory space when $\overline{\text{WR}}$ is held "L". Data in an external memory space is read when $\overline{\text{RD}}$ is held "L". An odd address is accessed when $\overline{\text{BHE}}$ is held "L". Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for external 8-bit data bus.
	ALE	O	ALE is a signal latching the address
	$\overline{\text{HOLD}}$	I	The microcomputer is placed in a hold state while the $\overline{\text{HOLD}}$ pin is held "L"
	$\overline{\text{HLDA}}$	O	Outputs an "L" signal while the microcomputer is placed in a hold state
	$\overline{\text{RDY}}$	I	Bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is held "L"
DRAM Bus Control Pin(2)	MA0 to MA12	O	When DRAM area is accessed, outputs column and row addresses by time-sharing.
	$\overline{\text{DW}}$ $\overline{\text{CASL}}$ $\overline{\text{CASH}}$ $\overline{\text{RAS}}$	O	The $\overline{\text{DW}}$ signal becomes "L" when data is written to the DRAM area. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ are signals indicating the timing to latch column addresses. The $\overline{\text{CASL}}$ signal becomes "L" when an even address is accessed. The $\overline{\text{CASH}}$ signal becomes "L" when an odd address is accessed. $\overline{\text{RAS}}$ is a signal latching row addresses.

I : Input O : Output I/O : Input and output

NOTES:

1. Apply 4.2 to 5.5V to the VCC pin when using M32C/83T.
2. Bus control pins in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			
0040₁₆	DRAM Control Register (1)	DRAMCONT	XX₁₆
0041₁₆	DRAM Refresh Interval Set Register (1)	REFCNT	XX₁₆
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆			
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆	Flash Memory Control Register 0	FMR0	XX00 0001₂
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
012016 012116	Group 1 Base Timer Register	G1BT	XX16 XX16
012216	Group 1 Base Timer Control Register 0	G1BCR0	0016
012316	Group 1 Base Timer Control Register 1	G1BCR1	0016
012416	Group 1 Time Measurement Prescaler Register 6	G1TPR6	0016
012516	Group 1 Time Measurement Prescaler Register 7	G1TPR7	0016
012616	Group 1 Function Enable Register	G1FE	0016
012716	Group 1 Function Select Register	G1FS	0016
012816 012916	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX2 XX00 XXXX2
012A16	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX16
012B16			
012C16	Group 1 Receive Input Register	G1RI	XX16
012D16	Group 1 SI/O Communication Mode Register	G1MR	0016
012E16	Group 1 Transmit Output Register	G1TO	XX16
012F16	Group 1 SI/O Communication Control Register	G1CR	0000 X0002
013016	Group 1 Data Compare Register 0	G1CMP0	XX16
013116	Group 1 Data Compare Register 1	G1CMP1	XX16
013216	Group 1 Data Compare Register 2	G1CMP2	XX16
013316	Group 1 Data Compare Register 3	G1CMP3	XX16
013416	Group 1 Data Mask Register 0	G1MSK0	XX16
013516	Group 1 Data Mask Register 1	G1MSK1	XX16
013616			
013716			
013816 013916	Group 1 Receive CRC Code Register	G1RCRC	XX16 XX16
013A16 013B16	Group 1 Transmit CRC Code Register	G1TCRC	0016 0016
013C16	Group 1 SI/O Extended Mode Register	G1EMR	0016
013D16	Group 1 SI/O Extended Receive Control Register	G1ERC	0016
013E16	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX2
013F16	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX2
014016 014116	Group 2 Waveform Generating Register 0	G2PO0	XX16 XX16
014216 014316	Group 2 Waveform Generating Register 1	G2PO1	XX16 XX16
014416 014516	Group 2 Waveform Generating Register 2	G2PO2	XX16 XX16
014616 014716	Group 2 Waveform Generating Register 3	G2PO3	XX16 XX16
014816 014916	Group 2 Waveform Generating Register 4	G2PO4	XX16 XX16
014A16 014B16	Group 2 Waveform Generating Register 5	G2PO5	XX16 XX16
014C16 014D16	Group 2 Waveform Generating Register 6	G2PO6	XX16 XX16
014E16 014F16	Group 2 Waveform Generating Register 7	G2PO7	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0210₁₆ 0211₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00₁₆(2) 00₁₆(2)
0212₁₆			
0213₁₆			
0214₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000₂(2)
0215₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000₂(2)
0216₁₆			
0217₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001₂(2)
0218₁₆			
0219₁₆			
021A₁₆			
021B₁₆			
021C₁₆			
021D₁₆			
021E₁₆			
021F₁₆			
0220₁₆			
0221₁₆			
0222₁₆			
0223₁₆			
0224₁₆			
0225₁₆			
0226₁₆			
0227₁₆			
0228₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000₂(2)
0229₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000₂(2)
022A₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000₂(2)
022B₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00₁₆(2)
022C₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000₂(2)
022D₁₆			
022E₁₆			
022F₁₆			
0230₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000₂(2) XXX0 0000₂(2)
0231₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000₂(2) XX00 0000₂(2)
0232₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000₂(2) XXXX 0000₂(2)
0233₁₆	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00₁₆(2) 00₁₆(2)
0234₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000₂(2) XX00 0000₂(2)
0235₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00₁₆(2)
0236₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00₁₆(2)
0237₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00₁₆(2)
0238₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000₂(2) XXX0 0000₂(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Baud Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆ 0311₁₆	Timer B3 Register	TB3	XX₁₆ XX₁₆
0312₁₆ 0313₁₆	Timer B4 Register	TB4	XX₁₆ XX₁₆
0314₁₆ 0315₁₆	Timer B5 Register	TB5	XX₁₆ XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XX16 XX16
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216			
039316			
039416	A/D0 Control Register 2	AD0CON2	X000 00002
039516			
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

VCC=5V

Table 5.4 A/D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, Vss = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	VREF=VCC				10	Bits
INL	Integral Nonlinearity Error	VREF=VCC=5V	AN0 to AN7 ANEX0, ANEX1			±3	LSB LSB
			External op-amp connection mode			±7	LSB LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
RLADDER	Resistor Ladder	VREF=VCC		8		40	kΩ
tCONV	10-bit Conversion Time			2.1			µs
tCONV	8-bit Conversion Time			1.8			µs
tSAMP	Sample Time			0.2			µs
VREF	Reference Voltage			2		VCC	V
VIA	Analog Input Voltage			0		VREF	V

NOTES:
1. Divide f(XIN), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 5.5 D/A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tSU	Setup Time				3	µs
RO	Output Resistance		4	10	20	kΩ
IVREF	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00$_{16}$". The resistor ladder in the A/D converter is exclued. IVREF flows even if the VCUT bit in the ADiCON1 register is set to "0" (no VREF connection).

Table 5.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. VCC= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.9 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

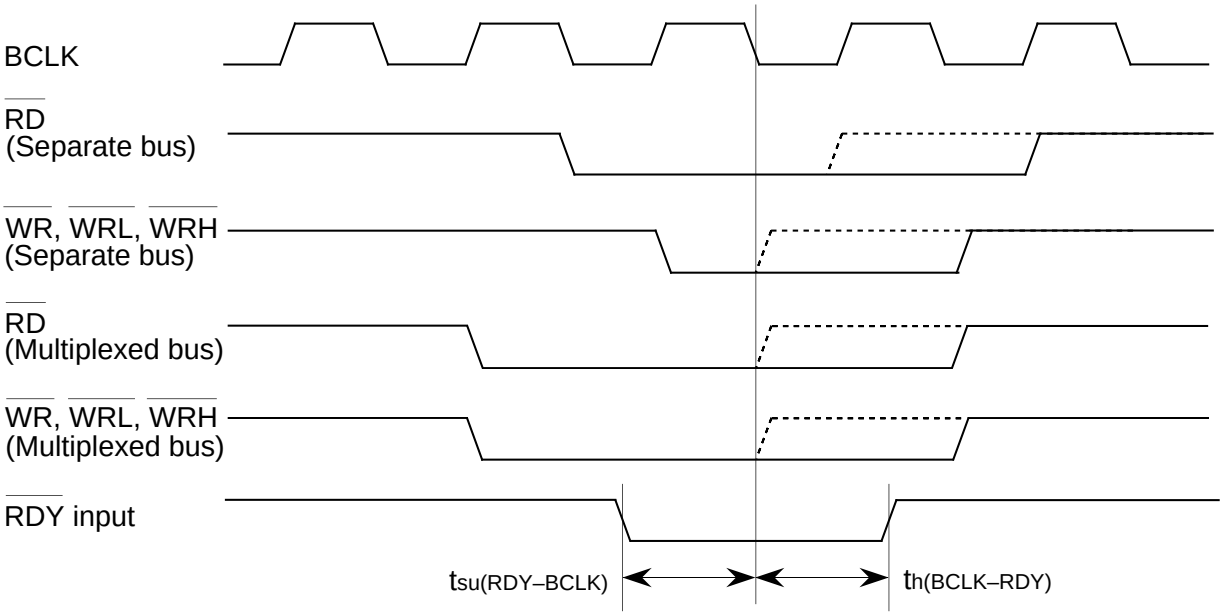
$$td(AD-ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

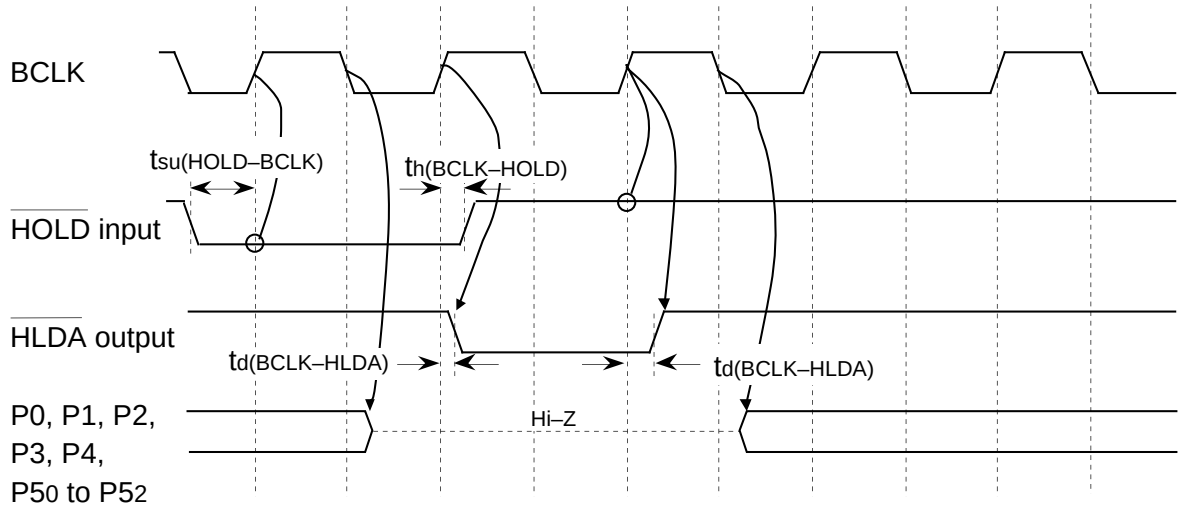
Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state or with no wait state)



Measurement Conditions:

- VCC=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 5.9 Vcc=5V Timing Diagram (8)

VCC=3.3V

Timing Requirements (Vcc = 3.0 to 3.6V, Vss = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.28 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	50		ns
tw(H)	External Clock Input High ("H") Pulse Width	22		ns
tw(L)	External Clock Input Low ("L") Pulse Width	22		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.29 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	30		ns
tsu(RDY-BCLK)	RDY Input Setup Time	40		ns
tsu(HOLD-BCLK)	HOLD Input Setup Time	60		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(CAS-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	RDY Input Hold Time	0		ns
th(BCLK-HOLD)	HOLD Input Hold Time	0		ns
td(BCLK-HLDA)	HLDA Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns]\ (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns]\ (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

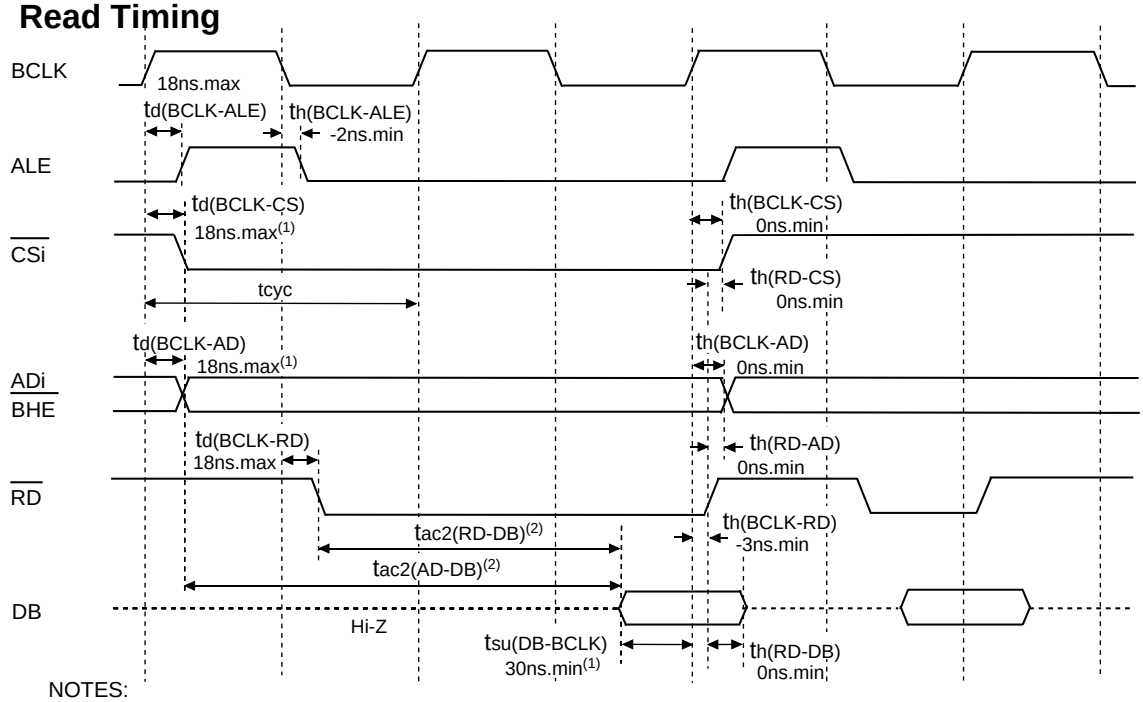
Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with a wait state)

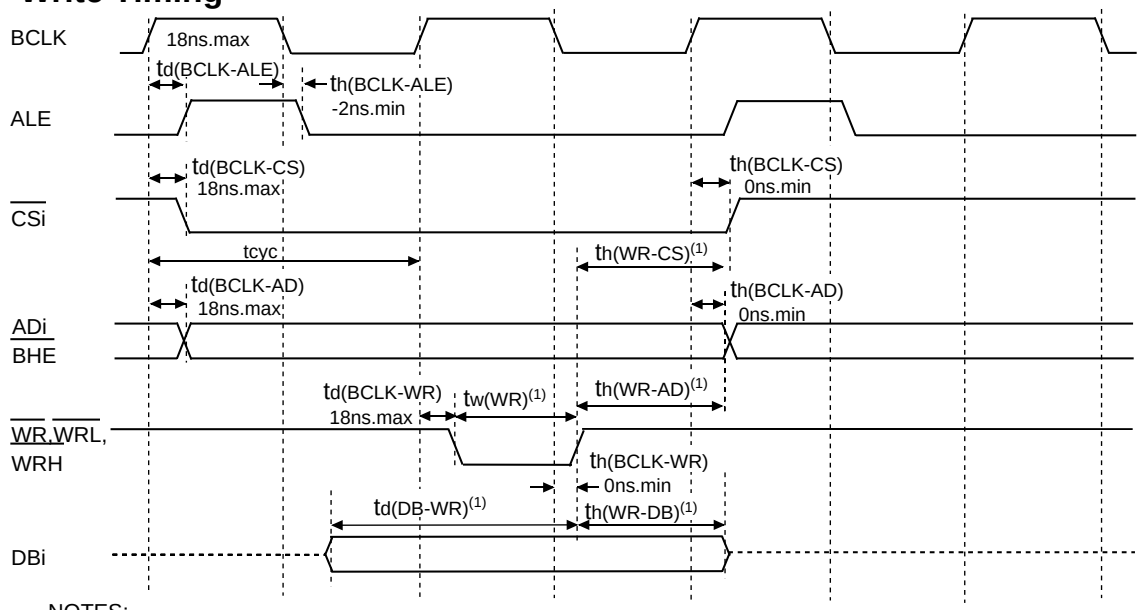
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement Conditions:

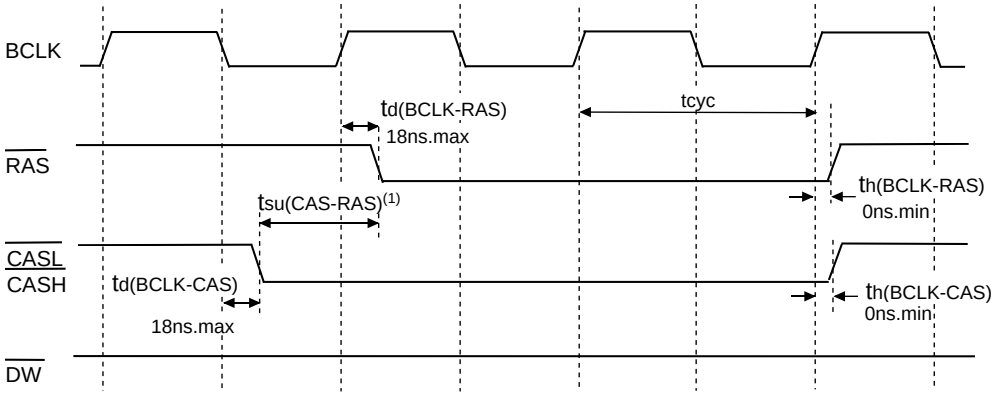
- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

Vcc=3.3V

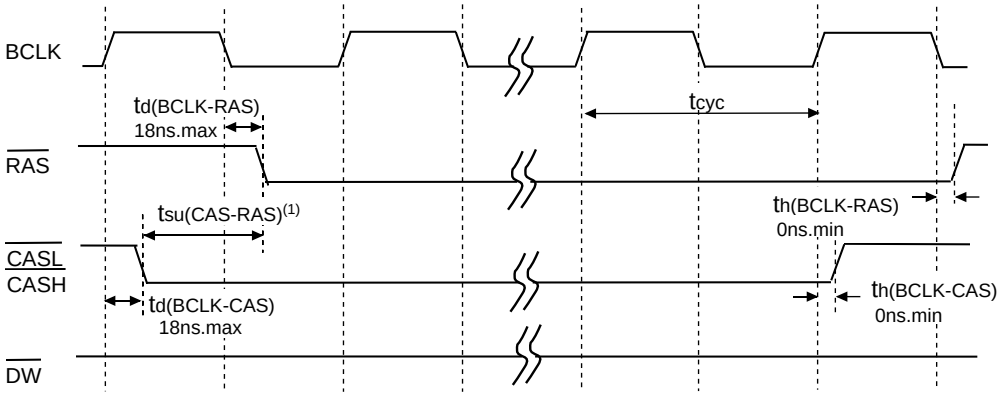
Memory Expansion Mode and Microprocessor Mode

Refresh Timing (CAS-before-RAS refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh Timing (Self-refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement Conditions:
- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.15 V_{CC}=3.3V Timing Diagram (6)

Table 5.46 Recommended Operating Conditions

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		4.2	5.0	5.5	V
AV_{CC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
AV_{SS}	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$	0.8V_{CC}		6.0	
V_{IL}	Input Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	V_{CC}=4.2 to 5.5V	0		32	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)

Table 5.52 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.53 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.54 Timer A Input (External Trigger Input in One-Shot Timer Mode)

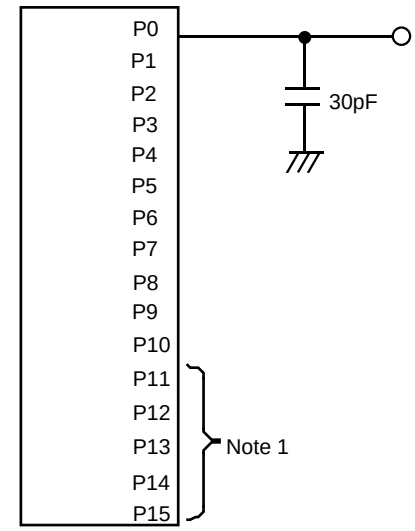
Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.55 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.56 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns



NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.18 P0 to P15 Measurement Circuit

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