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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M32C/80 |
| Core Size | 16/32-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, I²C, IEBus, SIO, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 31K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 26x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30833fjfp-u5 |

## 1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/83 Group (M32C/83, M32C/83T).

**Table 1.1 M32C/83 Group (M32C/83, M32C/83T) Performance (144-Pin Package)**

| Characteristic | | Performance | |
|---|---|---|---|
| | | M32C/83 | M32C/83T |
| CPU | Basic Instructions | 108 instructions | |
| | Minimum Instruction Execution Time | 31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3)<br>50 ns (f(BCLK)=20 MHz, VCC=3.0 to 5.5 V) | 31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3) |
| | Operating Mode | Single-chip mode, Memory expansion mode and Microprocessor mode | Single-chip mode |
| | Address Space | 16 Mbytes | |
| | Memory Capacity | See Table 1.3 | |
| Peripheral Function | I/O Port | 123 I/O pins and 1 input pin | |
| | Multifunction Timer | Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels<br>Three-phase motor control circuit | |
| | Intelligent I/O | Time measurement function: 16 bits x 12 channels<br>Waveform generating function: 16 bits x 28 channels<br>Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1), 8-bit or 16-bit Clock synchronous serial I/O) | |
| | Serial I/O | 5 Channels<br>Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2) | |
| | CAN Module | 1 channel Supporting CAN 2.0B specification | |
| | A/D Converter | 10-bit A/D converter: 2 circuit, 34 channels | |
| | D/A Converter | 8 bits x 2 channels | |
| | DMAC | 4 channels | |
| | DMAC II | Can be activated by all peripheral function interrupt sources<br>Immediate transfer, Calculation transfer and Chain transfer functions | |
| | DRAM | CAS before RAS refresh, Self-reflesh, EDO, EP | |
| | CRC Calculation Circuit | CRC-CCITT | |
| | X/Y Converter | 16 bits x 16 bits | |
| | Watchdog Timer | 15 bits x 1 channel (with prescaler) | |
| | Interrupt | 42 internal and 8 external sources, 5 software sources, Interrupt priority level: 7 | |
| | Clock Generation Circuit | 4 circuits<br>Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer<br>(*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally | |
| | Oscillation Stop Detect Function | Main clock oscillation stop detect function | |
| Electrical Characteristics | Supply Voltage | 4.2 to 5.5 V (f(BCLK)=32 MHz)<br>3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC)<br>3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC) | 4.2 to 5.5 V (f(BCLK)=32 MHz) |
| | Power Consumption | 41 mA (VCC=5 V, f(BCLK)=32 MHz)<br>38 mA (VCC=5 V, f(BCLK)=30 MHz)<br>26 mA (VCC=3.3 V, f(BCLK)=20 MHz)<br>470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode)<br>340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode)<br>5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode)<br>0.4 µA (VCC=5 V, stop mode)<br>0.4 µA (VCC=3.3 V, stop mode) | 41 mA (VCC=5 V, f(BCLK)=32 MHz)<br>38 mA (VCC=5 V, Vf(BCLK)=30 MHz)<br>470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode)<br>0.4 µA (VCC=5 V, stop mode) |
| Flash Memory | Program/Erase Supply Voltage | 3.3 ± 0.3 V or 5.0 ± 0.5 V | 5.0 ± 0.5 V |
| | Program and Erase Endurance | 100 times | |
| Operating Ambient Temperature | | –20 to 85°C, –40 to 85°C (optional) | –40 to 85°C (T version) |
| Package | | 144-pin plastic molded LQFP | |

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

| Classsfication | Symbol | I/O Type | Function |
|---|---|---|---|
| Serial I/O Special Function | STxD0 to STxD4 | O | Outputs serial data when slave mode is selected |
| | SRxD0 to SRxD4 | I | Inputs serial data when slave mode is selected |
| | $\overline{SS0}$ to $\overline{SS4}$ | I | Input pins to control serial I/O special function |
| Reference Voltage Input | VREF | I | Applies reference voltage to the A/D converter and D/A converter |
| A/D Converter | AN0 to AN7<br>AN00 to AN07<br>AN20 to AN27 | I | Analog input pins for the A/D converter |
| | AN150 to AN157 | | |
| | $\overline{ADTRG}$ | I | Input pin for an external A/D trigger |
| | ANEX0 | I/O | Extended analog input pin for the A/D converter and output pin in external op-amp connection mode |
| | ANEX1 | I | Extended analog input pin for the A/D converter |
| D/A Converter | DA0, DA1 | O | Output pin for the D/A converter |
| Intelligent I/O | INPC00 to INPC02 | I | Input pins for the time measurement function |
| | INPC03 to INPC07(1) | | |
| | INPC11 to INPC12 | | |
| | INPC16 to INPC17(1) | | |
| | OUTC00 to OUTC02 | O | Output pins for the waveform generating function<br>(OUTC20 and OUTC22 assigned to P70 and P71 are pins for the N-channel open drain output.) |
| | OUTC04 to OUTC05(1) | | |
| | OUTC10 to OUTC12 | | |
| | OUTC13 to OUTC17(1) | | |
| | OUTC20 to OUTC22 | | |
| | OUTC23 to OUTC27(1) | | |
| | OUTC30 to OUTC32 | | |
| | OUTC31, OUTC33 to OUTC37(1) | | |
| | ISCLK0 to ISCLK2 | I/O | Inputs and outputs the clock for the intelligent I/O communication function |
| | ISCLK3(1) | | |
| | ISRXD0 to ISRXD3 | I | Inputs data for the intelligent I/O communication function |
| | ISTXD0 to ISTXD3 | O | Outputs data for the intelligent I/O communication function |
| | BE0IN, BE1IN | I | Inputs data for the intelligent I/O communication function |
| | BE0OUT, BE1OUT | O | Outputs data for the intelligent I/O communication function |
| | IEIN | I | Inputs data for the intelligent I/O communication function |
| | IEOUT | O | Outputs data for the intelligent I/O communication function |
| CAN | CANIN | I | Input pin for the CAN communication function |
| | CANOUT | O | Output pin for the CAN communication function |

I : Input O : Output I/O : Input and output

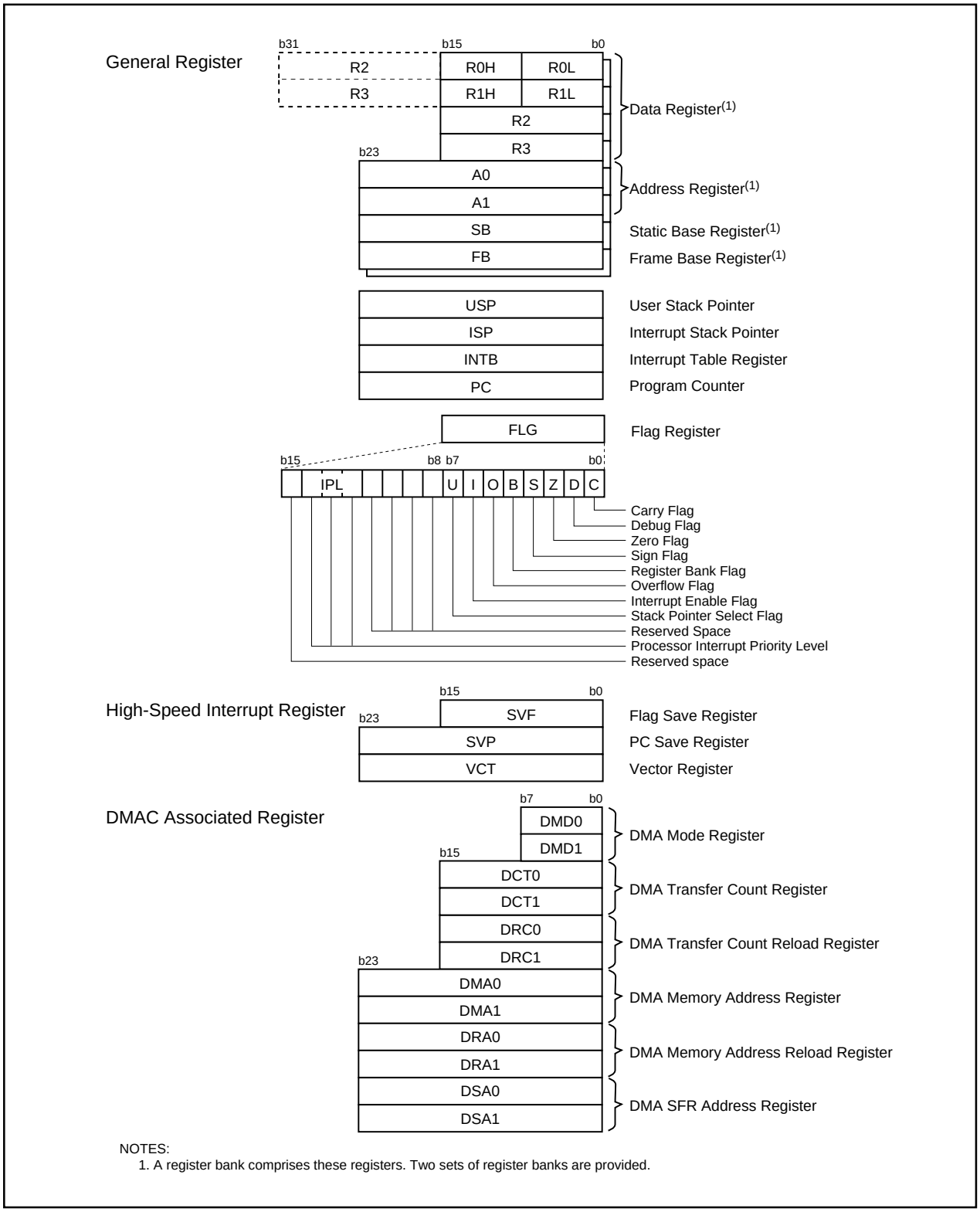
NOTE:

1. Available in the 144-pin package only.

# 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.




NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided.

**Figure 2.1 CPU Register**

# 3. Memory

Figure 3.1 shows a memory map of the M32C/83 group (M32C/83, M32C/83T).

M32C/83 group (M32C/83, M32C/83T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses FF0000$_{16}$ to FFFFFF$_{16}$.

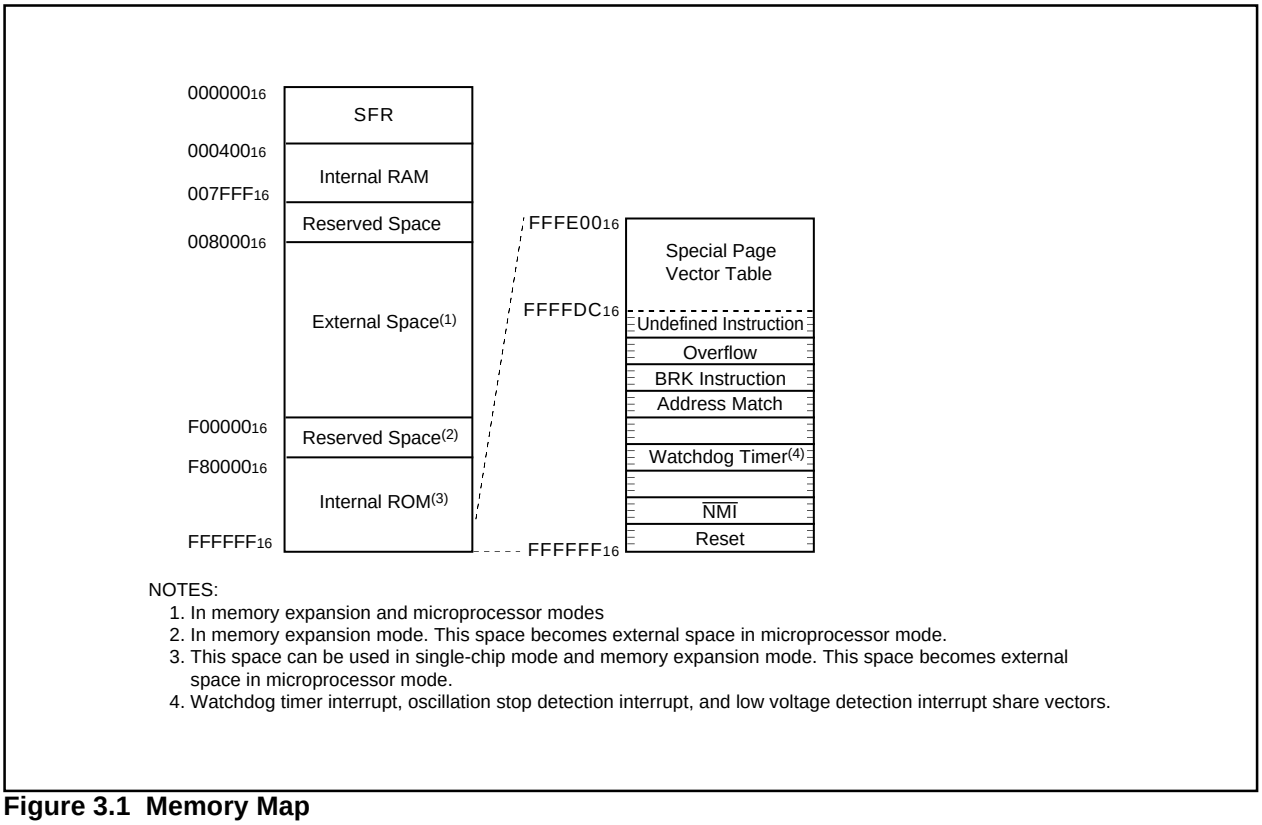
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.




NOTES:
1. In memory expansion and microprocessor modes
2. In memory expansion mode. This space becomes external space in microprocessor mode.
3. This space can be used in single-chip mode and memory expansion mode. This space becomes external space in microprocessor mode.
4. Watchdog timer interrupt, oscillation stop detection interrupt, and low voltage detection interrupt share vectors.

**Figure 3.1 Memory Map**

| Address | Register | Symbol | Value after RESET |
|---|---|---|---|
| 0030₁₆ | | | |
| 0031₁₆ | | | |
| 0032₁₆ | | | |
| 0033₁₆ | | | |
| 0034₁₆ | | | |
| 0035₁₆ | | | |
| 0036₁₆ | | | |
| 0037₁₆ | | | |
| 0038₁₆ | | | |
| 0039₁₆ | | | |
| 003A₁₆ | | | |
| 003B₁₆ | | | |
| 003C₁₆ | | | |
| 003D₁₆ | | | |
| 003E₁₆ | | | |
| 003F₁₆ | | | |
| 0040₁₆ | DRAM Control Register (1) | DRAMCONT | XX₁₆ |
| 0041₁₆ | DRAM Refresh Interval Set Register (1) | REFCNT | XX₁₆ |
| 0042₁₆ | | | |
| 0043₁₆ | | | |
| 0044₁₆ | | | |
| 0045₁₆ | | | |
| 0046₁₆ | | | |
| 0047₁₆ | | | |
| 0048₁₆ | | | |
| 0049₁₆ | | | |
| 004A₁₆ | | | |
| 004B₁₆ | | | |
| 004C₁₆ | | | |
| 004D₁₆ | | | |
| 004E₁₆ | | | |
| 004F₁₆ | | | |
| 0050₁₆ | | | |
| 0051₁₆ | | | |
| 0052₁₆ | | | |
| 0053₁₆ | | | |
| 0054₁₆ | | | |
| 0055₁₆ | | | |
| 0056₁₆ | | | |
| 0057₁₆ | Flash Memory Control Register 0 | FMR0 | XX00 0001₂ |
| 0058₁₆ | | | |
| 0059₁₆ | | | |
| 005A₁₆ | | | |
| 005B₁₆ | | | |
| 005C₁₆ | | | |
| 005D₁₆ | | | |
| 005E₁₆ | | | |
| 005F₁₆ | | | |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/83T cannot be used.

| Address | Register | Symbol | Value after RESET |
|---|---|---|---|
| 018016<br>018116 | Group 3 Waveform Generating Register 0 | G3PO0 | XX16<br>XX16 |
| 018216<br>018316 | Group 3 Waveform Generating Register 1 | G3PO1 | XX16<br>XX16 |
| 018416<br>018516 | Group 3 Waveform Generating Register 2 | G3PO2 | XX16<br>XX16 |
| 018616<br>018716 | Group 3 Waveform Generating Register 3 | G3PO3 | XX16<br>XX16 |
| 018816<br>018916 | Group 3 Waveform Generating Register 4 | G3PO4 | XX16<br>XX16 |
| 018A16<br>018B16 | Group 3 Waveform Generating Register 5 | G3PO5 | XX16<br>XX16 |
| 018C16<br>018D16 | Group 3 Waveform Generating Register 6 | G3PO6 | XX16<br>XX16 |
| 018E16<br>018F16 | Group 3 Waveform Generating Register 7 | G3PO7 | XX16<br>XX16 |
| 019016 | Group 3 Waveform Generating Control Register 0 | G3POCR0 | 0016 |
| 019116 | Group 3 Waveform Generating Control Register 1 | G3POCR1 | 0016 |
| 019216 | Group 3 Waveform Generating Control Register 2 | G3POCR2 | 0016 |
| 019316 | Group 3 Waveform Generating Control Register 3 | G3POCR3 | 0016 |
| 019416 | Group 3 Waveform Generating Control Register 4 | G3POCR4 | 0016 |
| 019516 | Group 3 Waveform Generating Control Register 5 | G3POCR5 | 0016 |
| 019616 | Group 3 Waveform Generating Control Register 6 | G3POCR6 | 0016 |
| 019716 | Group 3 Waveform Generating Control Register 7 | G3POCR7 | 0016 |
| 019816<br>019916 | Group 3 Waveform Generating Mask Register 4 | G3MK4 | XX16<br>XX16 |
| 019A16<br>019B16 | Group 3 Waveform Generating Mask Register 5 | G3MK5 | XX16<br>XX16 |
| 019C16<br>019D16 | Group 3 Waveform Generating Mask Register 6 | G3MK6 | XX16<br>XX16 |
| 019E16<br>019F16 | Group 3 Waveform Generating Mask Register 7 | G3MK7 | XX16<br>XX16 |
| 01A016<br>01A116 | Group 3 Base Timer Register | G3BT | XX16<br>XX16 |
| 01A216 | Group 3 Base Timer Control Register 0 | G3BCR0 | 0016 |
| 01A316 | Group 3 Base Timer Control Register 1 | G3BCR1 | 0016 |
| 01A416 | | | |
| 01A516 | | | |
| 01A616 | Group 3 Function Enable Register | G3FE | 0016 |
| 01A716 | Group 3 RTP Output Buffer Register | G3RTP | 0016 |
| 01A816 | | | |
| 01A916 | | | |
| 01AA16 | | | |
| 01AB16 | | | |
| 01AC16 | | | |
| 01AD16 | Group 3 SI/O Communication Flag Register | G3FLG | XXXX XXX02 |
| 01AE16 | | | |
| 01AF16 | | | |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

| Address | Register | Symbol | Value after RESET |
|---|---|---|---|
| 01E016 | CAN0 Message Slot Buffer 0 Standard ID0 | C0SLOT0_0 | XX16 |
| 01E116 | CAN0 Message Slot Buffer 0 Standard ID1 | C0SLOT0_1 | XX16 |
| 01E216 | CAN0 Message Slot Buffer 0 Extended ID0 | C0SLOT0_2 | XX16 |
| 01E316 | CAN0 Message Slot Buffer 0 Extended ID1 | C0SLOT0_3 | XX16 |
| 01E416 | CAN0 Message Slot Buffer 0 Extended ID2 | C0SLOT0_4 | XX16 |
| 01E516 | CAN0 Message Slot Buffer 0 Data Length Code | C0SLOT0_5 | XX16 |
| 01E616 | CAN0 Message Slot Buffer 0 Data 0 | C0SLOT0_6 | XX16 |
| 01E716 | CAN0 Message Slot Buffer 0 Data 1 | C0SLOT0_7 | XX16 |
| 01E816 | CAN0 Message Slot Buffer 0 Data 2 | C0SLOT0_8 | XX16 |
| 01E916 | CAN0 Message Slot Buffer 0 Data 3 | C0SLOT0_9 | XX16 |
| 01EA16 | CAN0 Message Slot Buffer 0 Data 4 | C0SLOT0_10 | XX16 |
| 01EB16 | CAN0 Message Slot Buffer 0 Data 5 | C0SLOT0_11 | XX16 |
| 01EC16 | CAN0 Message Slot Buffer 0 Data 6 | C0SLOT0_12 | XX16 |
| 01ED16 | CAN0 Message Slot Buffer 0 Data 7 | C0SLOT0_13 | XX16 |
| 01EE16 | CAN0 Message Slot Buffer 0 Time Stamp High-Order | C0SLOT0_14 | XX16 |
| 01EF16 | CAN0 Message Slot Buffer 0 Time Stamp Low-Order | C0SLOT0_15 | XX16 |
| 01F016 | CAN0 Message Slot Buffer 1 Standard ID0 | C0SLOT1_0 | XX16 |
| 01F116 | CAN0 Message Slot Buffer 1 Standard ID1 | C0SLOT1_1 | XX16 |
| 01F216 | CAN0 Message Slot Buffer 1 Extended ID0 | C0SLOT1_2 | XX16 |
| 01F316 | CAN0 Message Slot Buffer 1 Extended ID1 | C0SLOT1_3 | XX16 |
| 01F416 | CAN0 Message Slot Buffer 1 Extended ID2 | C0SLOT1_4 | XX16 |
| 01F516 | CAN0 Message Slot Buffer 1 Data Length Code | C0SLOT1_5 | XX16 |
| 01F616 | CAN0 Message Slot Buffer 1 Data 0 | C0SLOT1_6 | XX16 |
| 01F716 | CAN0 Message Slot Buffer 1 Data 1 | C0SLOT1_7 | XX16 |
| 01F816 | CAN0 Message Slot Buffer 1 Data 2 | C0SLOT1_8 | XX16 |
| 01F916 | CAN0 Message Slot Buffer 1 Data 3 | C0SLOT1_9 | XX16 |
| 01FA16 | CAN0 Message Slot Buffer 1 Data 4 | C0SLOT1_10 | XX16 |
| 01FB16 | CAN0 Message Slot Buffer 1 Data 5 | C0SLOT1_11 | XX16 |
| 01FC16 | CAN0 Message Slot Buffer 1 Data 6 | C0SLOT1_12 | XX16 |
| 01FD16 | CAN0 Message Slot Buffer 1 Data 7 | C0SLOT1_13 | XX16 |
| 01FE16 | CAN0 Message Slot Buffer 1 Time Stamp High-Order | C0SLOT1_14 | XX16 |
| 01FF16 | CAN0 Message Slot Buffer 1 Time Stamp Low-Order | C0SLOT1_15 | XX16 |
| 020016<br>020116 | CAN0 Control Register 0 | C0CTLR0 | XX01 0X012(1)<br>XXXX 00002(1) |
| 020216<br>020316 | CAN0 Status Register | C0STR | 0000 00002(1)<br>X000 0X012(1) |
| 020416<br>020516 | CAN0 Extended ID Register | C0IDR | 0016(1)<br>0016(1) |
| 020616<br>020716 | CAN0 Configuration Register | C0CONR | 0000 XXXX2(1)<br>0000 00002(1) |
| 020816<br>020916 | CAN0 Time Stamp Register | C0TSR | 0016(1)<br>0016(1) |
| 020A16 | CAN0 Transmit Error Count Register | C0TEC | 0016(1) |
| 020B16 | CAN0 Receive Error Count Register | C0REC | 0016(1) |
| 020C16<br>020D16 | CAN0 Slot Interrupt Status Register | C0SISTR | 0016(1)<br>0016(1) |
| 020E16 | | | |
| 020F16 | | | |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

| Address | Register | Symbol | Value after RESET |
|---|---|---|---|
| 023916 | CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1 | C0MCTL9/ C0LMBR1 | 0000 00002(2) XX00 00002(2) |
| 023A16 | CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0 | C0MCTL10/ C0LMBR2 | 0000 00002(2) XXXX 00002(2) |
| 023B16 | CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1 | C0MCTL11/ C0LMBR3 | 0016(2) 0016(2) |
| 023C16 | CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2 | C0MCTL12/ C0LMBR4 | 0000 00002(2) XX00 00002(2) |
| 023D16 | CAN0 Message Slot 13 Control Register | C0MCTL13 | 0016(2) |
| 023E16 | CAN0 Message Slot 14 Control Register | C0MCTL14 | 0016(2) |
| 023F16 | CAN0 Message Slot 15 Control Register | C0MCTL15 | 0016(2) |
| 024016 | CAN0 Slot Buffer Select Register | C0SBS | 0016(2) |
| 024116 | CAN0 Control Register 1 | C0CTLR1 | XX00 00XX2(2) |
| 024216 | CAN0 Sleep Control Register | C0SLPR | XXXX XXX02 |
| 024316 | | | |
| 024416 | CAN0 Acceptance Filter Support Register | C0AFS | 0016(2) |
| 024516 | | | 0116(2) |
| 024616 | | | |
| 024716 | | | |
| 024816 | | | |
| 024916 | | | |
| 024A16 | | | |
| 024B16 | | | |
| 024C16 | | | |
| 024D16 | | | |
| 024E16 | | | |
| 024F16 | | | |
| 025016 | | | |
| 025116 | | | |
| 025216 | | | |
| 025316 | | | |
| 025416 | | | |
| 025516 | | | |
| 025616 | | | |
| 025716 | | | |
| 025816 | | | |
| 025916 | | | |
| 025A16 | | | |
| 025B16 | | | |
| 025C16 | | | |
| 025D16 | | | |
| 025E16 | | | |
| 025F16 | | | |
| 026016 | | | |
| 026116 to 02BF16 | | | |

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

<100-pin package>

| Address | Register | Symbol | Value after RESET | |
|---|---|---|---|---|
| 03A016 | | | | (Note 2) |
| 03A116 | | | | |
| 03A216 | | | | |
| 03A316 | | | | |
| 03A416 | | | | |
| 03A516 | | | | |
| 03A616 | | | | |
| 03A716 | | | | |
| 03A816 | | | | |
| 03A916 | | | | |
| 03AA16 | | | | |
| 03AB16 | | | | |
| 03AC16 | | | | |
| 03AD16 | | | | |
| 03AE16 | | | | |
| 03AF16 | Function Select Register C | PSC | 0X00 00002 | |
| 03B016 | Function Select Register A0 | PS0 | 0016 | |
| 03B116 | Function Select Register A1 | PS1 | 0016 | |
| 03B216 | Function Select Register B0 | PSL0 | 0016 | |
| 03B316 | Function Select Register B1 | PSL1 | 0016 | |
| 03B416 | Function Select Register A2 | PS2 | 00X0 00002 | |
| 03B516 | Function Select Register A3 | PS3 | 0016 | |
| 03B616 | Function Select Register B2 | PSL2 | 00X0 00002 | |
| 03B716 | Function Select Register B3 | PSL3 | 0016 | |
| 03B816 | | | | |
| 03B916 | | | | (Note 2) |
| 03BA16 | | | | |
| 03BB16 | | | | |
| 03BC16 | | | | (Note 2) |
| 03BD16 | | | | |
| 03BE16 | | | | |
| 03BF16 | | | | |
| 03C016 | Port P6 Register | P6 | XX16 | |
| 03C116 | Port P7 Register | P7 | XX16 | |
| 03C216 | Port P6 Direction Register | PD6 | 0016 | |
| 03C316 | Port P7 Direction Register | PD7 | 0016 | |
| 03C416 | Port P8 Register | P8 | XX16 | |
| 03C516 | Port P9 Register | P9 | XX16 | |
| 03C616 | Port P8 Direction Register | PD8 | 00X0 00002 | |
| 03C716 | Port P9 Direction Register | PD9 | 0016 | |
| 03C816 | Port P10 Register | P10 | XX16 | |
| 03C916 | | | | (Note 2) |
| 03CA16 | Port P10 Direction Register | PD10 | 0016 | |
| 03CB16 | | | | (Note 1) |
| 03CC16 | | | | (Note 2) |
| 03CD16 | | | | |
| 03CE16 | | | | (Note 1) |
| 03CF16 | | | | |

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03CB16, 03CE16 and 03CF16 to "FF16" in the 100-pin package.
2. Address spaces 03A016, 03A116, 03B916, 03BC16, 03BD16, 03C916, 03CC16 and 03CD16 are not provided in the 100-pin package.

VCC=5V

**Table 5.4 A/D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, Vss = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)**

| Symbol | Parameter | Measurement Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| - | Resolution | VREF=VCC | | | | 10 | Bits |
| INL | Integral Nonlinearity Error | VREF=VCC=5V | AN0 to AN7<br>ANEX0, ANEX1 | | | ±3 | LSB<br>LSB |
| | | | External op-amp connection mode | | | ±7 | LSB<br>LSB |
| DNL | Differential Nonlinearity Error | | | | | ±1 | LSB |
| - | Offset Error | | | | | ±3 | LSB |
| - | Gain Error | | | | | ±3 | LSB |
| RLADDER | Resistor Ladder | VREF=VCC | | 8 | | 40 | kΩ |
| tCONV | 10-bit Conversion Time | | | 2.1 | | | µs |
| tCONV | 8-bit Conversion Time | | | 1.8 | | | µs |
| tSAMP | Sample Time | | | 0.2 | | | µs |
| VREF | Reference Voltage | | | 2 | | VCC | V |
| VIA | Analog Input Voltage | | | 0 | | VREF | V |

NOTES:
1. Divide f(XIN), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

**Table 5.5 D/A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)**

| Symbol | Parameter | Measurement Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| - | Resolution | | | | 8 | Bits |
| - | Absolute Accuracy | | | | 1.0 | % |
| tSU | Setup Time | | | | 3 | µs |
| RO | Output Resistance | | 4 | 10 | 20 | kΩ |
| IVREF | Reference Power Supply Input Current | (Note 1) | | | 1.5 | mA |

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00$_{16}$". The resistor ladder in the A/D converter is exclued. IVREF flows even if the VCUT bit in the ADiCON1 register is set to "0" (no VREF connection).

**Table 5.6 Flash Memory Version Electrical Characteristics**

| Parameter | Standard | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Program Time (per page) | | 8 | 120 | ms |
| Block Erase Time (per block) | | 50 | 600 | ms |

NOTES:
1. VCC= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

$V_{CC}$=5V

### Timing Requirements

**($V_{CC}$ = 4.2 to 5.5V, $V_{SS}$ = 0V at Topr = –20 to 85°C unless otherwise specified)**

#### Table 5.14 Timer B Input (Count Source Input in Event Counter Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(TB)}$ | $TBi_{IN}$ Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | $TBi_{IN}$ Input High ("H") Pulse Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | $TBi_{IN}$ Input Low ("L") Pulse Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | $TBi_{IN}$ Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | $TBi_{IN}$ Input High ("H") Pulse Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | $TBi_{IN}$ Input Low ("L") Pulse Width (counted on both edges) | 80 | | ns |

#### Table 5.15 Timer B Input (Pulse Period Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(TB)}$ | $TBi_{IN}$ Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | $TBi_{IN}$ Input High ("H") Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | $TBi_{IN}$ Input Low ("L") Pulse Width | 200 | | ns |

#### Table 5.16 Timer B Input (Pulse Width Measurement Mode)

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(TB)}$ | $TBi_{IN}$ Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | $TBi_{IN}$ Input High ("H") Pulse Width | 200 | | ns |
| $t_{w(TBL)}$ | $TBi_{IN}$ Input Low ("L") Pulse Width | 200 | | ns |

#### Table 5.17 A/D Trigger Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(AD)}$ | $\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger) | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{AD_{TRG}}$ Input Low ("L") Pulse Width | 125 | | ns |

#### Table 5.18 Serial I/O

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input High ("H") Pulse Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input Low ("L") Pulse Width | 100 | | ns |
| $t_{d(C-Q)}$ | TxDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TxDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RxDi Input Set Up Time | 30 | | ns |
| $t_{h(C-Q)}$ | RxDi Input Hold Time | 90 | | ns |

#### Table 5.19 External Interrupt $\overline{INTi}$ Input

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{w(INH)}$ | $\overline{INTi}$ Input High ("H") Pulse Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{INTi}$ Input Low ("L") Pulse Width | 250 | | ns |

VCC=3.3V

**Table 5.24 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = –20 to 85°C, f(XIN)=20MHz unless otherwise specified)**

| Symbol | Parameter | | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| VOH | Output High ("H") Voltage | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1) | IOH=-1mA | Vcc-0.6 | | | V |
| | | XOUT | IOH=-0.1mA | 2.7 | | | V |
| | | XCOUT | No load applied | | 3.3 | | V |
| VOL | Output Low ("L") Voltage | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1) | IOL=1mA | | | 0.5 | V |
| | | XOUT | IOL=0.1mA | | | 0.5 | V |
| | | XCOUT | No load applied | | 0 | | V |
| VT+-VT- | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0IN-TA4IN, TB0IN-TB5IN, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0OUT-TA4OUT, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4 | | 0.2 | | 1.0 | V |
| | | $\overline{RESET}$ | | 0.2 | | 1.8 | V |
| IIH | Input High ("H") Current | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE | VI=3V | | | 4.0 | µA |
| IIL | Input Low ("L") Current | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE | VI=0V | | | -4.0 | µA |
| RPULLUP | Pull-up Resistance | P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1) | VI=0V | 66 | 120 | 500 | kΩ |
| RfXIN | Feedback Resistance | XIN | | | 3.0 | | MΩ |
| RfXCIN | Feedback Resistance | XCIN | | | 20.0 | | MΩ |
| VRAM | RAM Standby Voltage | Through VDC | | 2.5 | | | V |
| | | Not through VDC | | 2.0 | | | V |
| ICC | Power Supply Current | Measurement condition: In single-chip mode, output pins are left open and other pins are connected to VSS. | f(XIN)=20 MHz, square wave, no division | | 26 | 38 | mA |
| | | | f(XCIN)=32 kHz, with a wait state, not through VDC, Topr=25° C | | 5.0 | | µA |
| | | | f(XCIN)=32 kHz, with a wait state, through VDC, Topr=25° C | | 340 | | µA |
| | | | Topr=25° C when the clock stops | | 0.4 | 20 | µA |

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=3.3V

Timing Requirements (Vcc = 3.0 to 3.6V, Vss = 0V at Topr = –20 to 85°C unless otherwise specified)

**Table 5.28 External Clock Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tc | External Clock Input Cycle Time | 50 | | ns |
| tw(H) | External Clock Input High ("H") Pulse Width | 22 | | ns |
| tw(L) | External Clock Input Low ("L") Pulse Width | 22 | | ns |
| tr | External Clock Rise Time | | 5 | ns |
| tf | External Clock Fall Time | | 5 | ns |

**Table 5.29 Memory Expansion Mode and Microprocessor Mode**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tac1(RD-DB) | Data Input Access Time (RD standard, with no wait state) | | (Note 1) | ns |
| tac1(AD-DB) | Data Input Access Time (AD standard, CS standard, with no wait state) | | (Note 1) | ns |
| tac2(RD-DB) | Data Input Access Time (RD standard, with a wait state) | | (Note 1) | ns |
| tac2(AD-DB) | Data Input Access Time (AD standard, CS standard, with a wait state) | | (Note 1) | ns |
| tac3(RD-DB) | Data Input Access Time (RD standard, when accessing a space with the multiplexed bus) | | (Note 1) | ns |
| tac3(AD-DB) | Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus) | | (Note 1) | ns |
| tac4(RAS-DB) | Data Input Access Time (RAS standard, when accessing a DRAM space) | | (Note 1) | ns |
| tac4(CAS-DB) | Data Input Access Time (CAS standard, when accessing a DRAM space) | | (Note 1) | ns |
| tac4(CAD-DB) | Data Input Access Time (CAD standard, when accessing a DRAM space) | | (Note 1) | ns |
| tsu(DB-BCLK) | Data Input Setup Time | 30 | | ns |
| tsu(RDY-BCLK) | RDY Input Setup Time | 40 | | ns |
| tsu(HOLD-BCLK) | HOLD Input Setup Time | 60 | | ns |
| th(RD-DB) | Data Input Hold Time | 0 | | ns |
| th(CAS-DB) | Data Input Hold Time | 0 | | ns |
| th(BCLK-RDY) | RDY Input Hold Time | 0 | | ns |
| th(BCLK-HOLD) | HOLD Input Hold Time | 0 | | ns |
| td(BCLK-HLDA) | HLDA Output Delay Time | | 25 | ns |

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns]\ (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns]\ (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC=3.3V

**Switching Characteristics**

**(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C, unless otherwise specified)**

**Table 5.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

| Symbol | Parameter | Measurement Condition | Standard | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{d(BCLK-AD)}$ | Address Output Delay Time | See Figure 5.1 | | 18 | ns |
| $t_{h(BCLK-AD)}$ | Address Output Hold Time (BCLK standard) | | 0 | | ns |
| $t_{h(RD-AD)}$ | Address Output Hold Time (RD standard) | | 0 | | ns |
| $t_{h(WR-AD)}$ | Address Output Hold Time (WR standard) | | (Note 1) | | ns |
| $t_{d(BCLK-CS)}$ | Chip-select Signal Output Delay Time | | | 18 | ns |
| $t_{h(BCLK-CS)}$ | Chip-select Signal Output Hold Time (BCLK standard) | | 0 | | ns |
| $t_{h(RD-CS)}$ | Chip-select Signal Output Hold Time (RD standard) | | 0 | | ns |
| $t_{h(WR-CS)}$ | Chip-select Signal Output Hold Time (WR standard) | | (Note 1) | | ns |
| $t_{d(BCLK-ALE)}$ | ALE Signal Output Delay Time | | | 18 | ns |
| $t_{h(BCLK-ALE)}$ | ALE Signal Output Hold Time | | -2 | | ns |
| $t_{d(BCLK-RD)}$ | RD Signal Output Delay Time | | | 18 | ns |
| $t_{h(BCLK-RD)}$ | RD Signal Output Hold Time | | -3 | | ns |
| $t_{d(BCLK-WR)}$ | WR Signal Output Delay Time | | | 18 | ns |
| $t_{h(BCLK-WR)}$ | WR Signal Output Hold Time | | 0 | | ns |
| $t_{d(DB-WR)}$ | Data Output Delay Time (WR standard) | | (Note 1) | | ns |
| $t_{h(WR-DB)}$ | Data Output Hold Time (WR standard) | | (Note 1) | | ns |
| $t_{w(WR)}$ | WR Output Width | | (Note 1) | | ns |

NOTES:

1. Values can be obtained from the following equations according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

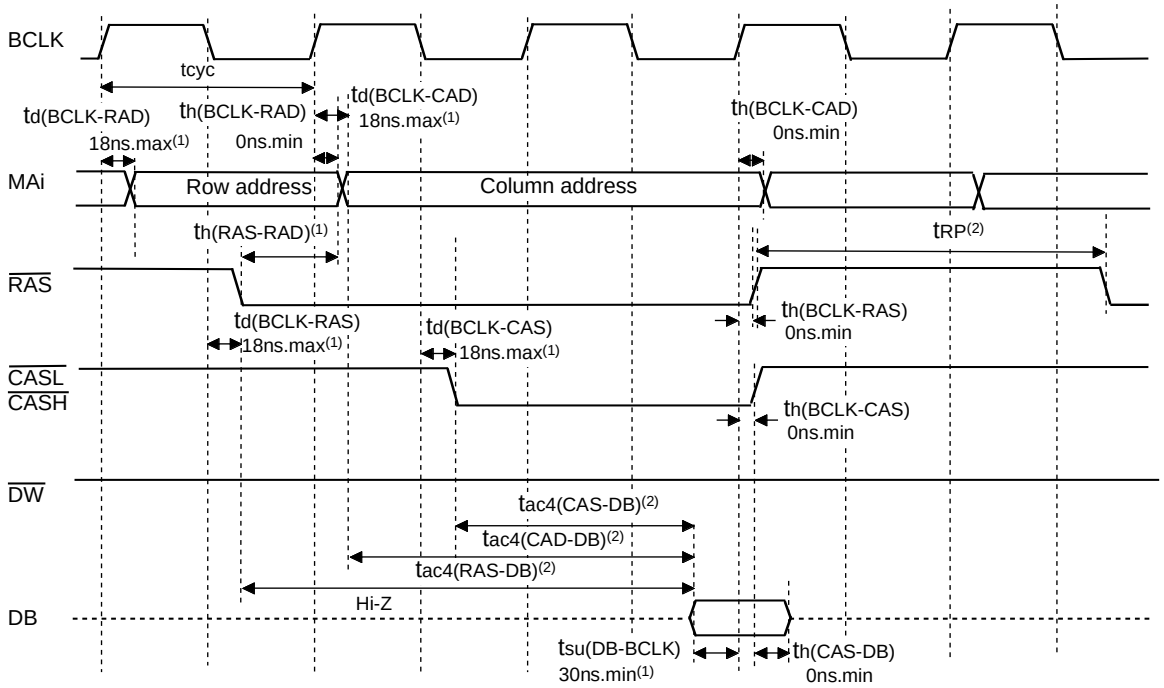
$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

Vcc=3.3V

## Memory Expansion Mode and Microprocessor Mode

**(With 2 wait states, when accessing the DRAM area)**

### Read Timing




NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for the followings:
   $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. It varies with the operation frequency.
   $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   $t_{RP}$=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- $V_{CC}$=3.0 to 3.6V
- Input high and low voltage: $V_{IH}$=1.5V, $V_{IL}$=0.5V
- Output high and low voltage: $V_{OH}$=1.5V, $V_{OL}$=1.5V

**Figure 5.13 $V_{CC}$=3.3V Timing Diagram (4)**

## 5.2 Electrical Characteristics (M32C/83T)

### Table 5.45 Absolute Maximum Ratings

| Symbol | Parameter | | Condition | Value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | $V_{CC}$=$AV_{CC}$ | -0.3 to 6.0 | V |
| $AV_{CC}$ | Analog Supply Voltage | | $V_{CC}$=$AV_{CC}$ | -0.3 to 6.0 | V |
| $V_I$ | Input Voltage | $\overline{RESET}$, $CNV_{SS}$, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), $V_{REF}$, $X_{IN}$ | | -0.3 to $V_{CC}$+0.3 | V |
| | | $P7_0$, $P7_1$ | | -0.3 to 6.0 | V |
| $V_O$ | Output Voltage | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), $X_{OUT}$ | | -0.3 to $V_{CC}$+0.3 | V |
| Pd | Power Dissipation | | Topr=25° C | 400 | mW |
| Topr | Operating Ambient Temperature | | T version | -40 to 85 | ° C |
| Tstg | Storage Temperature | | | -65 to 150 | ° C |

NOTES:
1. P11 to P15 are provided in the 144-pin package.

**Table 5.46 Recommended Operating Conditions**

**($V_{CC}$=4.2 to 5.5V, $V_{SS}$=0V at Topr = -40 to 85°C (T version) unless otherwise specified)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply Voltage | | 4.2 | 5.0 | 5.5 | V |
| $AV_{CC}$ | Analog Supply Voltage | | | $V_{CC}$ | | V |
| $V_{SS}$ | Supply Voltage | | | 0 | | V |
| $AV_{SS}$ | Analog Supply Voltage | | | 0 | | V |
| $V_{IH}$ | Input High ("H") Voltage | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| | | $P7_0$, $P7_1$ | 0.8$V_{CC}$ | | 6.0 | |
| $V_{IL}$ | Input Low ("L") Voltage | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0 | | 0.2$V_{CC}$ | V |
| $I_{OH(peak)}$ | Peak Output High ("H") Current(2) | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4) | | | -10.0 | mA |
| $I_{OH(avg)}$ | Average Output High ("H") Current(1) | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4) | | | -5.0 | mA |
| $I_{OL(peak)}$ | Peak Output Low ("L") Current(2) | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4) | | | 10.0 | mA |
| $I_{OL(avg)}$ | Average Output Low ("L") Current(1) | $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4) | | | 5.0 | mA |
| $f(X_{IN})$ | Main Clock Input Frequency | $V_{CC}$=4.2 to 5.5V | 0 | | 32 | MHz |
| $f(X_{CIN})$ | Sub Clock Oscillation Frequency | | | 32.768 | 50 | kHz |

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. $V_{IH}$ and $V_{IL}$ reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as $X_{CIN}$.
4. P11 to P15 are provided in the 144-pin package only.

VCC=5V

**Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)**

**Table 5.51 External Clock Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tc | External Clock Input Cycle Time | 33 | | ns |
| $tw_{(H)}$ | External Clock Input High ("H") Pulse Width | 13 | | ns |
| $tw_{(L)}$ | External Clock Input Low ("L") Pulse Width | 13 | | ns |
| tr | External Clock Rise Time | | 5 | ns |
| tf | External Clock Fall Time | | 5 | ns |

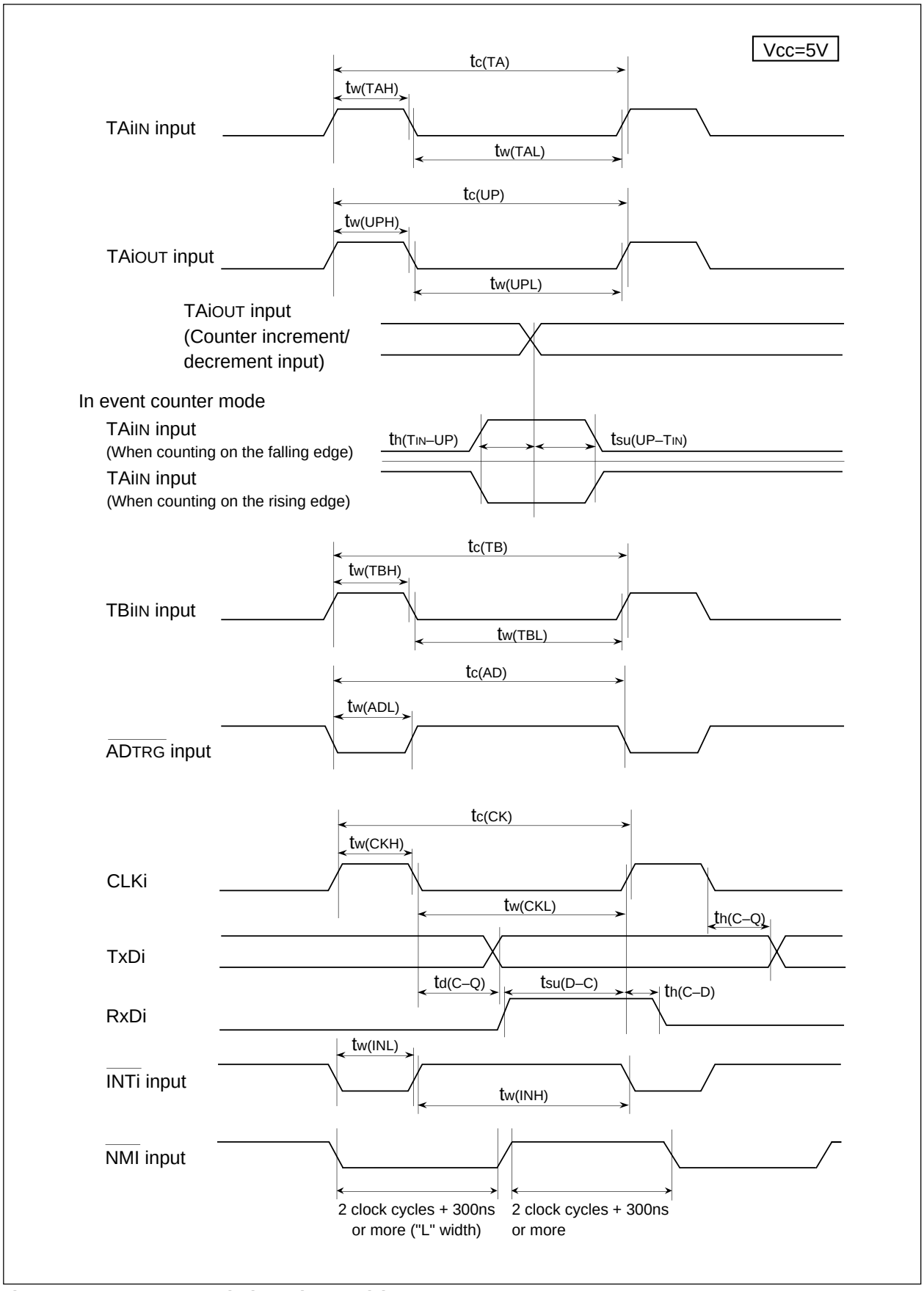


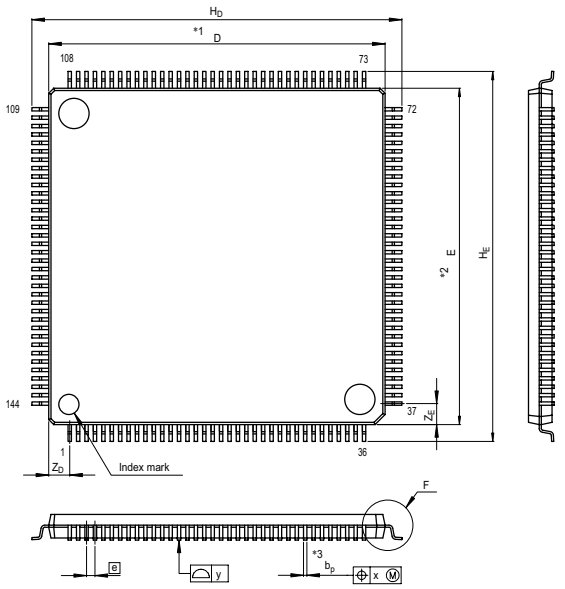

**Figure 5.19 VCC = 5 V Timing Diagram(1)**

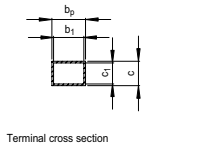
# Package Dimensions

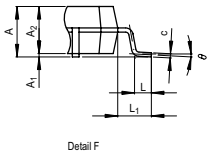
## PLQ0144KA-A (144P6Q-A)

**Plastic 144pin 20 X 20 mm body LQFP**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP144-20x20-0.50 | PLQP0144KA-A | 144P6Q-A / FP-144L / FP-144LV | 1.2g |



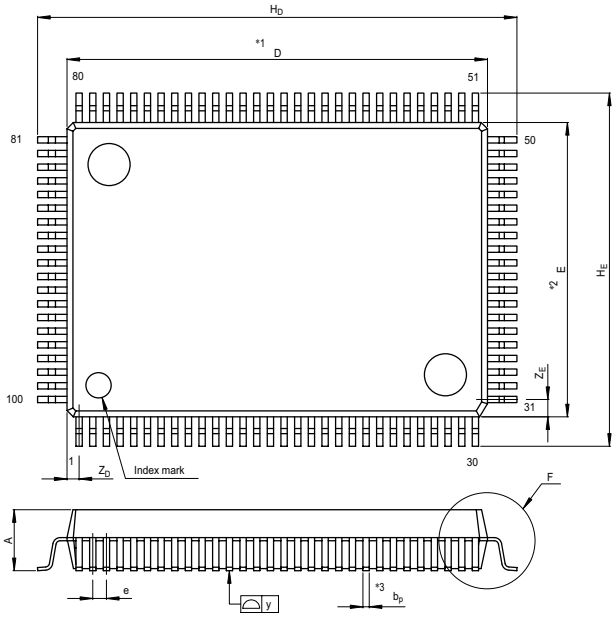

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

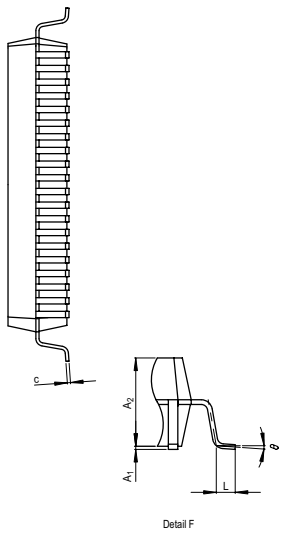
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

## PRQP0100JB-A (100P6S-A)

**Plastic 100pin 14 X 20 mm body LQFP**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-QFP100-14x20-0.65 | PRQP0100JB-A | 100P6S-A | 1.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.8 | 20.0 | 20.2 |
| E | 13.8 | 14.0 | 14.2 |
| $A_2$ | — | 2.8 | — |
| $H_D$ | 22.5 | 22.8 | 23.1 |
| $H_E$ | 16.5 | 16.8 | 17.1 |
| A | — | — | 3.05 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| θ | 0° | — | 10° |
| e | 0.5 | 0.65 | 0.8 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.825 | — |
| L | 0.4 | 0.6 | 0.8 |