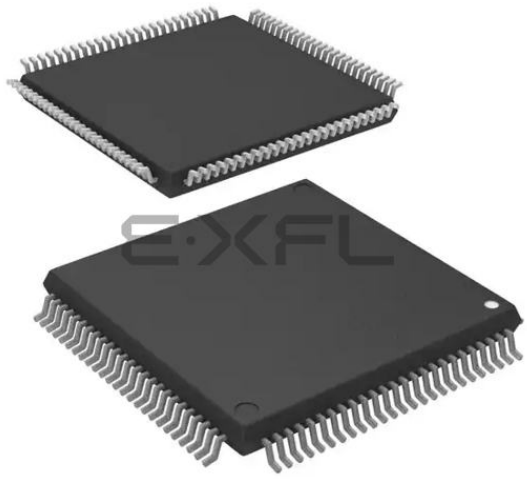
Renesas Electronics America Inc - M30833FJGP#U3 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30833fjgp-u3

REJ03B0013-0141
Rev.1.41
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1. Overview

The M32C/83 Group (M32C/83, M32C/83T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/83 Group (M32C/83, M32C/83T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

Table 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK) = 32 MHz, VCC = 4.2 to 5.5 V) 50 ns (f(BCLK) = 20 MHz, VCC = 3.0 to 5.5 V)	31.3 ns (f(BCLK) = 32 MHz, VCC=4.2 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1))	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuits, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 µA (VCC=5 V, stop mode) 0.4 µA (VCC=3.3 V, stop mode)	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, Vf(BCLK)=30 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 µA (VCC=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

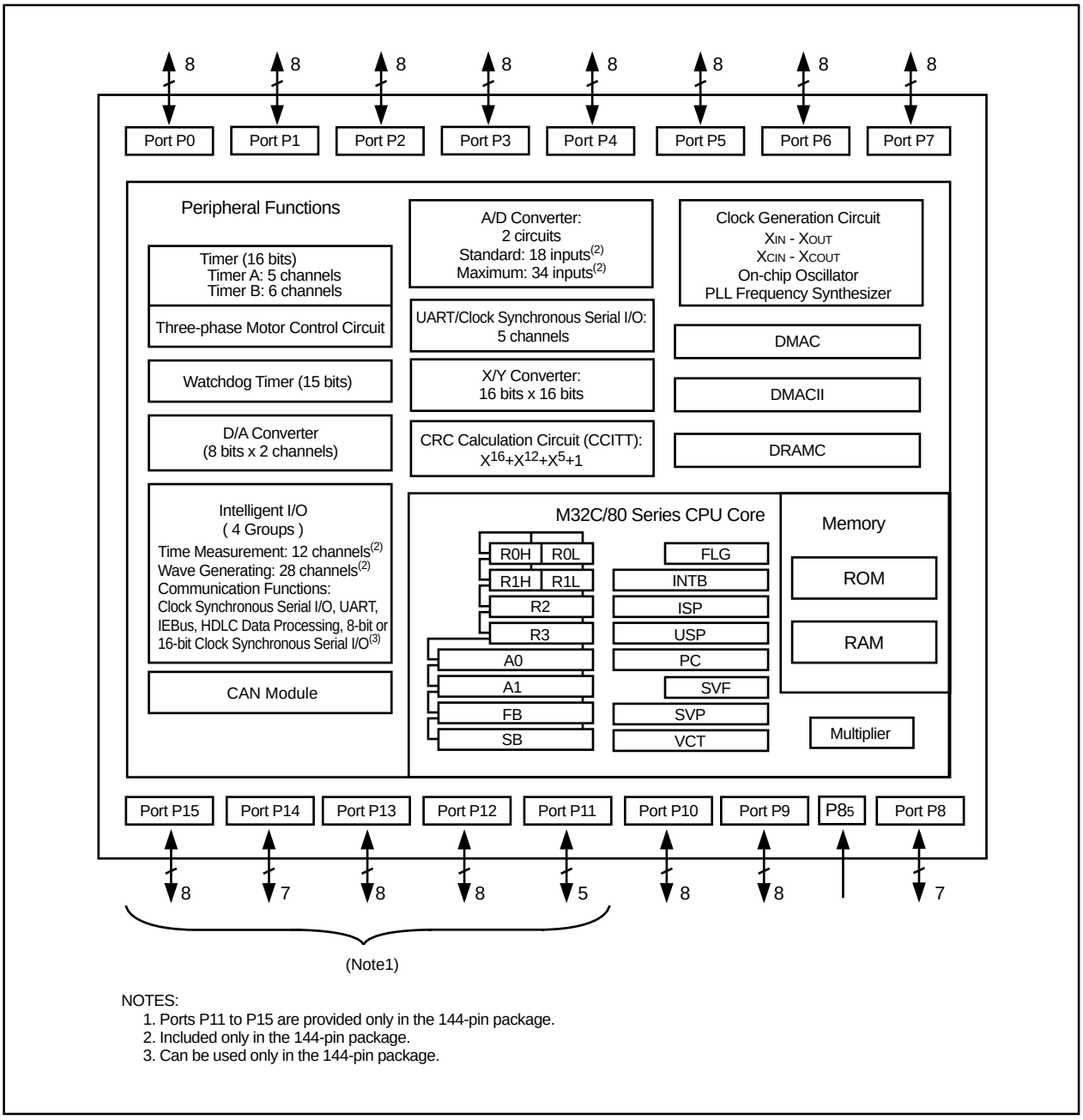
NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 Group (M32C/83, M32C/83T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided only in the 144-pin package.
2. Included only in the 144-pin package.
3. Can be used only in the 144-pin package.

Figure 1.1 M32C/83 Group (M32C/83, M32C/83T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85ºC Version)

Please contact our sales office for V version information.

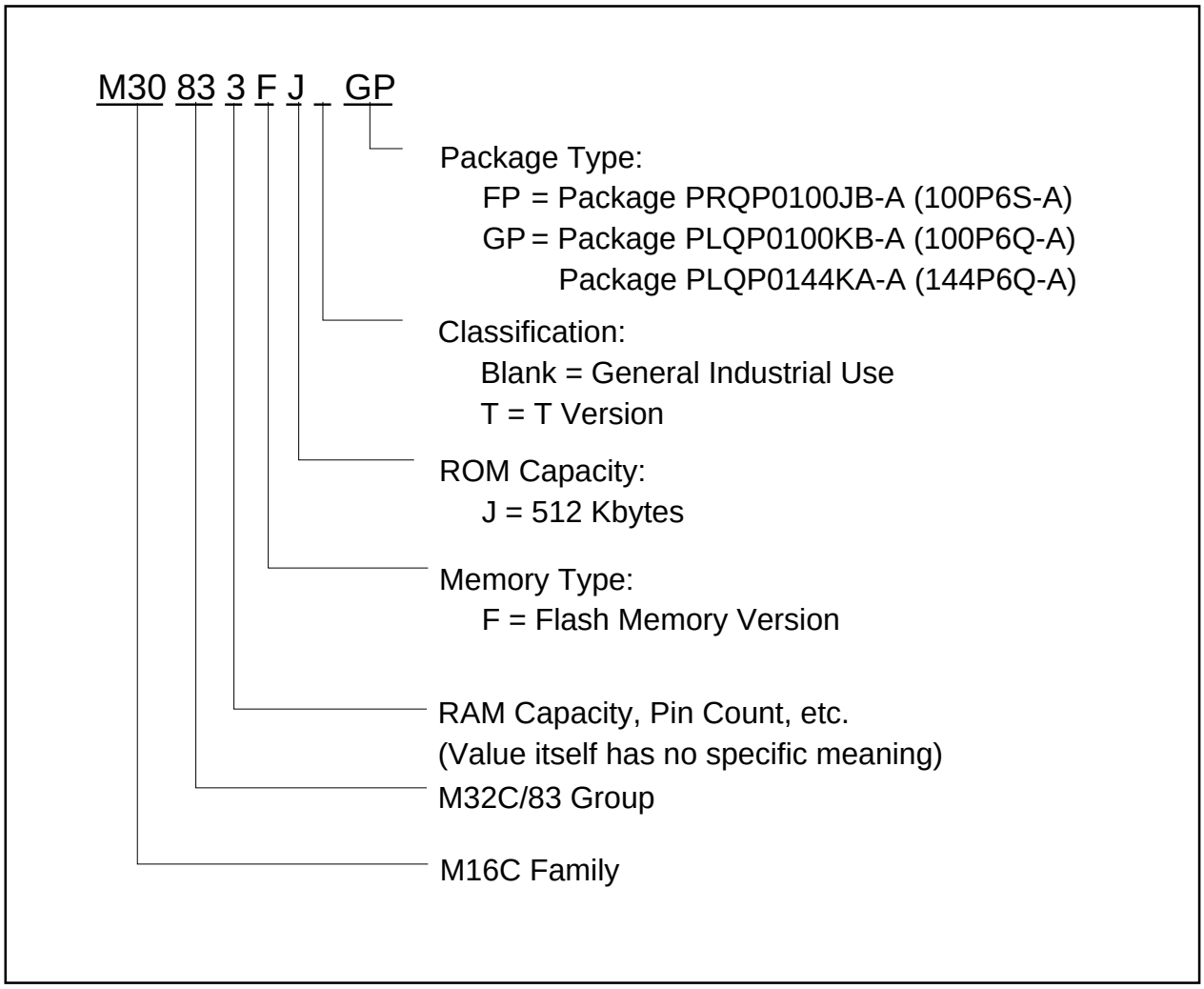


Figure 1.2 Product Numbering System

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
51	49		$P4_3$						$A_{19}(MA_{11})$
52	50		$P4_2$						$A_{18}(MA_{10})$
53	51		$P4_1$						$A_{17}(MA_9)$
54	52		$P4_0$						$A_{16}(MA_8)$
55	53		$P3_7$						$A_{15}(MA_7)(/D_{15})$
56	54		$P3_6$						$A_{14}(MA_6)(/D_{14})$
57	55		$P3_5$						$A_{13}(MA_5)(/D_{13})$
58	56		$P3_4$						$A_{12}(MA_4)(/D_{12})$
59	57		$P3_3$						$A_{11}(MA_3)(/D_{11})$
60	58		$P3_2$						$A_{10}(MA_2)(/D_{10})$
61	59		$P3_1$						$A_9(MA_1)(/D_9)$
62	60	V_{CC}							
63	61		$P3_0$						$A_8(MA_0)(/D_8)$
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	$A_7(/D_7)$
66	64		$P2_6$					$AN2_6$	$A_6(/D_6)$
67	65		$P2_5$					$AN2_5$	$A_5(/D_5)$
68	66		$P2_4$					$AN2_4$	$A_4(/D_4)$
69	67		$P2_3$					$AN2_3$	$A_3(/D_3)$
70	68		$P2_2$					$AN2_2$	$A_2(/D_2)$
71	69		$P2_1$					$AN2_1$	$A_1(/D_1)$
72	70		$P2_0$					$AN2_0$	$A_0(/D_0)$
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Function
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	
Low-Pass Filter Connect Pin for PLL Frequency Synthesizer Pin	VCONT		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
BCLK Output(1)	BCLK	O	Outputs BCLK signal
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTE:

1. Bus control pins in M32C/83T cannot be used.

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X0002
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	Intelligent I/O Interrupt Control Register 11/ CAN Interrupt 2 Control Register	IIO11IC CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616	A/D1 Conversion Interrupt Control Register	AD1IC	XXXX X0002
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
012016 012116	Group 1 Base Timer Register	G1BT	XX16 XX16
012216	Group 1 Base Timer Control Register 0	G1BCR0	0016
012316	Group 1 Base Timer Control Register 1	G1BCR1	0016
012416	Group 1 Time Measurement Prescaler Register 6	G1TPR6	0016
012516	Group 1 Time Measurement Prescaler Register 7	G1TPR7	0016
012616	Group 1 Function Enable Register	G1FE	0016
012716	Group 1 Function Select Register	G1FS	0016
012816 012916	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX2 XX00 XXXX2
012A16	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX16
012B16			
012C16	Group 1 Receive Input Register	G1RI	XX16
012D16	Group 1 SI/O Communication Mode Register	G1MR	0016
012E16	Group 1 Transmit Output Register	G1TO	XX16
012F16	Group 1 SI/O Communication Control Register	G1CR	0000 X0002
013016	Group 1 Data Compare Register 0	G1CMP0	XX16
013116	Group 1 Data Compare Register 1	G1CMP1	XX16
013216	Group 1 Data Compare Register 2	G1CMP2	XX16
013316	Group 1 Data Compare Register 3	G1CMP3	XX16
013416	Group 1 Data Mask Register 0	G1MSK0	XX16
013516	Group 1 Data Mask Register 1	G1MSK1	XX16
013616			
013716			
013816 013916	Group 1 Receive CRC Code Register	G1RCRC	XX16 XX16
013A16 013B16	Group 1 Transmit CRC Code Register	G1TCRC	0016 0016
013C16	Group 1 SI/O Extended Mode Register	G1EMR	0016
013D16	Group 1 SI/O Extended Receive Control Register	G1ERC	0016
013E16	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX2
013F16	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX2
014016 014116	Group 2 Waveform Generating Register 0	G2PO0	XX16 XX16
014216 014316	Group 2 Waveform Generating Register 1	G2PO1	XX16 XX16
014416 014516	Group 2 Waveform Generating Register 2	G2PO2	XX16 XX16
014616 014716	Group 2 Waveform Generating Register 3	G2PO3	XX16 XX16
014816 014916	Group 2 Waveform Generating Register 4	G2PO4	XX16 XX16
014A16 014B16	Group 2 Waveform Generating Register 5	G2PO5	XX16 XX16
014C16 014D16	Group 2 Waveform Generating Register 6	G2PO6	XX16 XX16
014E16 014F16	Group 2 Waveform Generating Register 7	G2PO7	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0210₁₆ 0211₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00₁₆(2) 00₁₆(2)
0212₁₆			
0213₁₆			
0214₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000₂(2)
0215₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000₂(2)
0216₁₆			
0217₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001₂(2)
0218₁₆			
0219₁₆			
021A₁₆			
021B₁₆			
021C₁₆			
021D₁₆			
021E₁₆			
021F₁₆			
0220₁₆			
0221₁₆			
0222₁₆			
0223₁₆			
0224₁₆			
0225₁₆			
0226₁₆			
0227₁₆			
0228₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000₂(2)
0229₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000₂(2)
022A₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000₂(2)
022B₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00₁₆(2)
022C₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000₂(2)
022D₁₆			
022E₁₆			
022F₁₆			
0230₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000₂(2) XXX0 0000₂(2)
0231₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000₂(2) XX00 0000₂(2)
0232₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000₂(2) XXXX 0000₂(2)
0233₁₆	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00₁₆(2) 00₁₆(2)
0234₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000₂(2) XX00 0000₂(2)
0235₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00₁₆(2)
0236₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00₁₆(2)
0237₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00₁₆(2)
0238₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000₂(2) XXX0 0000₂(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	XX00 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416	CAN0 Acceptance Filter Support Register	C0AFS	0016(2)
024516			0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			
026016			
026116 to 02BF16			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03A016				(Note 2)
03A116				
03A216				
03A316				
03A416				
03A516				
03A616				
03A716				
03A816				
03A916				
03AA16				
03AB16				
03AC16				
03AD16				
03AE16				
03AF16	Function Select Register C	PSC	0X00 00002	
03B016	Function Select Register A0	PS0	0016	
03B116	Function Select Register A1	PS1	0016	
03B216	Function Select Register B0	PSL0	0016	
03B316	Function Select Register B1	PSL1	0016	
03B416	Function Select Register A2	PS2	00X0 00002	
03B516	Function Select Register A3	PS3	0016	
03B616	Function Select Register B2	PSL2	00X0 00002	
03B716	Function Select Register B3	PSL3	0016	
03B816				
03B916				(Note 2)
03BA16				
03BB16				
03BC16				(Note 2)
03BD16				
03BE16				
03BF16				
03C016	Port P6 Register	P6	XX16	
03C116	Port P7 Register	P7	XX16	
03C216	Port P6 Direction Register	PD6	0016	
03C316	Port P7 Direction Register	PD7	0016	
03C416	Port P8 Register	P8	XX16	
03C516	Port P9 Register	P9	XX16	
03C616	Port P8 Direction Register	PD8	00X0 00002	
03C716	Port P9 Direction Register	PD9	0016	
03C816	Port P10 Register	P10	XX16	
03C916				(Note 2)
03CA16	Port P10 Direction Register	PD10	0016	
03CB16				(Note 1)
03CC16				(Note 2)
03CD16				
03CE16				(Note 1)
03CF16				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03CB16, 03CE16 and 03CF16 to "FF16" in the 100-pin package.
2. Address spaces 03A016, 03A116, 03B916, 03BC16, 03BD16, 03C916, 03CC16 and 03CD16 are not provided in the 100-pin package.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/83)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature			-20 to 85	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.

Table 5.2 Recommended Operating Conditions (V_{CC} = 3.0V to 5.5V at Topr = – 20 to 85°C)

Symbol	Parameter			Standard			Unit
				Min	Typ	Max	
V_{CC}	Supply Voltage (Through VDC)			3.0	5.0	5.5	V
	Supply Voltage (Not through VDC)			3.0	3.3	3.6	V
AV_{CC}	Analog Supply Voltage				V_{CC}		V
V_{SS}	Supply Voltage				0		V
AV_{SS}	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$[3], $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4], X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$		0.8V_{CC}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0.8V_{CC}		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0.5V_{CC}		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$[3], $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4], X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0		0.16V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current[2]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current[1]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current[2]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current[1]	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$[4]				5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	Through VDC	V_{CC}=4.2 to 5.5V	0		32	MHz
			V_{CC}=3.0 to 4.3V	0		20	MHz
		Not through VDC	V_{CC}=3.0 to 3.6	0		20	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency				32.768	50	kHz

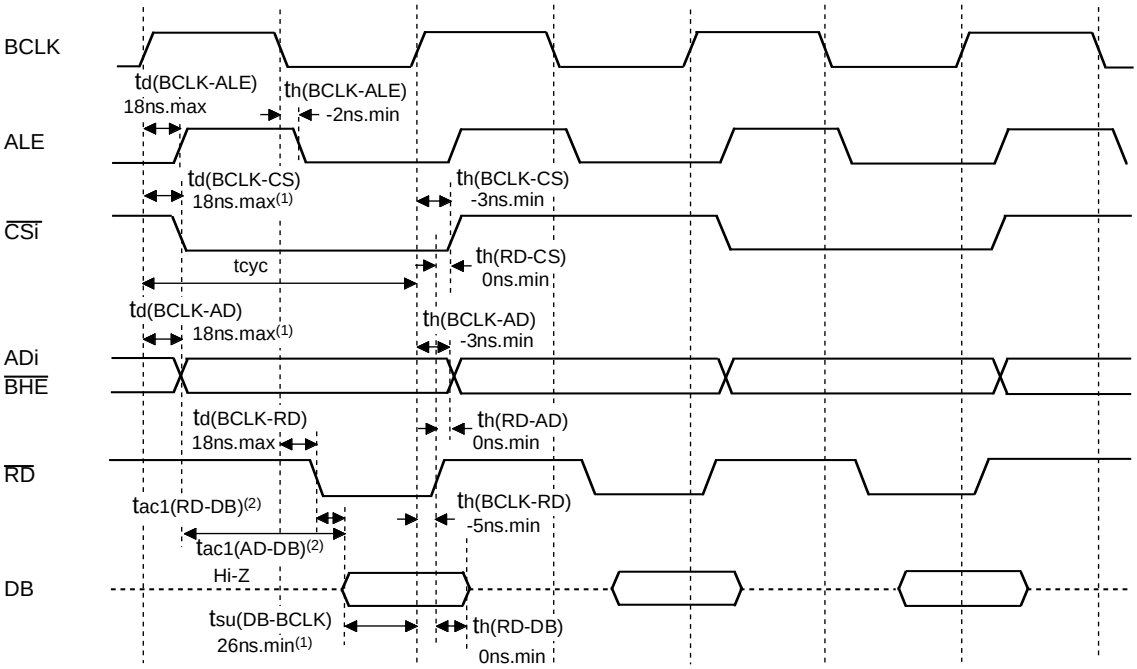
NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply to $P8_7$ used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

Vcc=5V

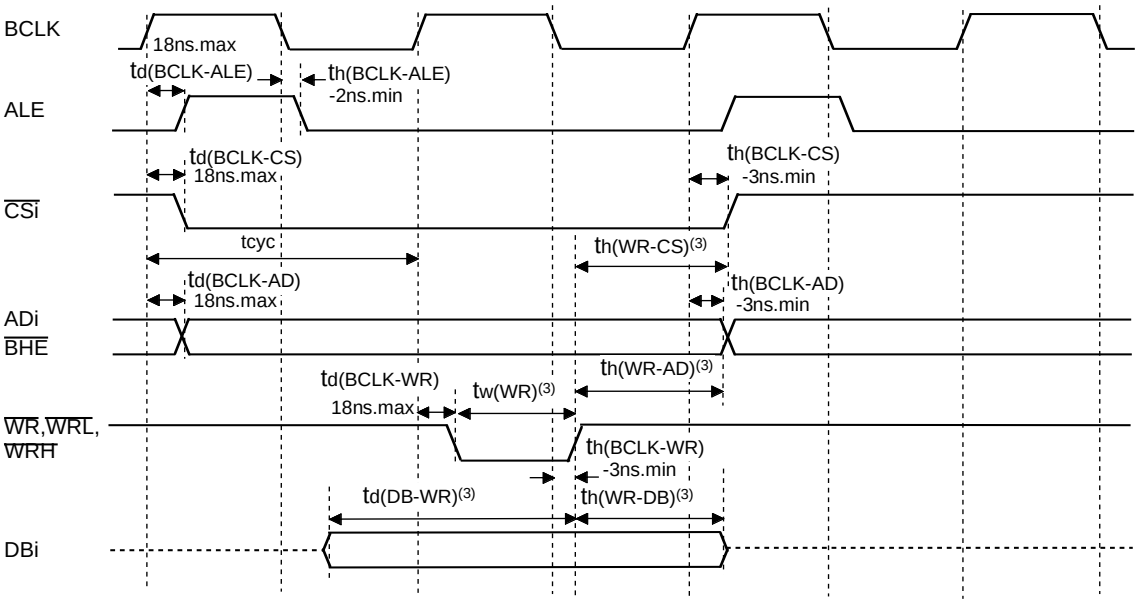
Memory Expansion Mode and Microprocessor Mode (with no wait state)

Read Timing



NOTES:
1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac1(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac1(AD-DB)}$=(tcyc-35)ns.max

Write Timing (written in 2 cycles with no wait state)



NOTES:
3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement Conditions:
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

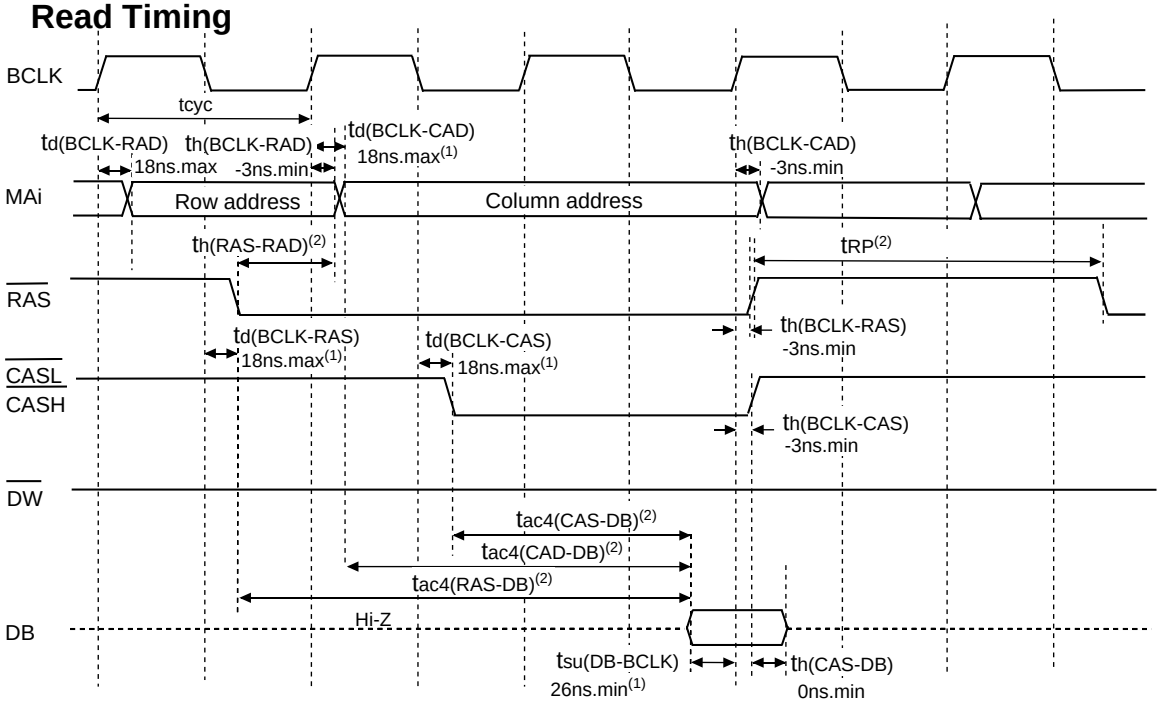
Figure 5.2 Vcc=5V Timing Diagram (1)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(When accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for the following combinations.
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. Varies with operation frequency:
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.5 Vcc=5V Timing Diagram (4)

VCC=3.3V

Table 5.25 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		V_{REF}=V_{CC}			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	V_{CC}=V_{REF}=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		V_{REF}=V_{CC}	8		40	kΩ
t_{CONV}	8-bit Conversion Time			4.9			µs
V_{REF}	Reference Voltage			3.0		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.

Table 5.26 D/A Conversion Characteristics (V_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00_{16}". The resistor ladder in the A/D converter is exclued.
I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.27 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.35 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.36 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.37 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.38 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input High ("H") Pulse Width (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 5.39 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.40 External Interrupt $\overline{INTi}$ input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	INTi Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	INTi Input Low ("L") Pulse Width	250		ns

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