Renesas Electronics America Inc - M30835FJGP#U3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30835fjgp-u3

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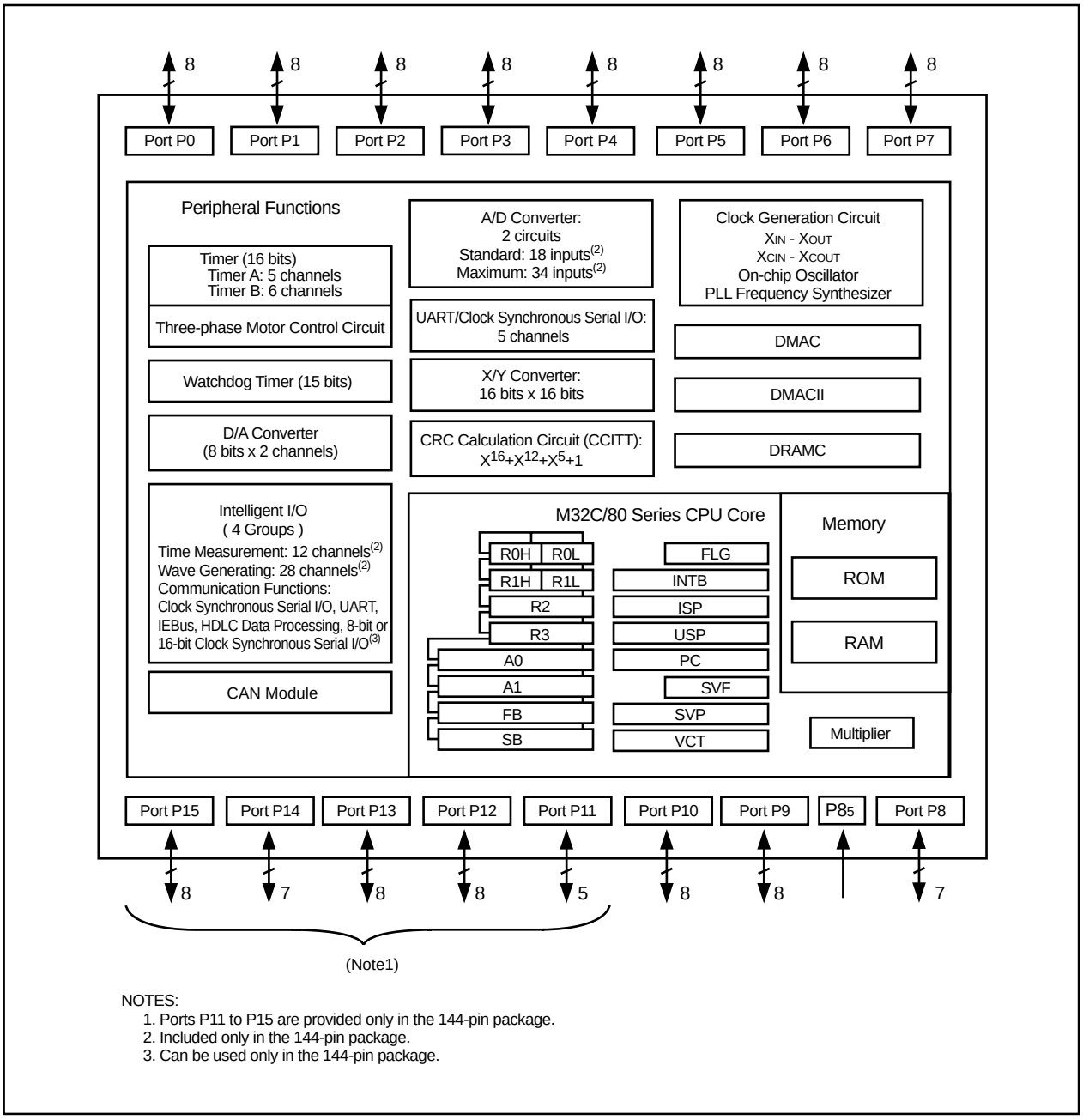
1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 Group (M32C/83, M32C/83T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided only in the 144-pin package.
2. Included only in the 144-pin package.
3. Can be used only in the 144-pin package.

Figure 1.1 M32C/83 Group (M32C/83, M32C/83T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85ºC Version)

Please contact our sales office for V version information.

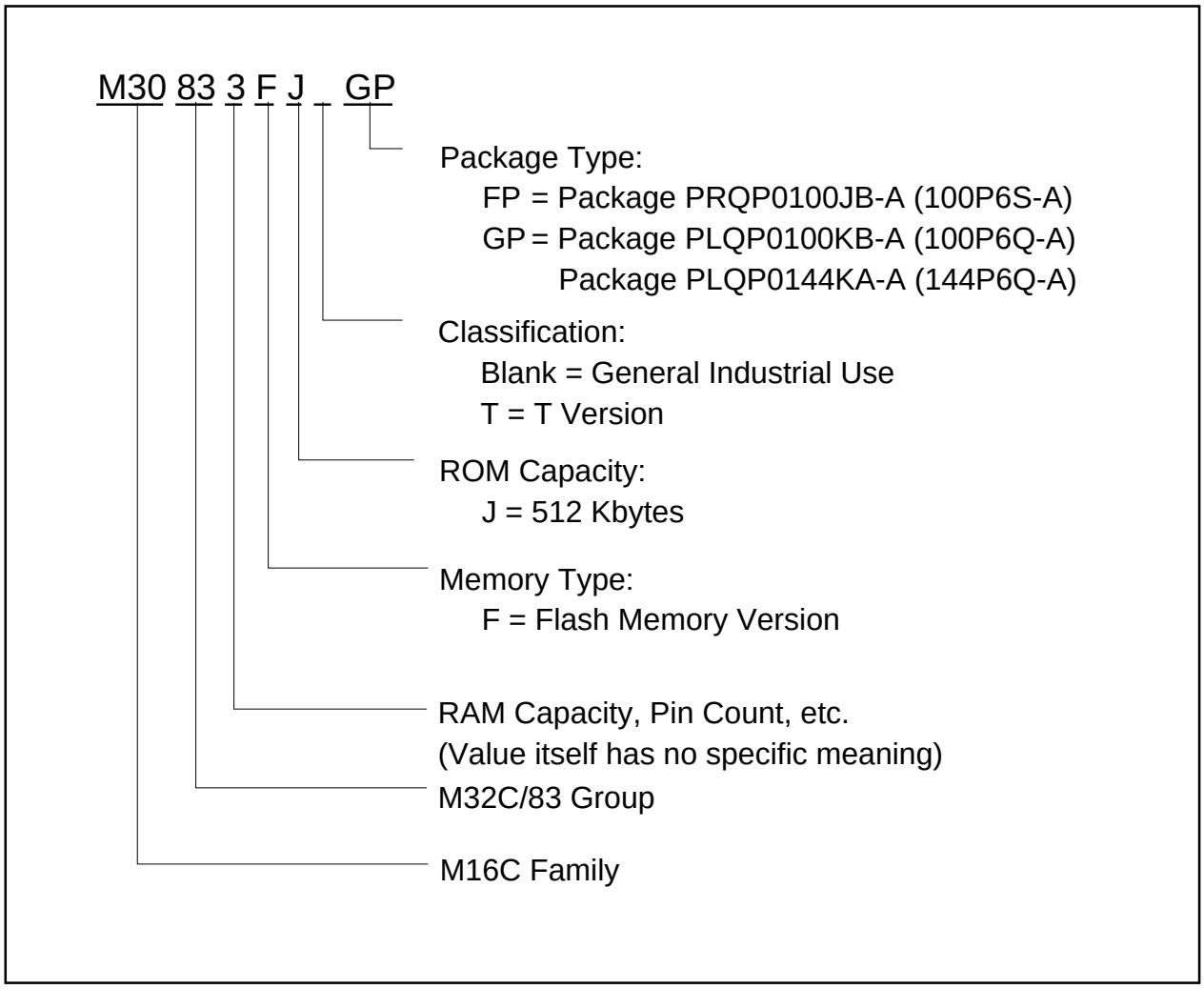


Figure 1.2 Product Numbering System

Address	Register	Symbol	Value after RESET
00F016	Group 0 Data Compare Register 0	G0CMP0	XX16
00F116	Group 0 Data Compare Register 1	G0CMP1	XX16
00F216	Group 0 Data Compare Register 2	G0CMP2	XX16
00F316	Group 0 Data Compare Register 3	G0CMP3	XX16
00F416	Group 0 Data Mask Register 0	G0MSK0	XX16
00F516	Group 0 Data Mask Register 1	G0MSK1	XX16
00F616			
00F716			
00F816	Group 0 Receive CRC Code Register	G0RCRC	XX16
00F916			XX16
00FA16	Group 0 Transmit CRC Code Register	G0TCRC	0016
00FB16			0016
00FC16	Group 0 SI/O Extended Mode Register	G0EMR	0016
00FD16	Group 0 SI/O Extended Receive Control Register	G0ERC	0016
00FE16	Group 0 SI/O Special Communication Interrupt Detect Register	G0IRF	0000 00XX2
00FF16	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXX2
010016	Group 1 Time Measurement/Waveform Generating Register 0	G1TM0/G1PO0	XX16
010116			XX16
010216	Group 1 Time Measurement/Waveform Generating Register 1	G1TM1/G1PO1	XX16
010316			XX16
010416	Group 1 Time Measurement/Waveform Generating Register 2	G1TM2/G1PO2	XX16
010516			XX16
010616	Group 1 Time Measurement/Waveform Generating Register 3	G1TM3/G1PO3	XX16
010716			XX16
010816	Group 1 Time Measurement/Waveform Generating Register 4	G1TM4/G1PO4	XX16
010916			XX16
010A16	Group 1 Time Measurement/Waveform Generating Register 5	G1TM5/G1PO5	XX16
010B16			XX16
010C16	Group 1 Time Measurement/Waveform Generating Register 6	G1TM6/G1PO6	XX16
010D16			XX16
010E16	Group 1 Time Measurement/Waveform Generating Register 7	G1TM7/G1PO7	XX16
010F16			XX16
011016	Group 1 Waveform Generating Control Register 0	G1POCR0	0X00 X0002
011116	Group 1 Waveform Generating Control Register 1	G1POCR1	0X00 X0002
011216	Group 1 Waveform Generating Control Register 2	G1POCR2	0X00 X0002
011316	Group 1 Waveform Generating Control Register 3	G1POCR3	0X00 X0002
011416	Group 1 Waveform Generating Control Register 4	G1POCR4	0X00 X0002
011516	Group 1 Waveform Generating Control Register 5	G1POCR5	0X00 X0002
011616	Group 1 Waveform Generating Control Register 6	G1POCR6	0X00 X0002
011716	Group 1 Waveform Generating Control Register 7	G1POCR7	0X00 X0002
011816	Group 1 Time Measurement Control Register 0	G1TMCR0	0016
011916	Group 1 Time Measurement Control Register 1	G1TMCR1	0016
011A16	Group 1 Time Measurement Control Register 2	G1TMCR2	0016
011B16	Group 1 Time Measurement Control Register 3	G1TMCR3	0016
011C16	Group 1 Time Measurement Control Register 4	G1TMCR4	0016
011D16	Group 1 Time Measurement Control Register 5	G1TMCR5	0016
011E16	Group 1 Time Measurement Control Register 6	G1TMCR6	0016
011F16	Group 1 Time Measurement Control Register 7	G1TMCR7	0016

X: Indeterminate

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Address	Register	Symbol	Value after RESET
018016 018116	Group 3 Waveform Generating Register 0	G3PO0	XX16 XX16
018216 018316	Group 3 Waveform Generating Register 1	G3PO1	XX16 XX16
018416 018516	Group 3 Waveform Generating Register 2	G3PO2	XX16 XX16
018616 018716	Group 3 Waveform Generating Register 3	G3PO3	XX16 XX16
018816 018916	Group 3 Waveform Generating Register 4	G3PO4	XX16 XX16
018A16 018B16	Group 3 Waveform Generating Register 5	G3PO5	XX16 XX16
018C16 018D16	Group 3 Waveform Generating Register 6	G3PO6	XX16 XX16
018E16 018F16	Group 3 Waveform Generating Register 7	G3PO7	XX16 XX16
019016	Group 3 Waveform Generating Control Register 0	G3POCR0	0016
019116	Group 3 Waveform Generating Control Register 1	G3POCR1	0016
019216	Group 3 Waveform Generating Control Register 2	G3POCR2	0016
019316	Group 3 Waveform Generating Control Register 3	G3POCR3	0016
019416	Group 3 Waveform Generating Control Register 4	G3POCR4	0016
019516	Group 3 Waveform Generating Control Register 5	G3POCR5	0016
019616	Group 3 Waveform Generating Control Register 6	G3POCR6	0016
019716	Group 3 Waveform Generating Control Register 7	G3POCR7	0016
019816 019916	Group 3 Waveform Generating Mask Register 4	G3MK4	XX16 XX16
019A16 019B16	Group 3 Waveform Generating Mask Register 5	G3MK5	XX16 XX16
019C16 019D16	Group 3 Waveform Generating Mask Register 6	G3MK6	XX16 XX16
019E16 019F16	Group 3 Waveform Generating Mask Register 7	G3MK7	XX16 XX16
01A016 01A116	Group 3 Base Timer Register	G3BT	XX16 XX16
01A216	Group 3 Base Timer Control Register 0	G3BCR0	0016
01A316	Group 3 Base Timer Control Register 1	G3BCR1	0016
01A416			
01A516			
01A616	Group 3 Function Enable Register	G3FE	0016
01A716	Group 3 RTP Output Buffer Register	G3RTP	0016
01A816			
01A916			
01AA16			
01AB16			
01AC16			
01AD16	Group 3 SI/O Communication Flag Register	G3FLG	XXXX XXX02
01AE16			
01AF16			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Baud Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆ 0311₁₆	Timer B3 Register	TB3	XX₁₆ XX₁₆
0312₁₆ 0313₁₆	Timer B4 Register	TB4	XX₁₆ XX₁₆
0314₁₆ 0315₁₆	Timer B5 Register	TB5	XX₁₆ XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XX16 XX16
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216			
039316			
039416	A/D0 Control Register 2	AD0CON2	X000 00002
039516			
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

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VCC=5V

Table 5.4 A/D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, Vss = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	VREF=VCC				10	Bits
INL	Integral Nonlinearity Error	VREF=VCC=5V	AN0 to AN7 ANEX0, ANEX1			±3	LSB LSB
			External op-amp connection mode			±7	LSB LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
RLADDER	Resistor Ladder	VREF=VCC		8		40	kΩ
tCONV	10-bit Conversion Time			2.1			µs
tCONV	8-bit Conversion Time			1.8			µs
tSAMP	Sample Time			0.2			µs
VREF	Reference Voltage			2		VCC	V
VIA	Analog Input Voltage			0		VREF	V

NOTES:
1. Divide f(XIN), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 5.5 D/A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tSU	Setup Time				3	µs
RO	Output Resistance		4	10	20	kΩ
IVREF	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00$_{16}$". The resistor ladder in the A/D converter is exclued. IVREF flows even if the VCUT bit in the ADiCON1 register is set to "0" (no VREF connection).

Table 5.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. VCC= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.9 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

V_{CC}=5V

Timing Requirements

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.14 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.15 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.16 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.17 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 5.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.19 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Pulse Width	250		ns

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{W(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{W(WR)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-RAD)}$	Row Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-RAD)}$	Row Address Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-CAD)}$	Column Address Output Delay Time			18	ns
$t_{h(BCLK-CAD)}$	Column Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RAS-RAD)}$	Row Address Output Hold Time after RAS Output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS Output Hold Time (BCLK standard)		-3		ns
t_{RP}	RAS High ("H") Hold Time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-DW)}$	DW Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW Output Hold Time (BCLK standard)		-5		ns
$t_{su(DB-CAS)}$	CAS Output Setup Time after DB Output		(Note 1)		ns
$t_{h(BCLK-DB)}$	DB Signal Output Hold Time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

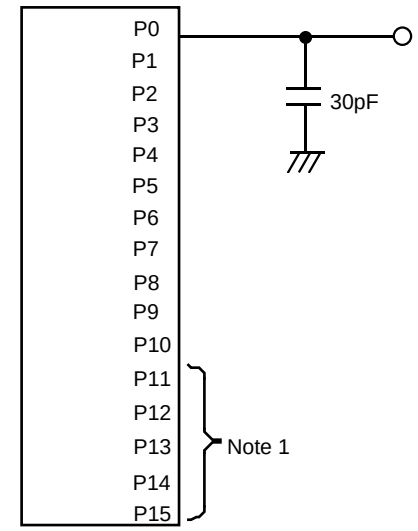
1. Values can be obtained from the following equation, according to BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$



NOTES:

1. P11 to P15 are provided in the 144-pin package only.

Figure 5.1 P0 to P15 Measurement Circuit

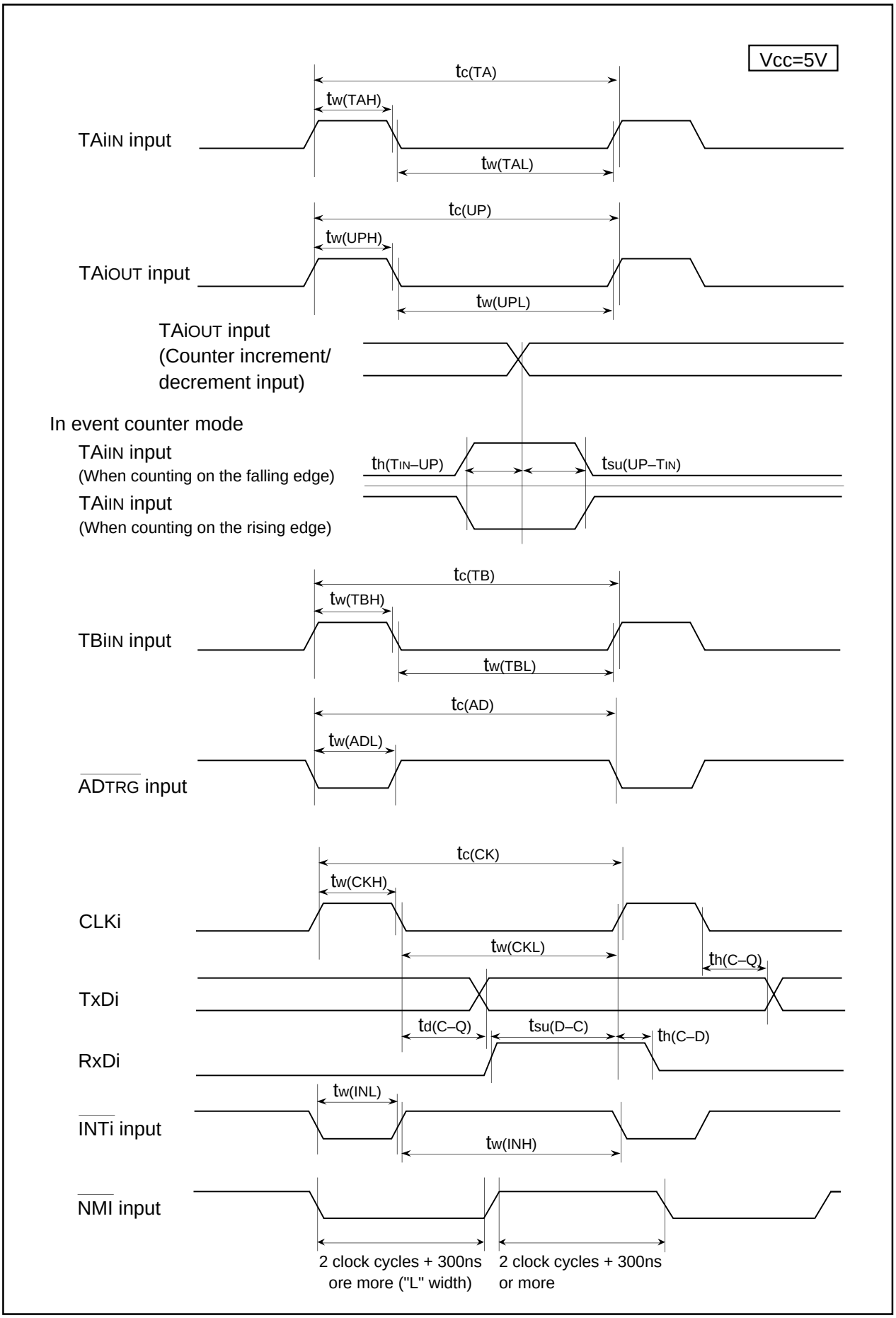
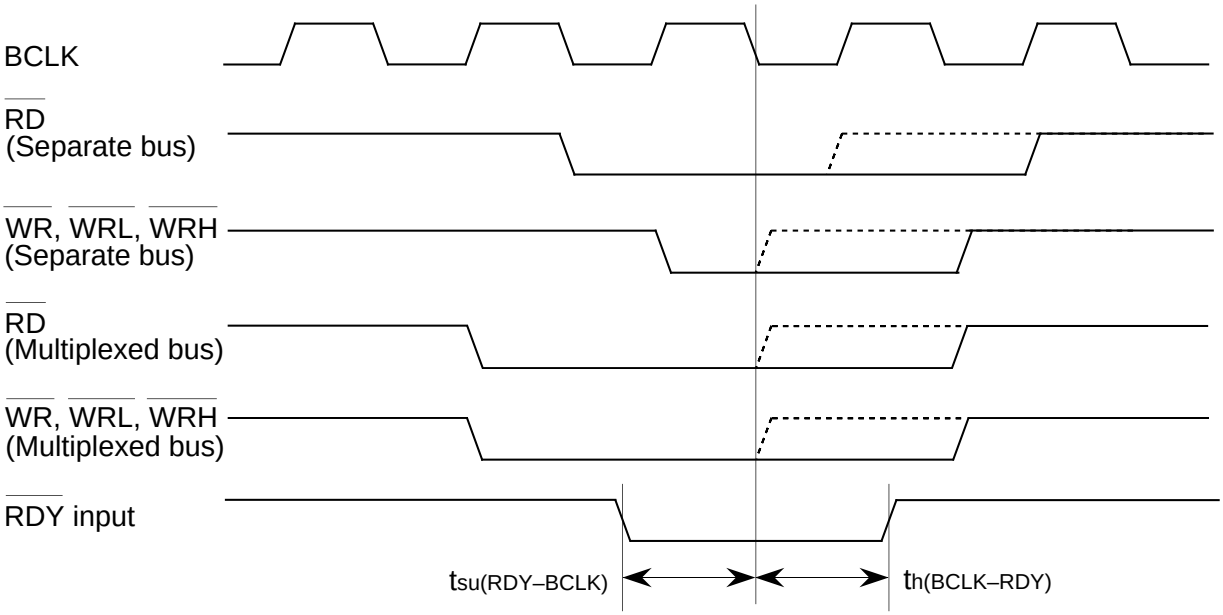


Figure 5.8 Vcc=5V Timing Diagram (7)

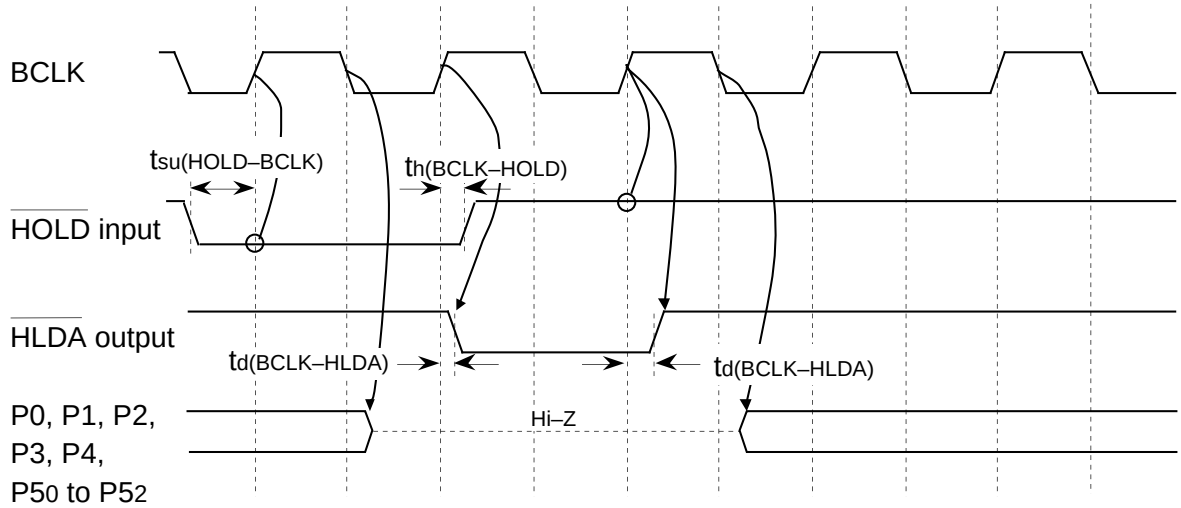
Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state or with no wait state)



Measurement Conditions:

- VCC=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 5.9 Vcc=5V Timing Diagram (8)

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=5V

Table 5.47 Electrical Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0V at Topr = –40 to 85°C(T version), f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	V_{CC}-2.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	V_{CC}-0.3			V
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage			2.5			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS} — f(X_{IN})=32 MHz, square wave, no division			40	54	mA
			f(X_{CIN})=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.48 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, Vss = AV_{SS} = 0V at Topr = –40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	V_{REF}=V_{CC}				10	Bits
INL	Integral Nonlinearity Error	V_{REF}=V_{CC}=5V	AN_0 to AN_7 $ANEX_0$, $ANEX_1$			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	V_{REF}=V_{CC}		8		40	kΩ
t_{CONV}	10-bit Conversion Time			2.1			µs
t_{CONV}	8-bit Conversion Time			1.8			µs
t_{SAMP}	Sample Time			0.2			µs
V_{REF}	Reference Voltage			2		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 5.49 D/A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V at Topr = –40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00_{16}". The resistor ladder in the A/D converter is exclued. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.50 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V at Topr= 0 to 60° C, unless otherwise specified

REVISION HISTORY	M32C/83 GROUP (M32C/83, M32C/83T) Datasheet

Rev.	Date	Description	
		Page	Summary
		72	• **Table 5.44 Memory Expansion Mode and Microprocessor Mode** Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		79	• **Figure 5.8 Vcc=3.3 V Timing Diagram (7)** Timing for $\overline{\text{NMI}}$ input added
		81-89	• **5.2 Electrical Characteristics (M32C/83T)** Newly added