Renesas Electronics America Inc - M30835FJGP#U5 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	31K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30835fjgp-u5

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1. Overview

The M32C/83 Group (M32C/83, M32C/83T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/83 Group (M32C/83, M32C/83T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/83 Group (M32C/83, M32C/83T).

Table 1.1 M32C/83 Group (M32C/83, M32C/83T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3) 50 ns (f(BCLK)=20 MHz, VCC=3.0 to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1), 8-bit or 16-bit Clock synchronous serial I/O)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	DRAM	CAS before RAS refresh, Self-reflesh, EDO, EP	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources, Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 µA (VCC=5 V, stop mode) 0.4 µA (VCC=3.3 V, stop mode)	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, Vf(BCLK)=30 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 µA (VCC=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
49		P13$_6$				OUTC2$_1$/ISCLK2		
50		P13$_5$				OUTC2$_2$/ISRxD2/IE$_{IN}$		
51		P13$_4$				OUTC2$_0$/ISTxD2/IE$_{OUT}$		
52		P5$_7$						$\overline{RDY}$
53		P5$_6$						ALE/$\overline{RAS}$
54		P5$_5$						$\overline{HOLD}$
55		P5$_4$						$\overline{HLDA}$/ALE
56		P13$_3$				OUTC2$_3$		
57	V$_{SS}$							
58		P13$_2$				OUTC2$_6$		
59	V$_{CC}$							
60		P13$_1$				OUTC2$_5$		
61		P13$_0$				OUTC2$_4$		
62		P5$_3$						CLK$_{OUT}$/BCLK/ALE
63		P5$_2$						$\overline{RD}$/$\overline{DW}$
64		P5$_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
65		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
66		P12$_7$				OUTC3$_7$		
67		P12$_6$				OUTC3$_6$		
68		P12$_5$				OUTC3$_5$		
69		P4$_7$						$\overline{CS0}$/A$_{23}$
70		P4$_6$						$\overline{CS1}$/A$_{22}$
71		P4$_5$						$\overline{CS2}$/A$_{21}$
72		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)
73		P4$_3$						A$_{19}$(MA$_{11}$)
74	V$_{CC}$							
75		P4$_2$						A$_{18}$(MA$_{10}$)
76	V$_{SS}$							
77		P4$_1$						A$_{17}$(MA$_9$)
78		P4$_0$						A$_{16}$(MA$_8$)
79		P3$_7$						A$_{15}$(MA$_7$)(/D$_{15}$)
80		P3$_6$						A$_{14}$(MA$_6$)(/D$_{14}$)
81		P3$_5$						A$_{13}$(MA$_5$)(/D$_{13}$)
82		P3$_4$						A$_{12}$(MA$_4$)(/D$_{12}$)
83		P3$_3$						A$_{11}$(MA$_3$)(/D$_{11}$)
84		P3$_2$						A$_{10}$(MA$_2$)(/D$_{10}$)
85		P3$_1$						A$_9$(MA$_1$)(/D$_9$)
86		P12$_4$				OUTC3$_4$		
87		P12$_3$				OUTC3$_3$		
88		P12$_2$				OUTC3$_2$/ISRxD3		
89		P12$_1$				OUTC3$_1$/ISCLK3		
90		P12$_0$				OUTC3$_0$/ISTxD3		
91	V$_{CC}$							
92		P3$_0$						A$_8$(MA$_0$)(/D$_8$)
93	V$_{SS}$							
94		P2$_7$					AN2$_7$	A$_7$(/D$_7$)
95		P2$_6$					AN2$_6$	A$_6$(/D$_6$)
96		P2$_5$					AN2$_5$	A$_5$(/D$_5$)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

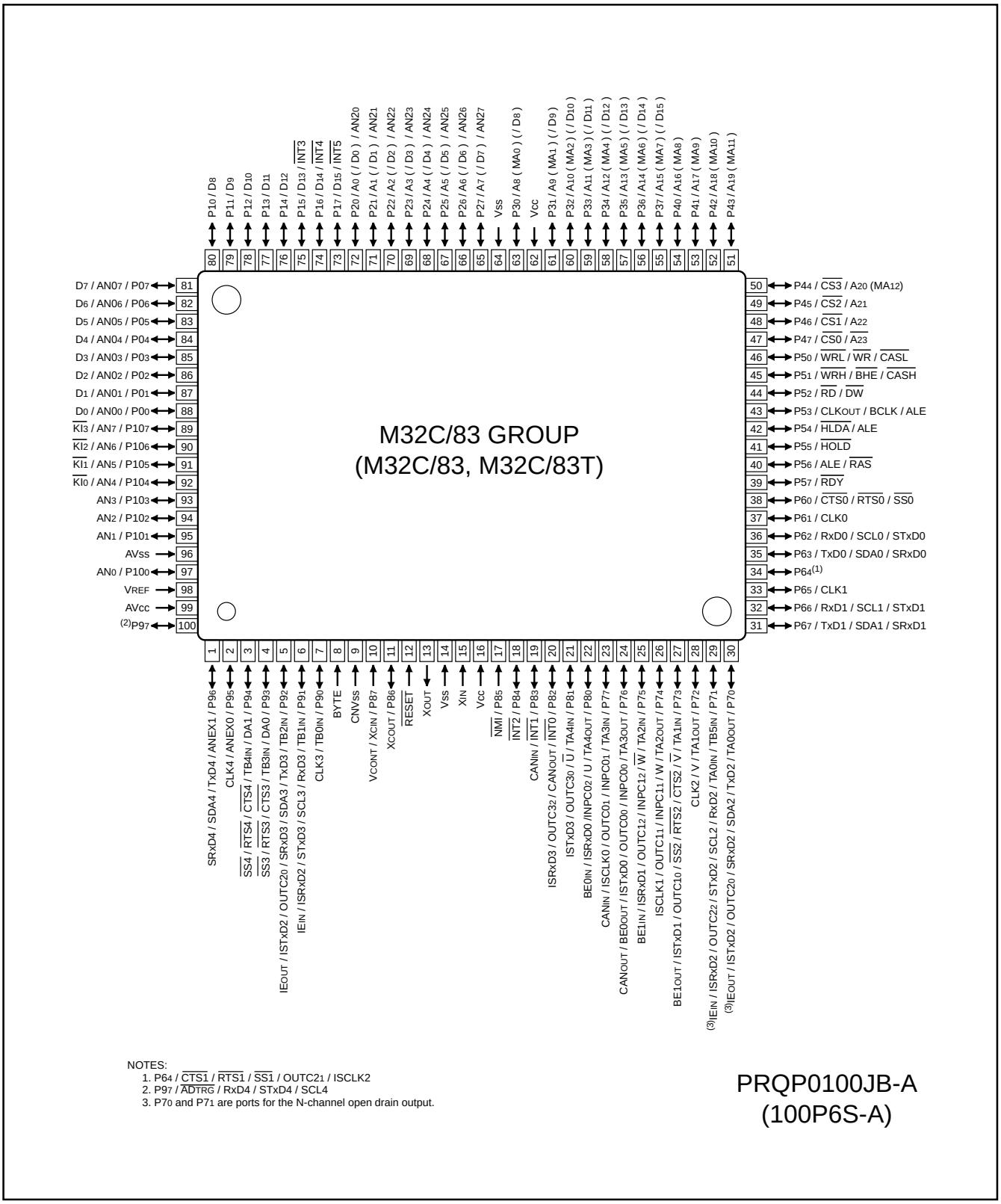


Figure 1.4 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
51	49		$P4_3$						$A_{19}(MA_{11})$
52	50		$P4_2$						$A_{18}(MA_{10})$
53	51		$P4_1$						$A_{17}(MA_9)$
54	52		$P4_0$						$A_{16}(MA_8)$
55	53		$P3_7$						$A_{15}(MA_7)(/D_{15})$
56	54		$P3_6$						$A_{14}(MA_6)(/D_{14})$
57	55		$P3_5$						$A_{13}(MA_5)(/D_{13})$
58	56		$P3_4$						$A_{12}(MA_4)(/D_{12})$
59	57		$P3_3$						$A_{11}(MA_3)(/D_{11})$
60	58		$P3_2$						$A_{10}(MA_2)(/D_{10})$
61	59		$P3_1$						$A_9(MA_1)(/D_9)$
62	60	V_{CC}							
63	61		$P3_0$						$A_8(MA_0)(/D_8)$
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	$A_7(/D_7)$
66	64		$P2_6$					$AN2_6$	$A_6(/D_6)$
67	65		$P2_5$					$AN2_5$	$A_5(/D_5)$
68	66		$P2_4$					$AN2_4$	$A_4(/D_4)$
69	67		$P2_3$					$AN2_3$	$A_3(/D_3)$
70	68		$P2_2$					$AN2_2$	$A_2(/D_2)$
71	69		$P2_1$					$AN2_1$	$A_1(/D_1)$
72	70		$P2_0$					$AN2_0$	$A_0(/D_0)$
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/83 group (M32C/83, M32C/83T).

M32C/83 group (M32C/83, M32C/83T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses FF0000$_{16}$ to FFFFFF$_{16}$.

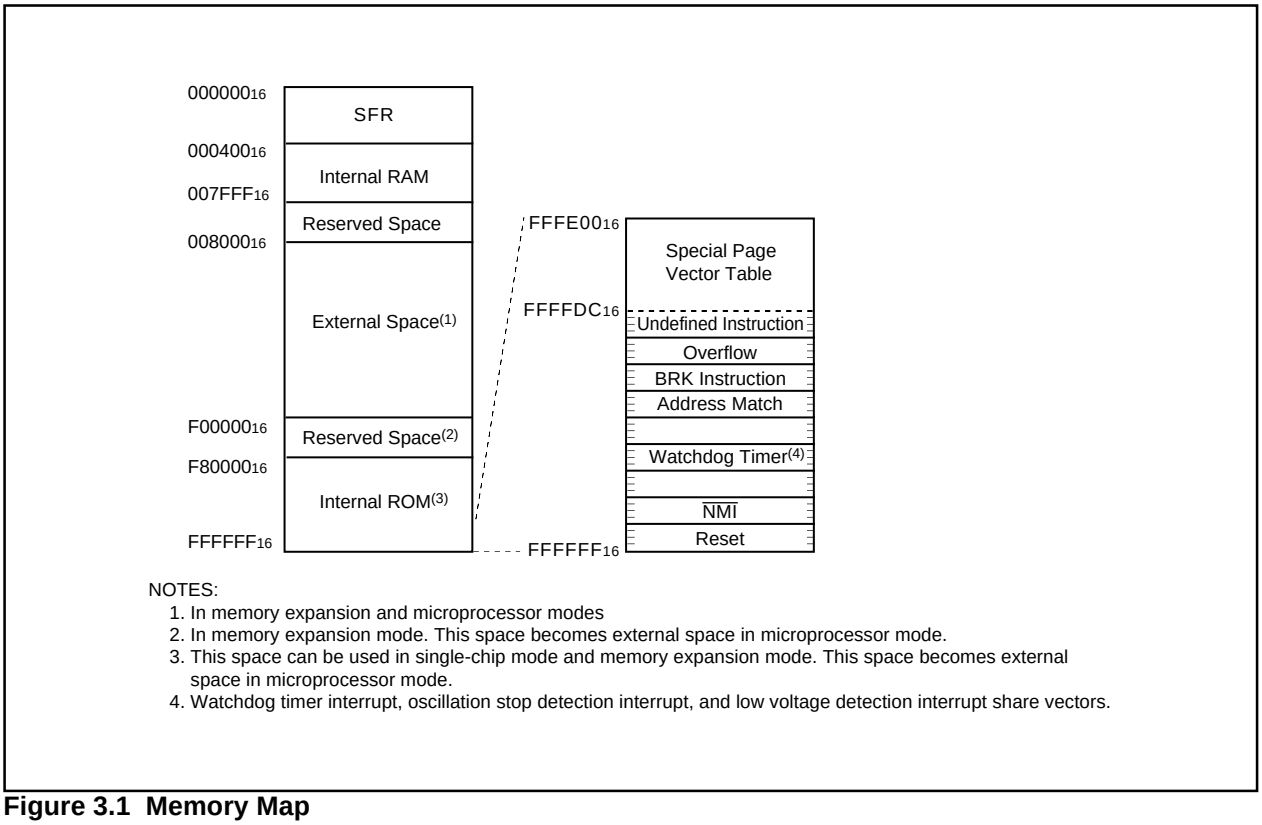
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.



NOTES:
1. In memory expansion and microprocessor modes
2. In memory expansion mode. This space becomes external space in microprocessor mode.
3. This space can be used in single-chip mode and memory expansion mode. This space becomes external space in microprocessor mode.
4. Watchdog timer interrupt, oscillation stop detection interrupt, and low voltage detection interrupt share vectors.

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor Mode Register 0(1)	PM0	1000 0000₂ (CNVss pin ="L") 0000 0011₂ (CNVss pin ="H")
0005₁₆	Processor Mode Register 1	PM1	0X00 0000₂
0006₁₆	System Clock Control Register 0	CM0	0000 X000₂
0007₁₆	System Clock Control Register 1	CM1	0010 0000₂
0008₁₆	Wait Control Register(2)	WCR	1111 1111₂
0009₁₆	Address Match Interrupt Enable Register	AIER	XXXX 0000₂
000A₁₆	Protect Register	PRCR	XXXX 0000₂
000B₁₆	External Data Bus Width Control Register(2)	DS	XXXX 1000₂ (BYTE pin ="L") XXXX 0000₂ (BYTE pin ="H")
000C₁₆	Main Clock Division Register	MCD	XXX0 1000₂
000D₁₆	Oscillation Stop Detection Register	CM2	00₁₆
000E₁₆	Watchdog Timer Start Register	WDTS	XX₁₆
000F₁₆	Watchdog Timer Control Register	WDC	000X XXXX₂
0010₁₆ 0011₁₆ 0012₁₆	Address Match Interrupt Register 0	RMAD0	00 00 00₁₆
0013₁₆			
0014₁₆ 0015₁₆ 0016₁₆	Address Match Interrupt Register 1	RMAD1	00 00 00₁₆
0017₁₆	VDC Control Register for PLL	PLV	XXXX XX01₂
0018₁₆ 0019₁₆ 001A₁₆	Address Match Interrupt Register 2	RMAD2	00 00 00₁₆
001B₁₆	VDC Control Register 0	VDC0	00₁₆
001C₁₆ 001D₁₆ 001E₁₆	Address Match Interrupt Register 3	RMAD3	00 00 00₁₆
001F₁₆			
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/83T cannot be used.

V_{CC}=5V

Table 5.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr= –20 to 85°C, f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	Vcc - 2.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	Vcc - 0.3			
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	Through VDC		2.5			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=32 MHz, square wave, no division		40	54	mA
			f(X_{CIN})=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

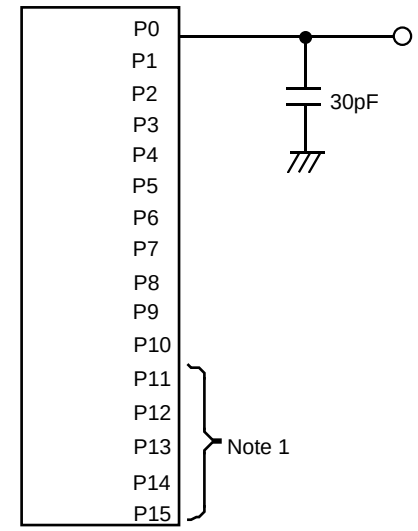
$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD-ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$



NOTES:

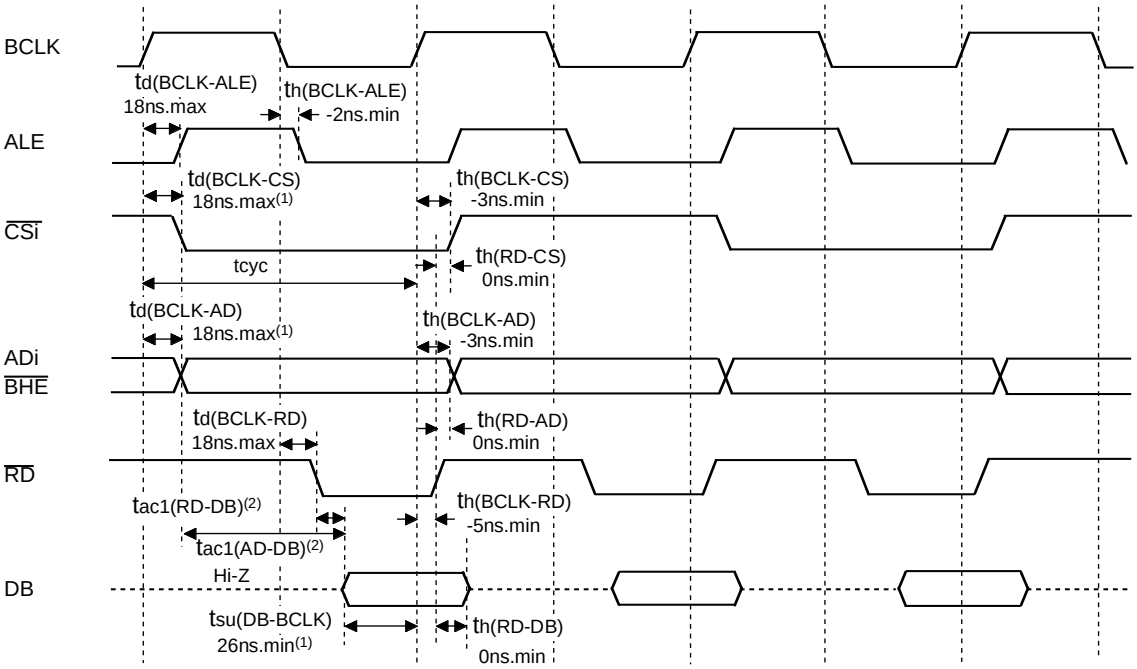
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.1 P0 to P15 Measurement Circuit

Vcc=5V

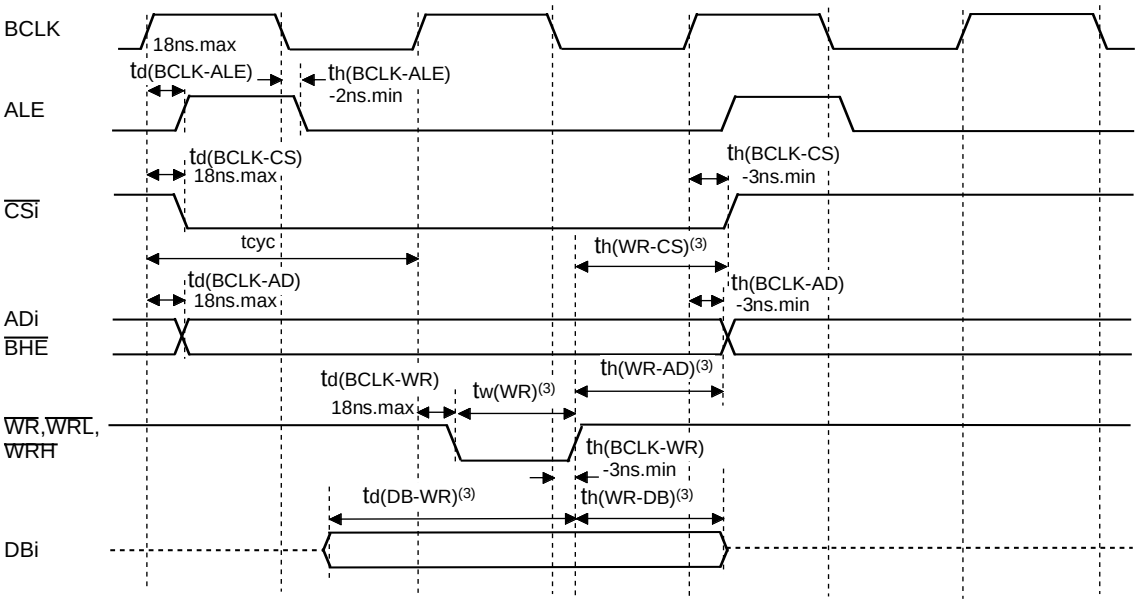
Memory Expansion Mode and Microprocessor Mode (with no wait state)

Read Timing



NOTES:
1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac1(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac1(AD-DB)}$=(tcyc-35)ns.max

Write Timing (written in 2 cycles with no wait state)



NOTES:
3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement Conditions:
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

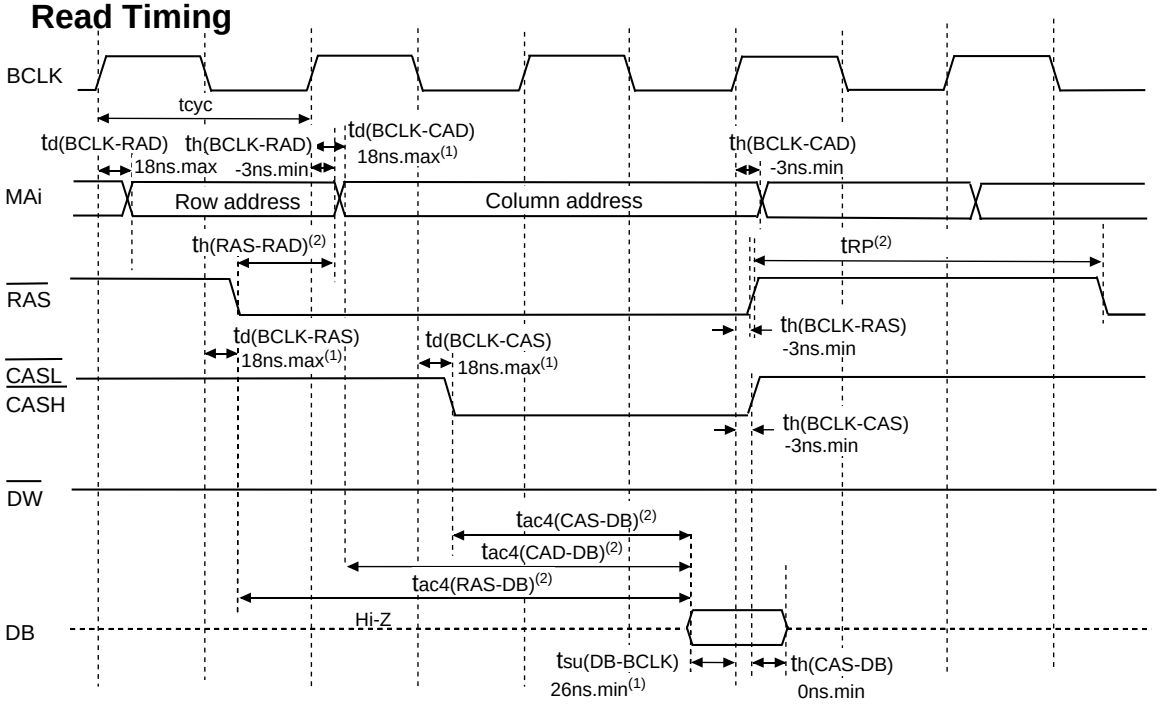
Figure 5.2 Vcc=5V Timing Diagram (1)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(When accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for the following combinations.
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. Varies with operation frequency:
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.5 Vcc=5V Timing Diagram (4)

VCC=3.3V

Table 5.24 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = –20 to 85°C, f(XIN)=20MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	IOH=-1mA	Vcc-0.6			V
		XOUT	IOH=-0.1mA	2.7			V
		XCOUT	No load applied		3.3		V
VOL	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	IOL=1mA			0.5	V
		XOUT	IOL=0.1mA			0.5	V
		XCOUT	No load applied		0		V
VT+-VT-	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN-TA4IN, TB0IN-TB5IN, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0OUT-TA4OUT, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
IIH	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE	VI=3V			4.0	µA
IIL	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE	VI=0V			-4.0	µA
RPULLUP	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	VI=0V	66	120	500	kΩ
RfXIN	Feedback Resistance	XIN			3.0		MΩ
RfXCIN	Feedback Resistance	XCIN			20.0		MΩ
VRAM	RAM Standby Voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
ICC	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to VSS.	f(XIN)=20 MHz, square wave, no division		26	38	mA
			f(XCIN)=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		µA
			f(XCIN)=32 kHz, with a wait state, through VDC, Topr=25° C		340		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.44 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-RAD)	Row Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-RAD)	Row Address Output Hold Time (BCLK standard)		0		ns
td(BCLK-CAD)	Column Address Output Delay Time			18	ns
th(BCLK-CAD)	Column Address Output Hold Time (BCLK standard)		0		ns
th(RAS-RAD)	Row Address Output Hold Time after RAS Output		(Note 1)		ns
td(BCLK-RAS)	RAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-RAS)	RAS Output Hold Time (BCLK standard)		0		ns
tRP	RAS High ("H") Hold Time		(Note 1)		ns
td(BCLK-CAS)	CAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-CAS)	CAS Output Hold Time (BCLK standard)		0		ns
td(BCLK-DW)	DW Output Delay Time (BCLK standard)			18	ns
th(BCLK-DW)	DW Output Hold Time (BCLK standard)		-3		ns
tsu(DB-CAS)	CAS Output Setup Time after DB output		(Note 1)		ns
th(BCLK-DB)	DB Signal Output Hold Time (BCLK standard)		-7		ns
tsu(CAS-RAS)	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

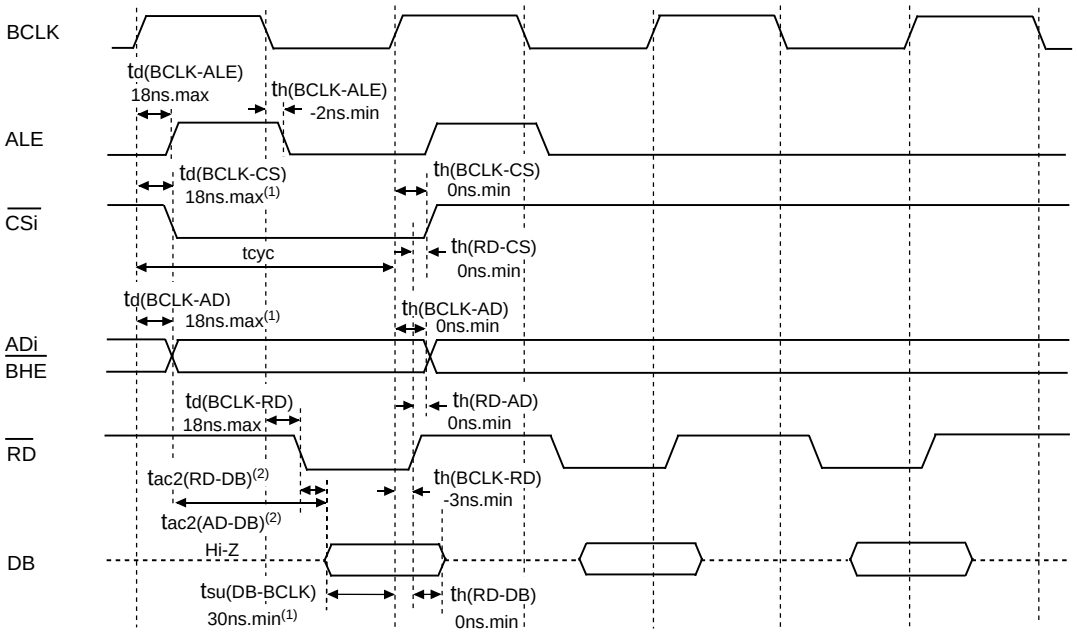
$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with no wait state)

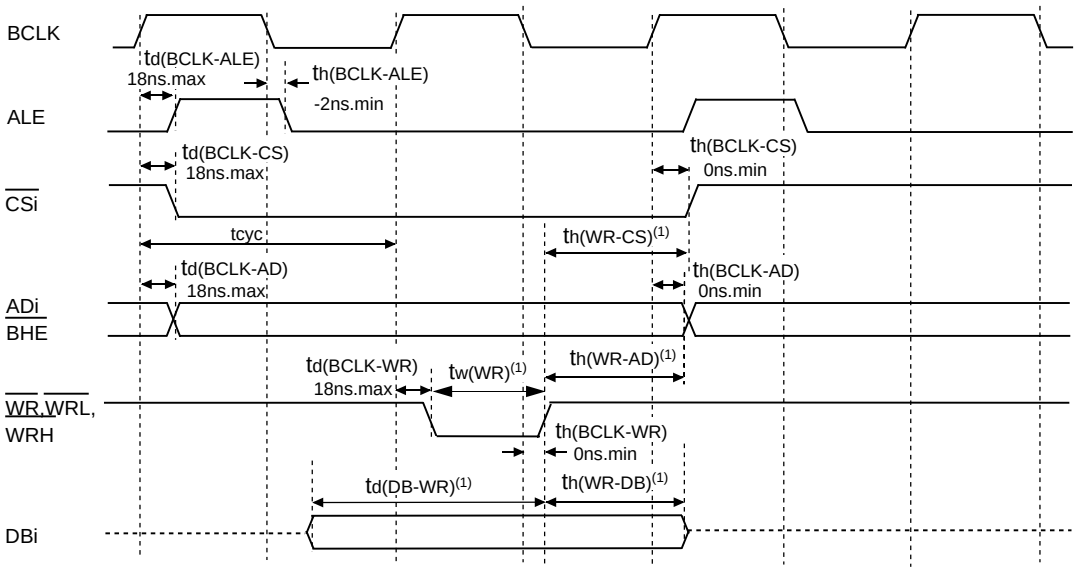
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac2(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac2(AD-DB)}$=(tcyc-35)ns.max

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.10 V_{CC}=3.3V Timing Diagram (1)

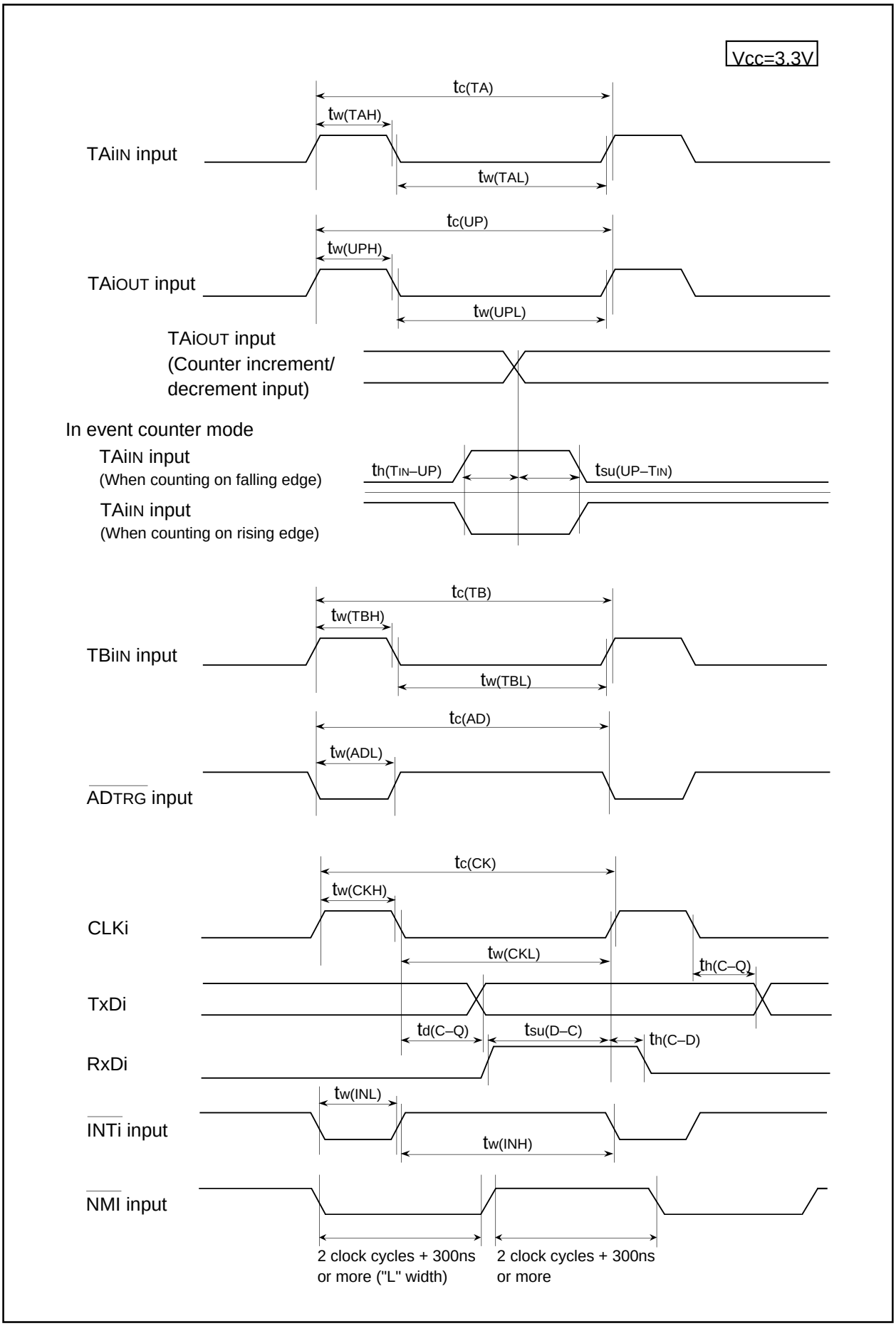


Figure 5.16 V_{CC}=3.3V Timing Diagram (7)

5.2 Electrical Characteristics (M32C/83T)

Table 5.45 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation		Topr=25° C	400	mW
Topr	Operating Ambient Temperature		T version	-40 to 85	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.

Table 5.46 Recommended Operating Conditions

(V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		4.2	5.0	5.5	V
AV_{CC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
AV_{SS}	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$	0.8V_{CC}		6.0	
V_{IL}	Input Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	V_{CC}=4.2 to 5.5V	0		32	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

REVISION HISTORY	M32C/83 GROUP (M32C/83, M32C/83T) Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	**2003-9**	-	New Document
1.20	**2003-12**		Maximum operating frequency changed from 30 MHz to 32 MHz. Overview, Electrical Characteristics Table 1.1 M32C/83 Group Performance (144-Pin Package) Table 1.2 M32C/83 Group Performance (100-Pin Package) Table 5.2 Recommended Operating Conditions Table 5.3 Electrical Characteristics
1.30	**2004-06**	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.41	**2006-01**	All Pages	**M32C/83T version** added; Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All Pages	Word standardized: Clock Generation Circuit , On-chip Oscillator, A/D Converter, D/A Converter, XY Conversion, Low -power consumption
			Overview
		1	• **1.1 Applications** Automobile added
		2, 3	• **Tables 1.1 and 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance**
		5	• **Table 1.3 M32C/83 Group (1) (M32C/83)** Information updated
			• **Table 1.3 M32C/83 Group (2) (M32C/83T)** M32C/83T product information added
			• **Figure 1.2 Product Numbering System** Classification modified
			• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
			• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
			• **Table 1.6 Pin Description** modified, notes added
			Memory
		21	• **Figure 3.1 Memory Map** modified; Note 2 modified, notes 3 and 4 added
			Special Function Registers (SFR)
		22 to 23	• Note 2 added
			Reset
		45	• **Figure 5.2 Reset Sequence** Note 2 added
			Electrical Characteristics
		46	• **Table 5.3 Electrical Characteristics** Minimum standard values for V_{OH} revised, values for I_{CC} when f(X_{IN})=32 MHz, square wave, no division revised, one condition of "f(X_{IN})=32 MHz, square wave, no division" deleted
		54	• **Table 5.23 Memory Expansion Mode and Microprocessor Mode** Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		62	• **Figure 5.8 V_{CC}=5 V Timing Diagram (7)** Timing for $\overline{NMI}$ input added
		64	• **Table 5.24 Electrical Characteristics** Minimum standard value for V_{OH} revised