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| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
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1.4 Pin Assignments

The MC68HC908QT4A, MC68H908QT2A, and MC68HC098QT1A are available in 8-pin packages. The MC68HC908QY4A, MC68HC908QY2A, and MC68HC908QY1A are available in 16-pin packages.

Figure 1-2 shows the pin assignment for these packages.

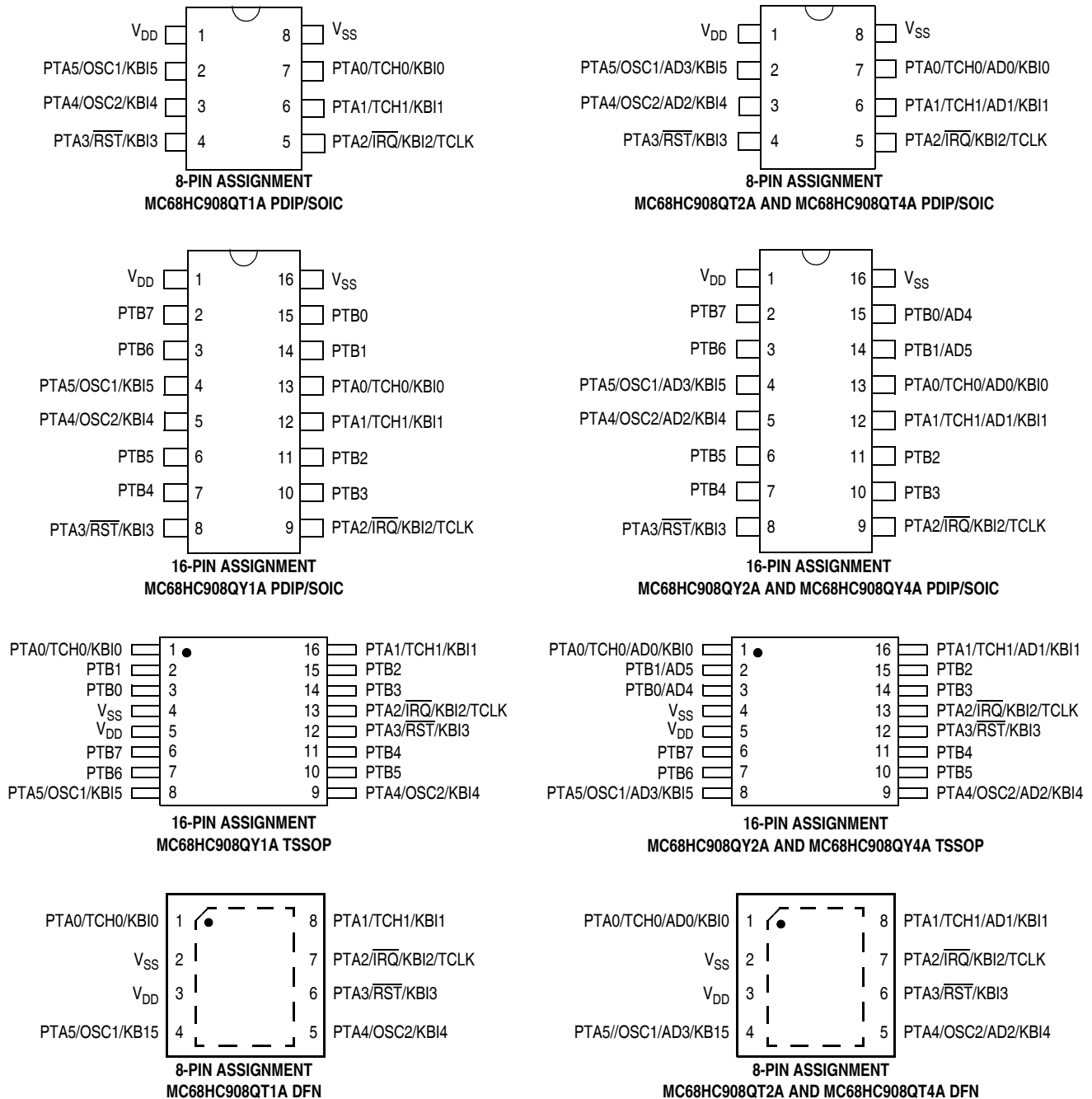


Figure 1-2. MCU Pin Assignments

4.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

4.5.1 Wait Mode

The AWU module is inactive in wait mode.

4.5.2 Stop Mode

When the AWU module is enabled (AWUIE = 1 in the keyboard interrupt enable register) it is activated automatically upon entering stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode. The AWU counters start from 0 each time stop mode is entered.

4.6 Registers

The AWU shares registers with the keyboard interrupt (KBI) module, the port A I/O module and configuration register 2. The following I/O registers control and monitor operation of the AWU:

- Port A data register (PTA)
- Keyboard interrupt status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)
- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)

4.6.1 Port A I/O Register

The port A data register (PTA) contains a data latch for the state of the AWU interrupt request, in addition to the data latches for port A.

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|-----------------|---------------------|------|------|------|------|-------|
| Read: | 0 | AWUL | PTA5 | PTA4 | PTA3 | PTA2 | PTA1 | PTA0 |
| Write: | | | | | | | | |
| Reset: | 0 | 0 | Unaffected by reset | | | | | |
| | | = Unimplemented | | | | | | |

Figure 4-2. Port A Data Register (PTA)

AWUL — Auto Wakeup Latch

This is a read-only bit which has the value of the auto wakeup interrupt request latch. The wakeup request signal is generated internally. There is no PTA6 port or any of the associated bits such as PTA6 data direction or pullup bits.

- 1 = Auto wakeup interrupt request is pending
- 0 = Auto wakeup interrupt request is not pending

NOTE

*PTA5–PTA0 bits are not used in conjunction with the auto wakeup feature.
To see a description of these bits, see [12.3.1 Port A Data Register](#).*

7.3.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset, the stack pointer is preset to \$00FF. The reset stack pointer (RSP) instruction sets the least significant byte to \$FF and does not affect the most significant byte. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

In the stack pointer 8-bit offset and 16-bit offset addressing modes, the stack pointer can function as an index register to access data on the stack. The CPU uses the contents of the stack pointer to determine the conditional address of the operand.

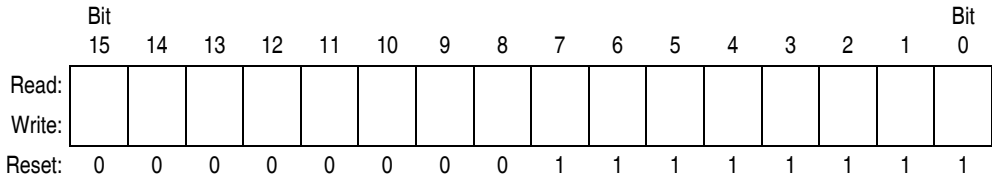


Figure 7-4. Stack Pointer (SP)

NOTE

The location of the stack is arbitrary and may be relocated anywhere in random-access memory (RAM). Moving the SP out of page 0 (\$0000 to \$00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.

7.3.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at \$FFFE and \$FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

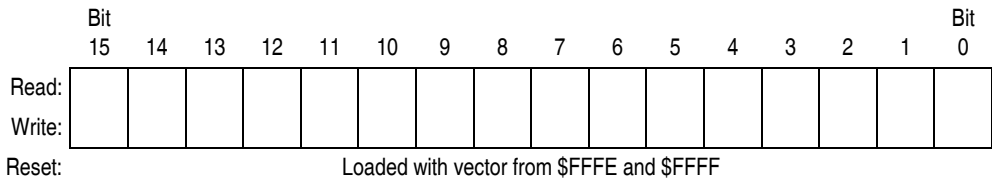
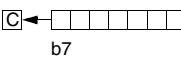
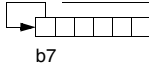


Figure 7-5. Program Counter (PC)

7.7 Instruction Set Summary

Table 7-1 provides a summary of the M68HC08 instruction set.

Table 7-1. Instruction Set Summary (Sheet 1 of 6)

| Source Form | Operation | Description | Effect on CCR | | | | | | Address Mode | Opcode | Operand | Cycles |
|--|---|---|---------------|---|---|---|---|---|--|--|---|--------------------------------------|
| | | | V | H | I | N | Z | C | | | | |
| ADC #opr ADC opr ADC opr ADC opr,X ADC opr,X ADC ,X ADC opr,SP ADC opr,SP | Add with Carry | $A \leftarrow (A) + (M) + (C)$ | ↑ | ↑ | – | ↑ | ↑ | ↑ | IMM DIR EXT IX2 IX1 IX SP1 SP2 | A9 B9 C9 D9 E9 F9 9EE9 9ED9 | ii dd hh ll ee ff ff ff ff ee ff | 2 3 4 4 3 2 4 5 |
| ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X ADD opr,SP ADD opr,SP | Add without Carry | $A \leftarrow (A) + (M)$ | ↑ | ↑ | – | ↑ | ↑ | ↑ | IMM DIR EXT IX2 IX1 IX SP1 SP2 | AB BB CB DB EB FB 9EEB 9EDB | ii dd hh ll ee ff ff ff ff ee ff | 2 3 4 4 3 2 4 5 |
| AIS #opr | Add Immediate Value (Signed) to SP | $SP \leftarrow (SP) + (16 \ll M)$ | – | – | – | – | – | – | IMM | A7 | ii | 2 |
| AIX #opr | Add Immediate Value (Signed) to H:X | $H:X \leftarrow (H:X) + (16 \ll M)$ | – | – | – | – | – | – | IMM | AF | ii | 2 |
| AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X AND opr,SP AND opr,SP | Logical AND | $A \leftarrow (A) \& (M)$ | 0 | – | – | ↑ | ↑ | – | IMM DIR EXT IX2 IX1 IX SP1 SP2 | A4 B4 C4 D4 E4 F4 9EE4 9ED4 | ii dd hh ll ee ff ff ff ff ee ff | 2 3 4 4 3 2 4 5 |
| ASL opr ASLA ASLX ASL opr,X ASL ,X ASL opr,SP | Arithmetic Shift Left (Same as LSL) |  | ↑ | – | – | ↑ | ↑ | ↑ | DIR INH INH IX1 IX SP1 | 38 48 58 68 78 9E68 | dd ff ff ff | 4 1 1 4 3 5 |
| ASR opr ASRA ASRX ASR opr,X ASR opr,X ASR opr,SP | Arithmetic Shift Right |  | ↑ | – | – | ↑ | ↑ | ↑ | DIR INH INH IX1 IX SP1 | 37 47 57 67 77 9E67 | dd ff ff ff ff | 4 1 1 4 3 5 |
| BCC rel | Branch if Carry Bit Clear | $PC \leftarrow (PC) + 2 + rel ? (C) = 0$ | – | – | – | – | – | – | REL | 24 | rr | 3 |
| BCLR n, opr | Clear Bit n in M | $M_n \leftarrow 0$ | – | – | – | – | – | – | DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7) | 11 13 15 17 19 1B 1D 1F | dd dd dd dd dd dd dd dd | 4 4 4 4 4 4 4 4 |
| BCS rel | Branch if Carry Bit Set (Same as BLO) | $PC \leftarrow (PC) + 2 + rel ? (C) = 1$ | – | – | – | – | – | – | REL | 25 | rr | 3 |
| BEQ rel | Branch if Equal | $PC \leftarrow (PC) + 2 + rel ? (Z) = 1$ | – | – | – | – | – | – | REL | 27 | rr | 3 |
| BGE opr | Branch if Greater Than or Equal To (Signed Operands) | $PC \leftarrow (PC) + 2 + rel ? (N \oplus V) = 0$ | – | – | – | – | – | – | REL | 90 | rr | 3 |
| BGT opr | Branch if Greater Than (Signed Operands) | $PC \leftarrow (PC) + 2 + rel ? (Z) \mid (N \oplus V) = 0$ | – | – | – | – | – | – | REL | 92 | rr | 3 |
| BHCC rel | Branch if Half Carry Bit Clear | $PC \leftarrow (PC) + 2 + rel ? (H) = 0$ | – | – | – | – | – | – | REL | 28 | rr | 3 |
| BHCS rel | Branch if Half Carry Bit Set | $PC \leftarrow (PC) + 2 + rel ? (H) = 1$ | – | – | – | – | – | – | REL | 29 | rr | 3 |
| BHI rel | Branch if Higher | $PC \leftarrow (PC) + 2 + rel ? (C) \mid (Z) = 0$ | – | – | – | – | – | – | REL | 22 | rr | 3 |

12.4.3 Port B Input Pullup Enable Register

The port B input pullup enable register (PTBPUE) contains a software configurable pullup device for each of the eight port B pins. Each bit is individually configurable and requires the corresponding data direction register, DDRBx, be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRBx bit is configured as output.

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Read: | PTBPUE7 | PTBPUE6 | PTBPUE5 | PTBPUE4 | PTBPUE3 | PTBPUE2 | PTBPUE2 | PTBPUE0 |
| Write: | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure 12-8. Port B Input Pullup Enable Register (PTBPUE)

PTBPUE[7:0] — Port B Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port B pins

- 1 = Corresponding port B pin configured to have internal pull if its DDRB bit is set to 0
- 0 = Pullup device is disconnected on the corresponding port B pin regardless of the state of its DDRB bit.

12.4.4 Port B Summary Table

[Table 12-2](#) summarizes the operation of the port A pins when used as a general-purpose input/output pins.

Table 12-2. Port B Pin Functions

| DDRB Bit | PTB Bit | I/O Pin Mode | Accesses to DDRB | Accesses to PTB | |
|----------|------------------|----------------------------|------------------|-----------------|--------------------------|
| | | | Read/Write | Read | Write |
| 0 | X ⁽¹⁾ | Input, Hi-Z ⁽²⁾ | DDRB7–DDRB0 | Pin | PTB7–PTB0 ⁽³⁾ |
| 1 | X | Output | DDRB7–DDRB0 | Pin | PTB7–PTB0 |

1. X = don't care
2. Hi-Z = high impedance
3. Writing affects data register, but does not affect the input.

13.4.2 Active Resets from Internal Sources

The $\overline{\text{RST}}$ pin is initially setup as a general-purpose input after a POR. Setting the RSTEN bit in the CONFIG2 register enables the pin for the reset function. This section assumes the RSTEN bit is set when describing activity on the $\overline{\text{RST}}$ pin.

NOTE

For POR and LVI resets, the SIM cycles through 4096 BUSCLKX4 cycles. The internal reset signal then follows the sequence from the falling edge of $\overline{\text{RST}}$ shown in Figure 13-4.

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

All internal reset sources actively pull the $\overline{\text{RST}}$ pin low for 32 BUSCLKX4 cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see Figure 13-4). An internal reset can be caused by an illegal address, illegal opcode, COP time out, LVI, or POR (see Figure 13-5).

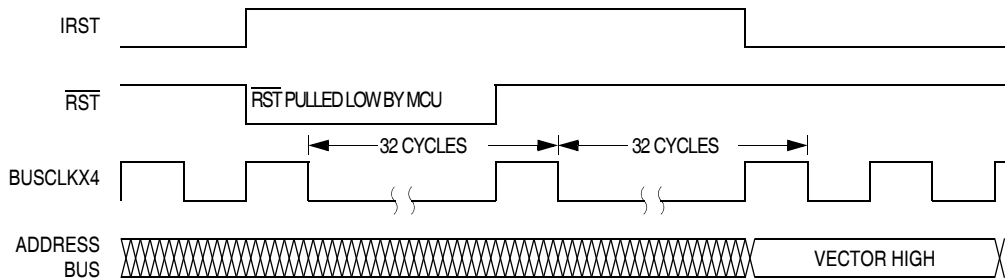


Figure 13-4. Internal Reset Timing

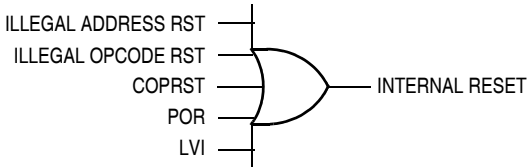


Figure 13-5. Sources of Internal Reset

Table 13-2. Reset Recovery Timing

| Reset Recovery Type | Actual Number of Cycles |
|---------------------|-------------------------|
| POR/LVI | 4163 (4096 + 64 + 3) |
| All others | 67 (64 + 3) |

13.6 Exception Control

Normal sequential program execution can be changed in three different ways:

1. Interrupts
 - a. Maskable hardware CPU interrupts
 - b. Non-maskable software interrupt instruction (SWI)
2. Reset
3. Break interrupts

13.6.1 Interrupts

An interrupt temporarily changes the sequence of program execution to respond to a particular event. [Figure 13-7](#) flow charts the handling of system interrupts.

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared).

At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the RTI instruction recovers the CPU register contents from the stack so that normal processing can resume. [Figure 13-8](#) shows interrupt entry timing. [Figure 13-9](#) shows interrupt recovery timing.

13.6.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. [Figure 13-10](#) demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

The LDA opcode is prefetched by both the INT1 and INT2 return-from-interrupt (RTI) instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE

To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.

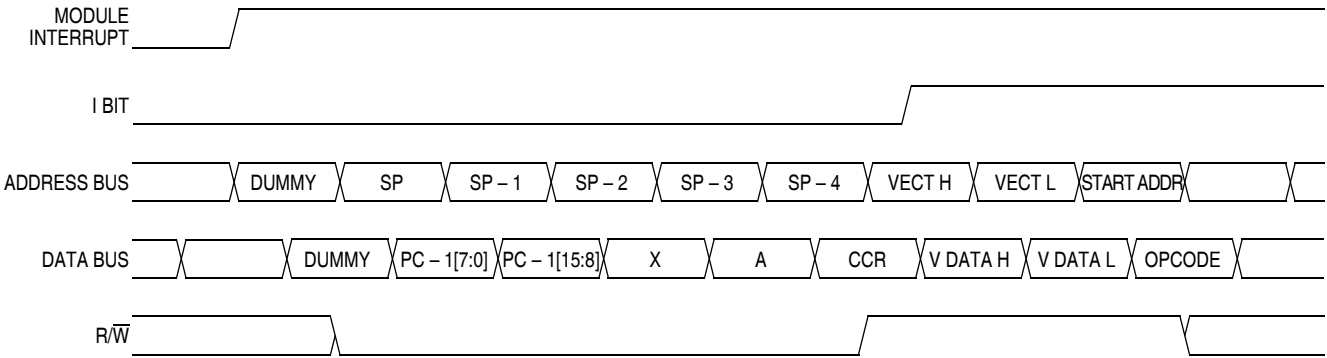


Figure 13-8. Interrupt Entry

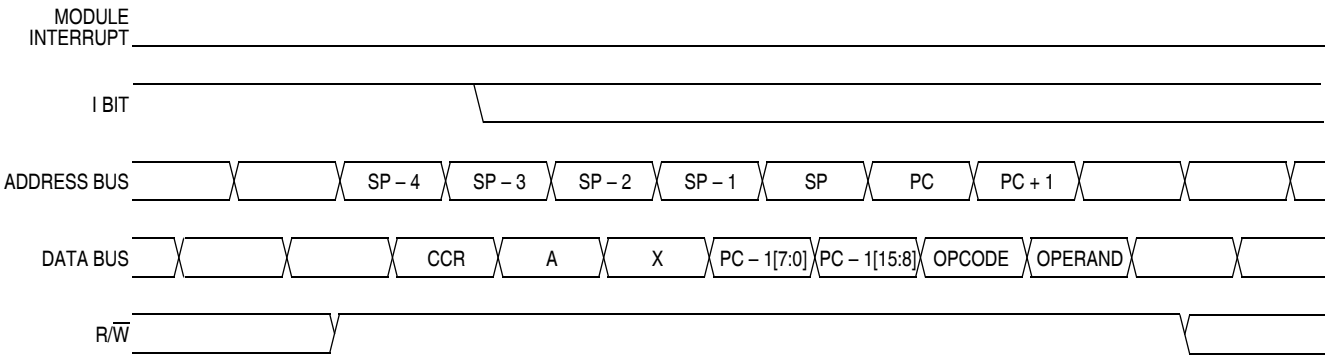


Figure 13-9. Interrupt Recovery

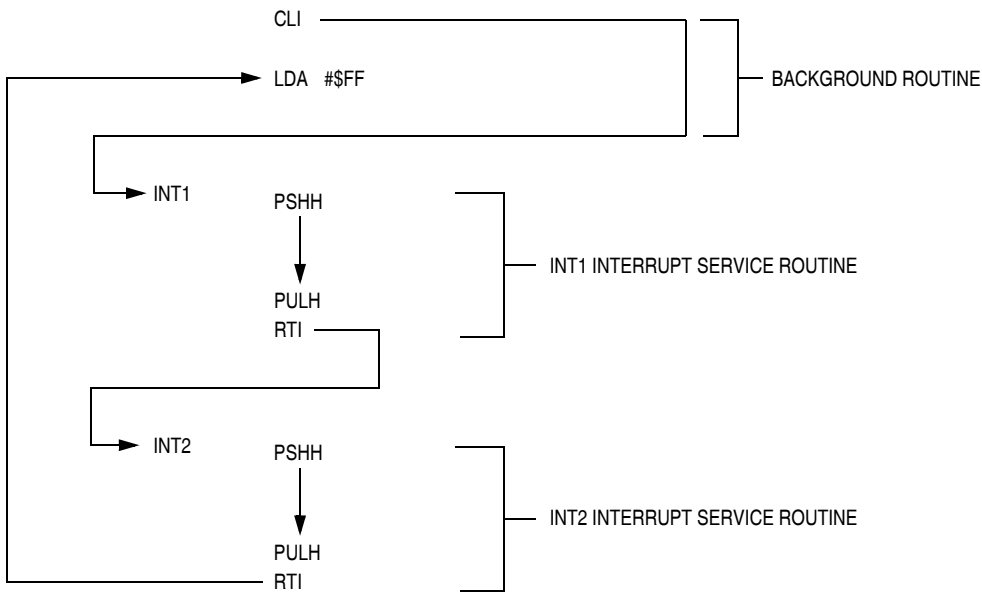


Figure 13-10. Interrupt Recognition Example

13.6.2.1 Interrupt Status Register 1

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|-----|-----|-----|-----|-----|---|-------|
| Read: | IF6 | IF5 | IF4 | IF3 | IF2 | IF1 | 0 | 0 |
| Write: | R | R | R | R | R | R | R | R |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

R = Reserved

Figure 13-11. Interrupt Status Register 1 (INT1)

IF1–IF6 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

Bit 0, 1 — Always read 0

13.6.2.2 Interrupt Status Register 2

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|------|------|------|------|-----|-----|-------|
| Read: | IF14 | IF13 | IF12 | IF11 | IF10 | IF9 | IF8 | IF7 |
| Write: | R | R | R | R | R | R | R | R |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

R = Reserved

Figure 13-12. Interrupt Status Register 2 (INT2)

IF7–IF14 — Interrupt Flags

This flag indicates the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

13.6.2.3 Interrupt Status Register 3

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|------|------|------|------|------|------|-------|
| Read: | IF22 | IF21 | IF20 | IF19 | IF18 | IF17 | IF16 | IF15 |
| Write: | R | R | R | R | R | R | R | R |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

R = Reserved

Figure 13-13. Interrupt Status Register 3 (INT3)

IF15–IF22 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in [Table 13-3](#).

1 = Interrupt request present

0 = No interrupt request present

14.7 I/O Signals

The TIM module can share its pins with the general-purpose I/O pins. See [Figure 14-1](#) for the port pins that are shared.

14.7.1 TIM Channel I/O Pins (TCH1:TCH0)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. TCH0 can be configured as buffered output compare or buffered PWM pin.

14.7.2 TIM Clock Pin (TCLK)

TCLK is an external clock input that can be the clock source for the counter instead of the prescaled internal bus clock. Select the TCLK input by writing 1s to the three prescaler select bits, PS[2:0]. [14.8.1 TIM Status and Control Register](#) The minimum TCLK pulse width is specified in the Timer Interface Module Characteristics table in the Electricals section. The maximum TCLK frequency is the least of 4 MHz or bus frequency $\div 2$.

14.8 Registers

The following registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM control registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H:TCH0L and TCH1H:TCH1L)

14.8.1 TIM Status and Control Register

The TIM status and control register (TSC) does the following:

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the counter
- Resets the counter
- Prescales the counter clock

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|--------|-------|------|-------|------|---|-----|-----|-------|
| Read: | TOF | TOIE | TSTOP | 0 | 0 | PS2 | PS1 | PS0 |
| Write: | 0 | | | TRST | | | | |
| Reset: | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

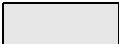
 = Unimplemented

Figure 14-4. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TSC register when TOF is set and then writing a 0 to TOF.

Chapter 15

Development Support

15.1 Introduction

This section describes the break module, the monitor module (MON), and the monitor mode entry methods.

15.2 Break Module (BRK)

The break module can generate a break interrupt that stops normal program flow at a defined address to enter a background program.

Features include:

- Accessible input/output (I/O) registers during the break Interrupt
- Central processor unit (CPU) generated break interrupts
- Software-generated break interrupts
- Computer operating properly (COP) disabling during break interrupts

15.2.1 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ($\overline{\text{BKPT}}$) to the system integration module (SIM). The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI). The program counter vectors to \$FFFC and \$FFFD (\$FEFC and \$FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a 1 to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt is generated. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the microcontroller unit (MCU) to normal operation.

Figure 15-2 shows the structure of the break module.

When the internal address bus matches the value written in the break address registers or when software writes a 1 to the BRKA bit in the break status and control register, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC and \$FFFD (\$FEFC and \$FEFD in monitor mode)

NOTE

If the reset vector is blank and monitor mode is entered, the chip will see an additional reset cycle after the initial power-on reset (POR). Once the reset vector has been programmed, the traditional method of applying a voltage, V_{TST} , to \overline{IRQ} must be used to enter monitor mode.

If monitor mode was entered as a result of the reset vector being blank, the COP is always disabled regardless of the state of \overline{IRQ} .

If the voltage applied to the \overline{IRQ} is less than V_{TST} , the MCU will come out of reset in user mode. Internal circuitry monitors the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased (\$FF). When the MCU comes out of reset, it is forced into monitor mode without requiring high voltage on the \overline{IRQ} pin. Once out of reset, the monitor code is initially executing with the internal clock at its default frequency.

If \overline{IRQ} is held high, all pins will default to regular input port functions except for PTA0 and PTA5 which will operate as a serial communication port and OSC1 input respectively (refer to [Figure 15-11](#)). That will allow the clock to be driven from an external source through OSC1 pin.

If \overline{IRQ} is held low, all pins will default to regular input port function except for PTA0 which will operate as serial communication port. Refer to [Figure 15-12](#).

Regardless of the state of the \overline{IRQ} pin, it will not function as a port input pin in monitor mode. Bit 2 of the Port A data register will always read 0. The BIH and BIL instructions will behave as if the \overline{IRQ} pin is enabled, regardless of the settings in the configuration register. See [Chapter 5 Configuration Register \(CONFIG\)](#).

The COP module is disabled in forced monitor mode. Any reset other than a power-on reset (POR) will automatically force the MCU to come back to the forced monitor mode.

15.3.1.3 Monitor Vectors

In monitor mode, the MCU uses different vectors for reset, SWI (software interrupt), and break interrupt than those for user mode. The alternate vectors are in the \$FE page instead of the \$FF page and allow code execution from the internal monitor firmware instead of user code.

NOTE

Exiting monitor mode after it has been initiated by having a blank reset vector requires a power-on reset (POR). Pulling \overline{RST} (when \overline{RST} pin available) low will not exit monitor mode in this situation.

[Table 15-2](#) summarizes the differences between user mode and monitor mode regarding vectors.

Table 15-2. Mode Difference

| Modes | Functions | | | | | |
|---------|-------------------|------------------|-------------------|------------------|-----------------|----------------|
| | Reset Vector High | Reset Vector Low | Break Vector High | Break Vector Low | SWI Vector High | SWI Vector Low |
| User | \$FFFE | \$FFFF | \$FFFC | \$FFFD | \$FFFC | \$FFFD |
| Monitor | \$FEFE | \$FEFF | \$FEFC | \$FEFD | \$FEFC | \$FEFD |

15.3.1.4 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.

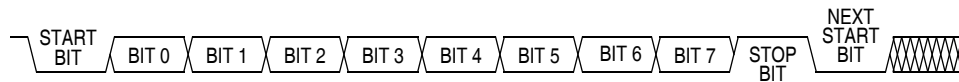


Figure 15-13. Monitor Data Format

15.3.1.5 Break Signal

A start bit (logic 0) followed by nine logic 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits and then echoes back the break signal.

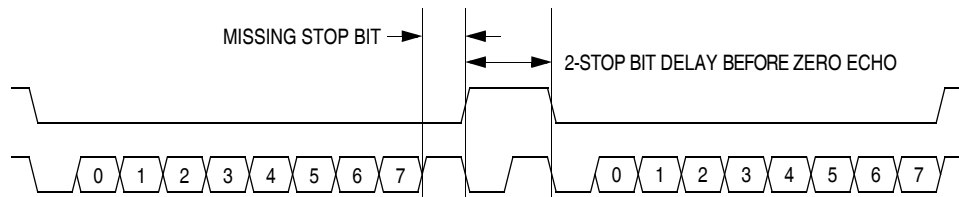


Figure 15-14. Break Transaction

15.3.1.6 Baud Rate

The monitor communication baud rate is controlled by the frequency of the external or internal oscillator and the state of the appropriate pins as shown in [Table 15-1](#).

[Table 15-1](#) also lists the bus frequencies to achieve standard baud rates. The effective baud rate is the bus frequency divided by 256 when using an external oscillator. When using the internal oscillator in forced monitor mode, the effective baud rate is the bus frequency divided by 335.

15.3.1.7 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

NOTE

Wait one bit time after each echo before sending the next byte.

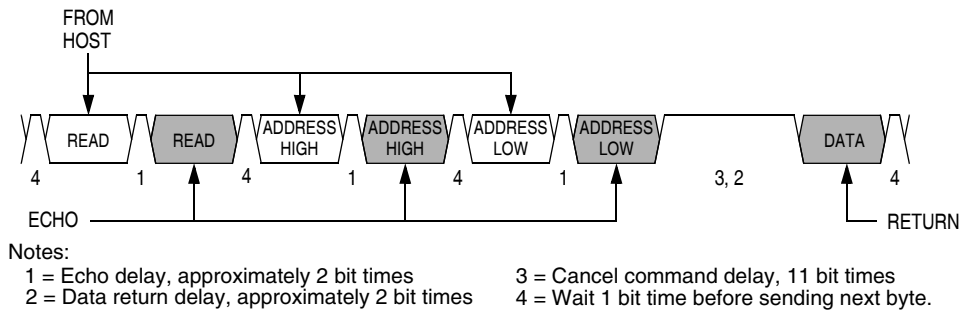


Figure 15-15. Read Transaction

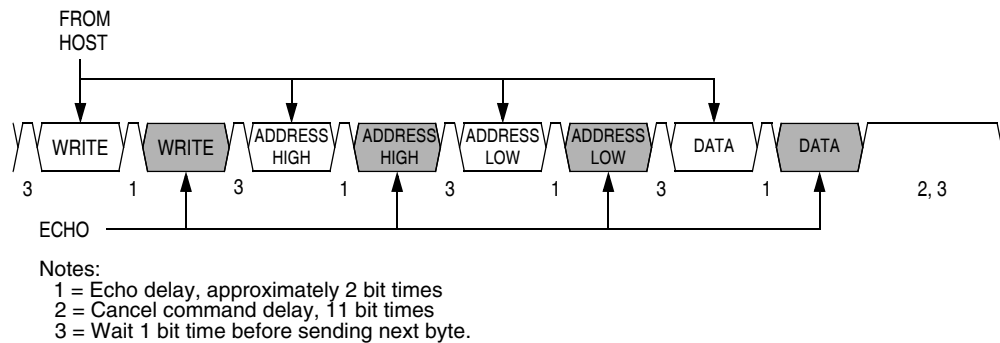


Figure 15-16. Write Transaction

A brief description of each monitor mode command is given in [Table 15-3](#) through [Table 15-8](#).

Table 15-3. READ (Read Memory) Command

| | |
|--|--|
| Description | Read byte from memory |
| Operand | 2-byte address in high-byte:low-byte order |
| Data Returned | Returns contents of specified address |
| Opcode | \$4A |
| <p style="text-align: center;">Command Sequence</p> | |



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