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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, PWM
Number of I/O	5
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.209", 5.30mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908qt2amdwe

MC68HC908QY4A MC68HC908QT4A
MC68HC908QY2A MC68HC908QT2A
MC68HC908QY1A MC68HC908QT1A
Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

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General Description

- On-chip random-access memory (RAM)
- 2-channel, 16-bit timer interface (TIM) module
- 6-channel, 10-bit analog-to-digital converter (ADC) with internal bandgap reference channel (ADC10)
- Up to 13 bidirectional input/output (I/O) lines and one input only:
 - Six shared with KBI
 - Six shared with ADC
 - Two shared with TIM
 - One input only shared with IRQ
 - High current sink/source capability on all port pins
 - Selectable pullups on all ports, selectable on an individual bit basis
 - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
 - Programmable for rising/falling or high/low level detect
- Low-voltage inhibit (LVI) module features:
 - Software selectable trip point
- System protection features:
 - Computer operating properly (COP) watchdog
 - Low-voltage detection with reset
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$) shared with general-purpose input pin
- Master asynchronous reset pin with internal pullup ($\overline{\text{RST}}$) shared with general-purpose input/output (I/O) pin
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HC908QY4A, MC68HC908QY2A and MC68HC908QY1A are available in these packages:
 - 16-pin plastic dual in-line package (PDIP)
 - 16-pin small outline integrated circuit (SOIC) package
 - 16-pin thin shrink small outline packages (TSSOP)
- MC68HC908QT4A, MC68HC908QT2A and MC68HC908QT1A are available in these packages:
 - 8-pin PDIP
 - 8-pin SOIC
 - 8-pin dual flat no lead (DFN) package

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8×8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

Memory

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$001D	IRQ Status and Control Register (INTSCR) See page 81.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0
\$001E	Configuration Register 2 (CONFIG2) ⁽¹⁾ See page 57.	Read:	IRQPUD	IRQEN	R	R	R	R	OSCENIN-STOP	RSTEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0
		1. One-time writable register after each reset.		2. RSTEN reset to 0 by a power-on reset (POR) only.						
\$001F	Configuration Register 1 (CONFIG1) ⁽¹⁾ See page 58.	Read:	COPRS	LVISTOP	LVI RSTD	LVIPWRD	LVITRIP	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0 ⁽²⁾	0	0	0
		1. One-time writable register after each reset.		2. LVITRIP reset to 0 by a power-on reset (POR) only.						
\$0020	TIM Status and Control Register (TSC) See page 132.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
\$0021	TIM Counter Register High (TCNTH) See page 134.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL) See page 134.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0023	TIM Counter Modulo Register High (TMODH) See page 134.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMODL) See page 134.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0) See page 135.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H) See page 137.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$0027	TIM Channel 0 Register Low (TCH0L) See page 137.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented
 = Reserved
U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 5)

Memory

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$FE00	Break Status Register (BSR) See page 143.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							0	
		Reset:	0							
\$FE01	SIM Reset Status Register (SRSR) See page 122.	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
\$FE02	Break Auxiliary Register (BRKAR) See page 143.	Read:	0	0	0	0	0	0	0	BDCOP
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE03	Break Flag Control Register (BFCR) See page 143.	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
\$FE04	Interrupt Status Register 1 (INT1) See page 119.	Read:	IF6	IF5	IF4	IF3	IF2	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$FE05	Interrupt Status Register 2 (INT2) See page 119.	Read:	IF14	IF13	IF12	IF11	IF10	IF9	IF8	IF7
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$FE06	Interrupt Status Register 3 (INT3) See page 119.	Read:	IF22	IF21	IF20	IF19	IF18	IF17	IF16	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$FE07	Reserved									
\$FE08	FLASH Control Register (FLCR) See page 29.	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE09	Break Address High Register (BRKH) See page 142.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE0A	Break Address low Register (BRKL) See page 142.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FE0B	Break Status and Control Register (BRKSCR) See page 143.	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented
 = Reserved
 U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 5)

3.4 Interrupts

When AIEN is set, the ADC10 is capable of generating a CPU interrupt after each conversion. A CPU interrupt is generated when the conversion completes (indicated by COCO being set). COCO will set at the end of a conversion regardless of the state of AIEN.

3.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

3.5.1 Wait Mode

The ADC10 will continue the conversion process and will generate an interrupt following a conversion if AIEN is set. If the ADC10 is not required to bring the MCU out of wait mode, ensure that the ADC10 is not in continuous conversion mode by clearing ADCO in the ADC10 status and control register before executing the WAIT instruction. In single conversion mode the ADC10 automatically enters a low-power state when the conversion is complete. It is not necessary to set the channel select bits (ADCH[4:0]) to all 1s to enter a low power state.

3.5.2 Stop Mode

If ACLKEN is clear, executing a STOP instruction will abort the current conversion and place the ADC10 in a low-power state. Upon return from stop mode, a write to ADSCR is required to resume conversions, and the result stored in ADRH and ADRL will represent the last completed conversion until the new conversion completes.

If ACLKEN is set, the ADC10 continues normal operation during stop mode. The ADC10 will continue the conversion process and will generate an interrupt following a conversion if AIEN is set. If the ADC10 is not required to bring the MCU out of stop mode, ensure that the ADC10 is not in continuous conversion mode by clearing ADCO in the ADC10 status and control register before executing the STOP instruction. In single conversion mode the ADC10 automatically enters a low-power state when the conversion is complete. It is not necessary to set the channel select bits (ADCH[4:0]) to all 1s to enter a low-power state.

If ACLKEN is set, a conversion can be initiated while in stop using the external hardware trigger ADEXTCO when in external convert mode. The ADC10 will operate in a low-power mode until the trigger is asserted, at which point it will perform a conversion and assert the interrupt when complete (if AIEN is set).

3.6 ADC10 During Break Interrupts

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. BCFE in the break flag control register (BFCR) enables software to clear status bits during the break state. See BFCR in the SIM section of this data sheet.

To allow software to clear status bits during a break interrupt, write a 1 to BCFE. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to BCFE. With BCFE cleared (its default state), software can read and write registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the

4.6.2 Keyboard Status and Control Register

The keyboard status and control register (KBSCR):

- Flags keyboard/auto wakeup interrupt requests
- Acknowledges keyboard/auto wakeup interrupt requests
- Masks keyboard/auto wakeup interrupt requests

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:						ACKK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-3. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used

These read-only bits always read as 0s.

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port A or auto wakeup. Reset clears the KEYF bit.

- 1 = Keyboard/auto wakeup interrupt pending
- 0 = No keyboard/auto wakeup interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a 1 to this write-only bit clears the keyboard/auto wakeup interrupt request on port A and auto wakeup logic. ACKK always reads as 0. Reset clears ACKK.

IMASKK— Keyboard Interrupt Mask Bit

Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wakeup. Reset clears the IMASKK bit.

- 1 = Keyboard/auto wakeup interrupt requests masked
- 0 = Keyboard/auto wakeup interrupt requests not masked

NOTE

MODEK is not used in conjunction with the auto wakeup feature. To see a description of this bit, see [9.8.1 Keyboard Status and Control Register \(KBSCR\)](#).

4.6.3 Keyboard Interrupt Enable Register

The keyboard interrupt enable register (KBIER) enables or disables the auto wakeup to operate as a keyboard/auto wakeup interrupt input.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-4. Keyboard Interrupt Enable Register (KBIER)

Configuration Register (CONFIG)

IRQPUD — $\overline{\text{IRQ}}$ Pin Pullup Control Bit

- 1 = Internal pullup is disconnected
- 0 = Internal pullup is connected between $\overline{\text{IRQ}}$ pin and V_{DD}

IRQEN — $\overline{\text{IRQ}}$ Pin Function Selection Bit

- 1 = Interrupt request function active in pin
- 0 = Interrupt request function inactive in pin

OSCENINSTOP— Oscillator Enable in Stop Mode Bit

OSCENINSTOP, when set, will allow the clock source to continue to generate clocks in stop mode. This function can be used to keep the auto-wakeup running while the rest of the microcontroller stops. When clear, the clock source is disabled when the microcontroller enters stop mode.

- 1 = Oscillator enabled to operate during stop mode
- 0 = Oscillator disabled during stop mode

RSTEN — $\overline{\text{RST}}$ Pin Function Selection

- 1 = Reset function active in pin
- 0 = Reset function inactive in pin

NOTE

The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVITRIP	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS (Out of Stop Mode) — COP Reset Period Selection Bit

- 1 = COP reset short cycle = $8176 \times \text{BUSCLKX4}$
- 0 = COP reset long cycle = $262,128 \times \text{BUSCLKX4}$

COPRS (In Stop Mode) — Auto Wakeup Period Selection Bit, depends on OSCSTOPEN in CONFIG2 and external clock source

- 1 = Auto wakeup short cycle = $512 \times (\text{INTRCOSC or BUSCLKX2})$
- 0 = Auto wakeup long cycle = $16,384 \times (\text{INTRCOSC or BUSCLKX2})$

LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

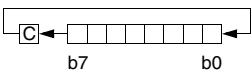
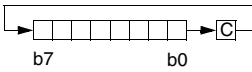
- 1 = LVI enabled during stop mode
- 0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable Bit

LVIRSTD disables the reset signal from the LVI module.

- 1 = LVI module resets disabled
- 0 = LVI module resets enabled

Table 7-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles	
			V	H	I	N	Z					C
PULA	Pull A from Stack	$SP \leftarrow (SP + 1); \text{Pull (A)}$	-	-	-	-	-	-	INH	86		2
PULH	Pull H from Stack	$SP \leftarrow (SP + 1); \text{Pull (H)}$	-	-	-	-	-	-	INH	8A		2
PULX	Pull X from Stack	$SP \leftarrow (SP + 1); \text{Pull (X)}$	-	-	-	-	-	-	INH	88		2
ROL <i>opr</i> ROLA ROLX ROL <i>opr,X</i> ROL ,X ROL <i>opr,SP</i>	Rotate Left through Carry		↑	-	-	-	↑	↑	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR <i>opr</i> RORA RORX ROR <i>opr,X</i> ROR ,X ROR <i>opr,SP</i>	Rotate Right through Carry		↑	-	-	-	↑	↑	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	$SP \leftarrow \$FF$	-	-	-	-	-	-	INH	9C		1
RTI	Return from Interrupt	$SP \leftarrow (SP + 1); \text{Pull (CCR)}$ $SP \leftarrow (SP + 1); \text{Pull (A)}$ $SP \leftarrow (SP + 1); \text{Pull (X)}$ $SP \leftarrow (SP + 1); \text{Pull (PCH)}$ $SP \leftarrow (SP + 1); \text{Pull (PCL)}$	↑	↑	↑	↑	↑	↑	INH	80		7
RTS	Return from Subroutine	$SP \leftarrow SP + 1; \text{Pull (PCH)}$ $SP \leftarrow SP + 1; \text{Pull (PCL)}$	-	-	-	-	-	-	INH	81		4
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr,X</i> SBC <i>opr,X</i> SBC ,X SBC <i>opr,SP</i> SBC <i>opr,SP</i>	Subtract with Carry	$A \leftarrow (A) - (M) - (C)$	↑	-	-	-	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	$C \leftarrow 1$	-	-	-	-	-	1	INH	99		1
SEI	Set Interrupt Mask	$I \leftarrow 1$	-	-	1	-	-	-	INH	9B		2
STA <i>opr</i> STA <i>opr</i> STA <i>opr,X</i> STA <i>opr,X</i> STA ,X STA <i>opr,SP</i> STA <i>opr,SP</i>	Store A in M	$M \leftarrow (A)$	0	-	-	-	↑	↑	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ff ee ff	3 4 4 3 2 4 5
STHX <i>opr</i>	Store H:X in M	$(M:M + 1) \leftarrow (H:X)$	0	-	-	-	↑	↑	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	$I \leftarrow 0; \text{Stop Processing}$	-	-	0	-	-	-	INH	8E		1
STX <i>opr</i> STX <i>opr</i> STX <i>opr,X</i> STX <i>opr,X</i> STX ,X STX <i>opr,SP</i> STX <i>opr,SP</i>	Store X in M	$M \leftarrow (X)$	0	-	-	-	↑	↑	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ff ee ff	3 4 4 3 2 4 5
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr,X</i> SUB <i>opr,X</i> SUB ,X SUB <i>opr,SP</i> SUB <i>opr,SP</i>	Subtract	$A \leftarrow (A) - (M)$	↑	-	-	-	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5

9.3.2 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the internal pullup or pulldown device to pull the pin to its deasserted level. Therefore a false interrupt can occur as soon as the pin is enabled.

To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting IMASKK in KBSCR.
2. Enable the KBI polarity by setting the appropriate KBIPx bits in KBIPR.
3. Enable the KBI pins by setting the appropriate KBIE_x bits in KBIER.
4. Write to ACKK in KBSCR to clear any false interrupts.
5. Clear IMASKK.

An interrupt signal on an edge sensitive pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge and level sensitive pin must be acknowledged after a delay that depends on the external load.

9.4 Interrupts

The following KBI source can generate interrupt requests:

- Keyboard flag (KEYF) — The KEYF bit is set when any enabled KBI pin is asserted based on the KBI mode and pin polarity. The keyboard interrupt mask bit, IMASKK, is used to enable or disable KBI interrupt requests.

9.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

9.5.1 Wait Mode

The KBI module remains active in wait mode. Clearing IMASKK in KBSCR enables keyboard interrupt requests to bring the MCU out of wait mode.

9.5.2 Stop Mode

The KBI module remains active in stop mode. Clearing IMASKK in KBSCR enables keyboard interrupt requests to bring the MCU out of stop mode.

9.6 KBI During Break Interrupts

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See BFCR in the SIM section of this data sheet.

To allow software to clear status bits during a break interrupt, write a 1 to BCFE. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to BCFE. With BCFE cleared (its default state), software can read and write registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is cleared. After the break, doing the second step clears the status bit.

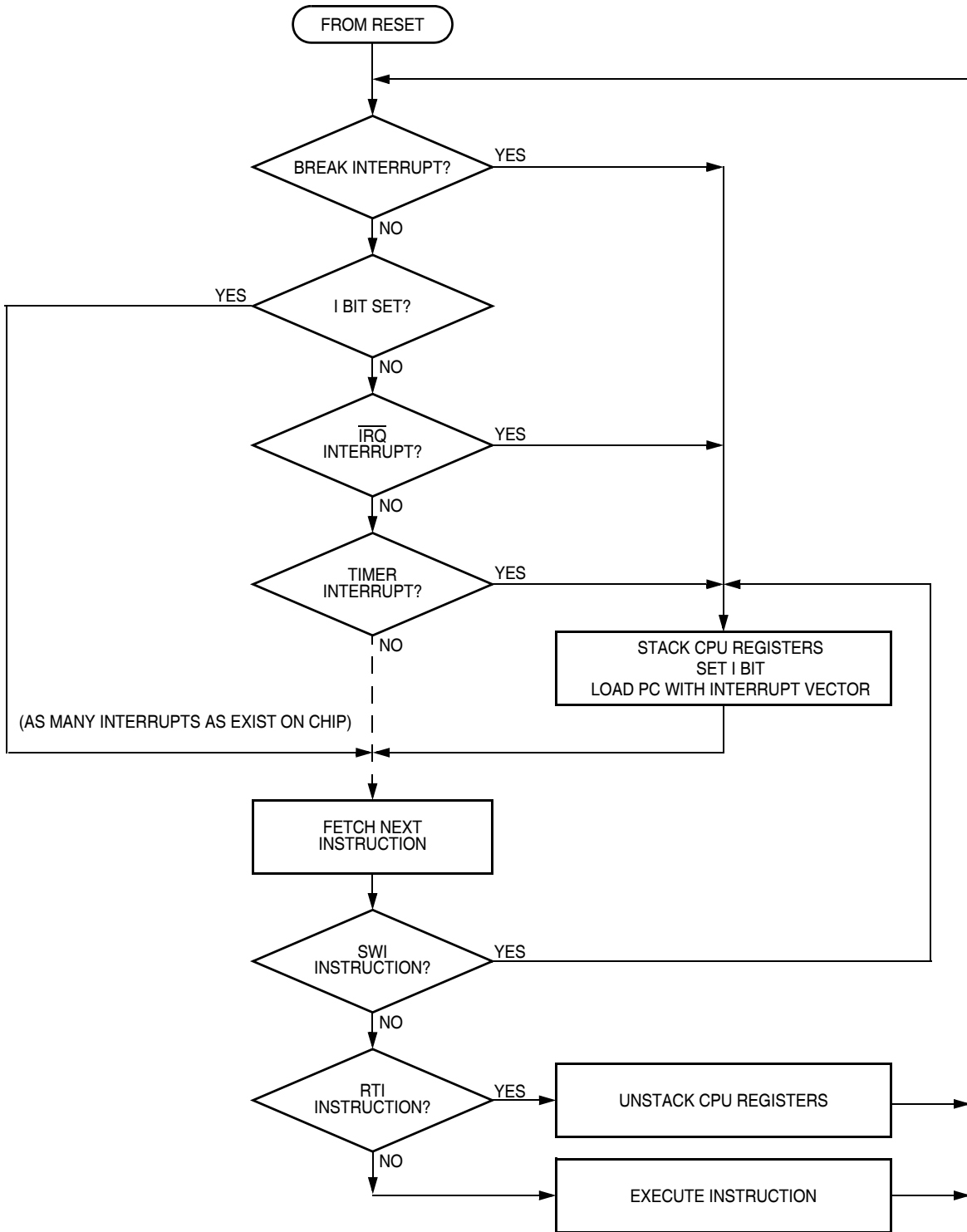


Figure 13-7. Interrupt Processing

Timer Interface Module (TIM)

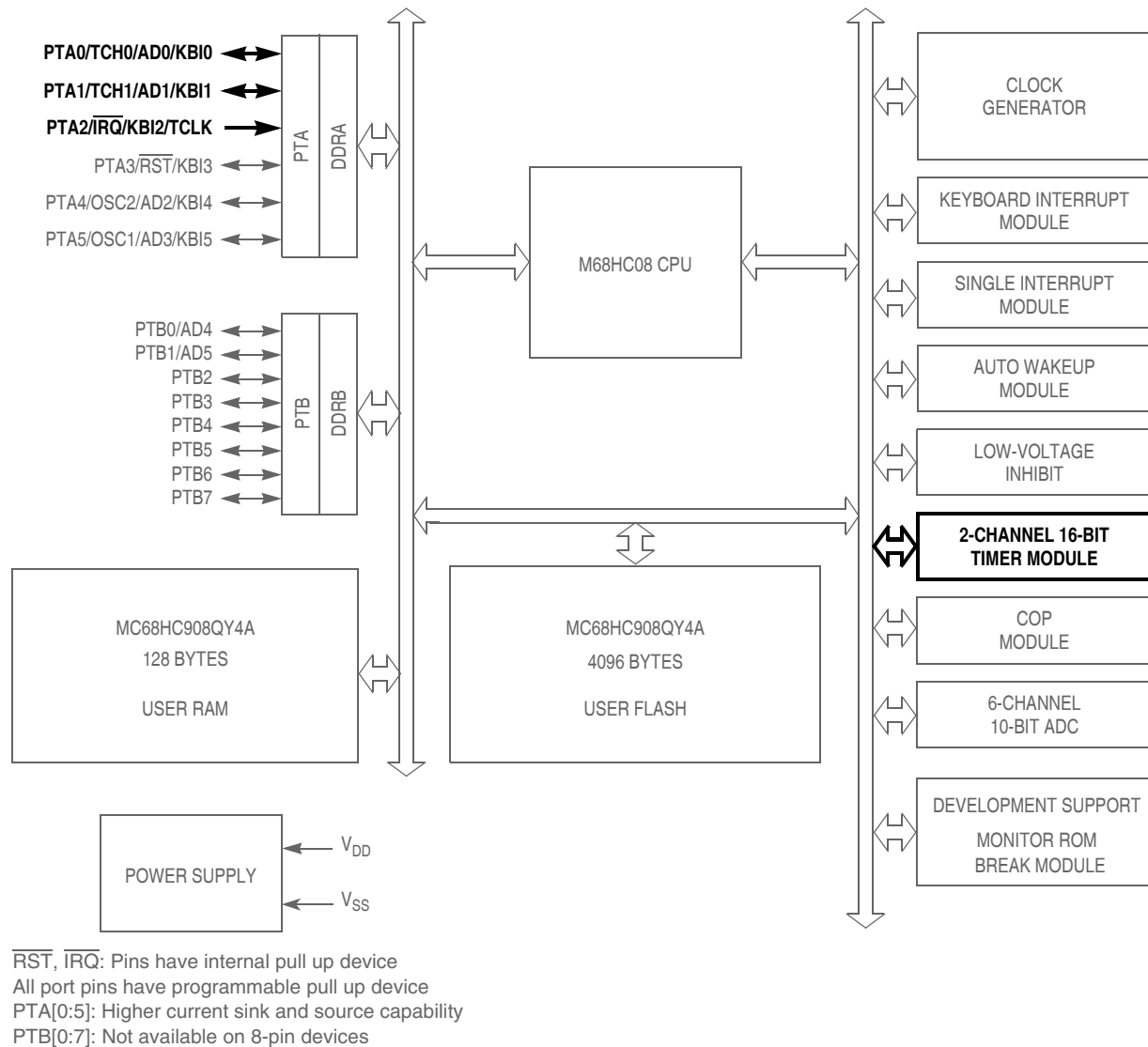


Figure 14-1. Block Diagram Highlighting TIM Block and Pins

14.3.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can be enabled to generate interrupt requests.

14.3.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can be enabled to generate interrupt requests.

14.8.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

NOTE

If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.

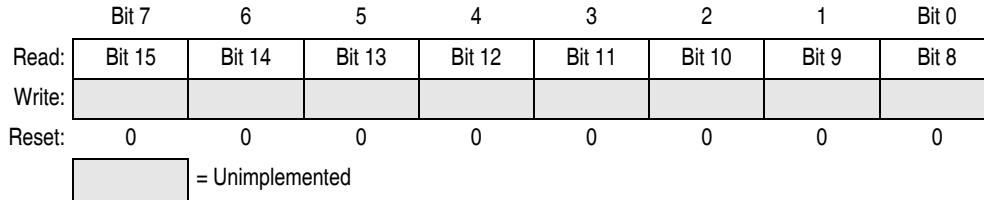


Figure 14-5. TIM Counter High Register (TCNTH)

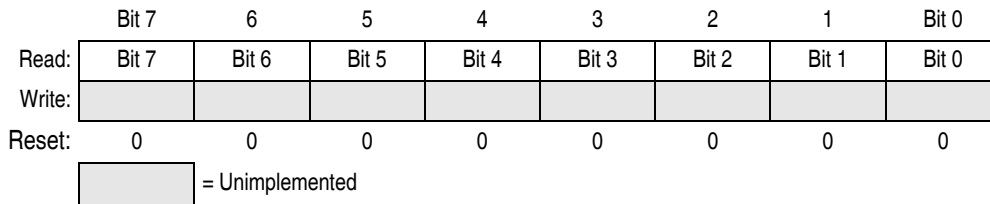


Figure 14-6. TIM Counter Low Register (TCNTL)

14.8.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the counter. When the counter reaches the modulo value, the overflow flag (TOF) becomes set, and the counter resumes counting from \$0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

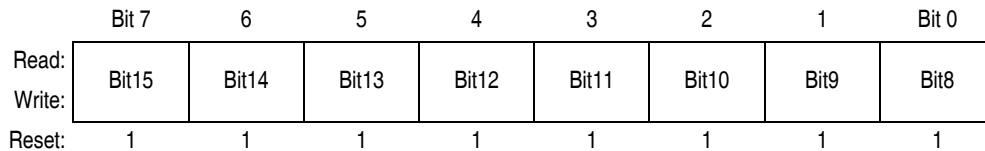


Figure 14-7. TIM Counter Modulo High Register (TMODH)

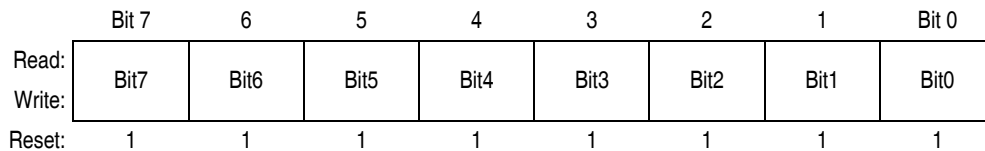


Figure 14-8. TIM Counter Modulo Low Register (TMODL)

NOTE

Reset the counter before writing to the TIM counter modulo registers.

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the counter overflows. When channel x is an input capture channel, TOVx has no effect.

1 = Channel x pin toggles on TIM counter overflow.

0 = Channel x pin does not toggle on TIM counter overflow.

NOTE

When TOVx is set, a counter overflow takes precedence over a channel x output compare if both occur at the same time.

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at 1, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As Figure 14-11 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

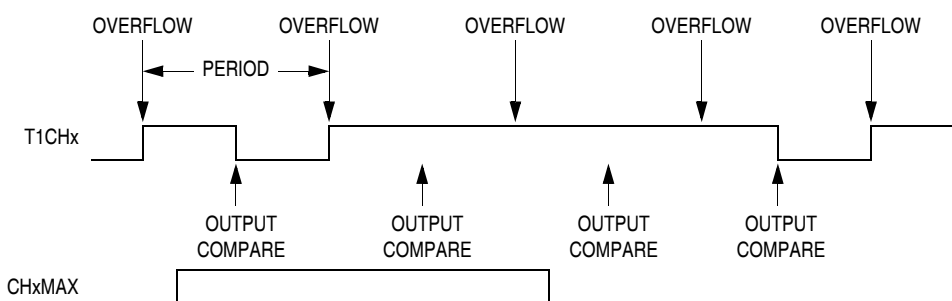


Figure 14-11. CHxMAX Latency

14.8.5 TIM Channel Registers

These read/write registers contain the captured counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode ($MSxB:MSxA = 0:0$), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode ($MSxB:MSxA \neq 0:0$), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

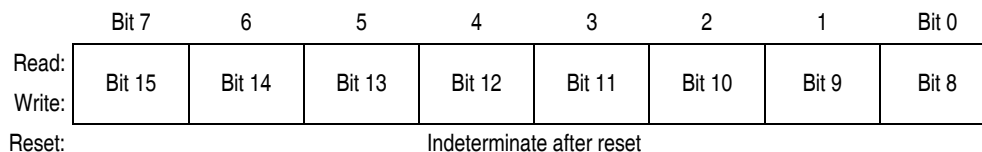


Figure 14-12. TIM Channel x Register High (TCHxH)



Figure 14-13. TIM Channel Register Low (TCHxL)

NOTE

If the reset vector is blank and monitor mode is entered, the chip will see an additional reset cycle after the initial power-on reset (POR). Once the reset vector has been programmed, the traditional method of applying a voltage, V_{TST} , to \overline{IRQ} must be used to enter monitor mode.

If monitor mode was entered as a result of the reset vector being blank, the COP is always disabled regardless of the state of \overline{IRQ} .

If the voltage applied to the \overline{IRQ} is less than V_{TST} , the MCU will come out of reset in user mode. Internal circuitry monitors the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased (\$FF). When the MCU comes out of reset, it is forced into monitor mode without requiring high voltage on the \overline{IRQ} pin. Once out of reset, the monitor code is initially executing with the internal clock at its default frequency.

If \overline{IRQ} is held high, all pins will default to regular input port functions except for PTA0 and PTA5 which will operate as a serial communication port and OSC1 input respectively (refer to [Figure 15-11](#)). That will allow the clock to be driven from an external source through OSC1 pin.

If \overline{IRQ} is held low, all pins will default to regular input port function except for PTA0 which will operate as serial communication port. Refer to [Figure 15-12](#).

Regardless of the state of the \overline{IRQ} pin, it will not function as a port input pin in monitor mode. Bit 2 of the Port A data register will always read 0. The BIH and BIL instructions will behave as if the \overline{IRQ} pin is enabled, regardless of the settings in the configuration register. See [Chapter 5 Configuration Register \(CONFIG\)](#).

The COP module is disabled in forced monitor mode. Any reset other than a power-on reset (POR) will automatically force the MCU to come back to the forced monitor mode.

15.3.1.3 Monitor Vectors

In monitor mode, the MCU uses different vectors for reset, SWI (software interrupt), and break interrupt than those for user mode. The alternate vectors are in the \$FE page instead of the \$FF page and allow code execution from the internal monitor firmware instead of user code.

NOTE

Exiting monitor mode after it has been initiated by having a blank reset vector requires a power-on reset (POR). Pulling \overline{RST} (when \overline{RST} pin available) low will not exit monitor mode in this situation.

[Table 15-2](#) summarizes the differences between user mode and monitor mode regarding vectors.

Table 15-2. Mode Difference

Modes	Functions					
	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	\$FFFE	\$FFFF	\$FFFC	\$FFFD	\$FFFC	\$FFFD
Monitor	\$FEFE	\$FEFF	\$FEFC	\$FEFD	\$FEFC	\$FEFD

16.8 3-V DC Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output high voltage $I_{Load} = -0.6$ mA, all I/O pins $I_{Load} = -4.0$ mA, all I/O pins $I_{Load} = -10.0$ mA, PTA0, PTA1, PTA3–PTA5 only	V_{OH}	$V_{DD}-0.3$ $V_{DD}-1.0$ $V_{DD}-0.8$	— — —	— — —	V
Maximum combined I_{OH} (all I/O pins)	I_{OHT}	—	—	50	mA
Output low voltage $I_{Load} = 0.5$ mA, all I/O pins $I_{Load} = 6.0$ mA, all I/O pins $I_{Load} = 10.0$ mA, PTA0, PTA1, PTA3–PTA5 only	V_{OL}	— — —	— — —	0.3 1.0 0.8	V
Maximum combined I_{OL} (all I/O pins)	I_{OHL}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V_{IL}	V_{SS}	—	$0.3 \times V_{DD}$	V
Input hysteresis ⁽³⁾	V_{HYS}	$0.06 \times V_{DD}$	—	—	V
DC injection current, all ports ⁽⁴⁾	I_{INJ}	-2	—	+2	mA
Total dc current injection (sum of all I/O) ⁽⁴⁾	I_{INJTOT}	-25	—	+25	mA
Ports Hi-Z leakage current	I_{IL}	-1	± 0.1	+1	μ A
Capacitance Ports (as input) ⁽³⁾	C_{IN}	—	—	8	pF
POR rearm voltage	V_{POR}	750	—	—	mV
POR rise time ramp rate ⁽³⁾⁽⁵⁾	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage ⁽³⁾	V_{TST}	$V_{DD} + 2.5$	—	$V_{DD} + 4.0$	V
Pullup resistors ⁽⁶⁾ PTA0–PTA5, PTB0–PTB7	R_{PU}	16	26	36	k Ω
Pulldown resistors ⁽⁷⁾ PTA0–PTA5	R_{PD}	16	26	36	k Ω
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	2.40	2.55	2.70	V
Low-voltage inhibit reset, trip rising voltage ⁽⁶⁾	V_{TRIPR}	2.475	2.625	2.775	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	75	—	mV

- $V_{DD} = 2.7$ to 3.3 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H , unless otherwise noted.
- Typical values reflect average measurements at midpoint of voltage range, 25°C only.
- Values are based on characterization results, not tested in production.
- Guaranteed by design, not tested in production.
- If minimum V_{DD} is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum V_{DD} is reached.
- R_{PU} is measured at $V_{DD} = 3.0$ V
- R_{PD} is measured at $V_{DD} = 3.0$ V, Pulldown resistors only available when KBix is enabled with KBixPOL = 1.

Chapter 17

Ordering Information and Mechanical Specifications

17.1 Introduction

This section contains order numbers for the MC68HC908QY1A, MC68HC908QY2A, MC68HC908QY4A, MC68HC908QT1A, MC68HC908QT2A, and MC69HC908QT4A. Dimensions are given for:

- 8-pin plastic dual in-line package (PDIP)
- 8-pin small outline integrated circuit (SOIC) package
- 8-pin dual flat no lead (DFN) package
- 16-pin PDIP
- 16-pin SOIC
- 16-pin thin shrink small outline package (TSSOP)

17.2 Ordering Information

Table 17-1. Consumer and Industrial Device Numbering System

Device Number	ADC	FLASH Memory	Packages ⁽¹⁾
MC908QT1A	—	1536 bytes	8-pins PDIP, SOIC, and DFN
MC908QT2A	Yes	1536 bytes	
MC908QT4A	Yes	4096 bytes	
MC908QY1A	—	1536 bytes	16-pins PDIP, SOIC, and TSSOP
MC908QY2A	Yes	1536 bytes	
MC908QY4A	Yes	4096 bytes	

1. See [Table 17-3](#) for package information.

Table 17-2. Automotive Device Numbering System

Device Number	ADC	FLASH Memory	Packages ⁽¹⁾
S908QY2A	Yes	1536 bytes	16-pins TSSOP and SOIC
S908QY4A	Yes	4096 bytes	

1. See [Table 17-3](#) for package information.



Ordering Information and Mechanical Specifications

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