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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372c8t6

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Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of µA per pin can be observed if V_{DDA} is higher than V_{DDIO}.

3.10 Direct memory access (DMA)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F37x devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either from V_{DD} supply when present or through the V_{BAT} pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28th, 29th (leap year), 30th and 31st day of the month.
- 2 programmable alarms with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.26 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F37x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
29	M3	20	14	PA4	I/O	TTa		SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1,	ADC_IN4, DAC1_OUT1
30	K4	21	15	PA5	I/O	TTa		SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2	ADC_IN5, DAC1_OUT2
31	L4	22	16	PA6	I/O	TTa		SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3	ADC_IN6, DAC2_OUT1,
32	M4	23		PA7	I/O	TTa	(1)	TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT	ADC_IN7
33	K5	24		PC4	I/O	TTa	(1)	TIM13_CH1, TSC_G3_IO1, USART1_TX	ADC_IN14
34	L5	25		PC5	I/O	TTa	(1)	TSC_G3_IO2, USART1_RX	ADC_IN15
35	M5	26	18	PB0	I/O	TTa		SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2	ADC_IN8, SDADC1_AIN6P
36	M6	27	19	PB1	I/O	TTa		TIM3_CH4, TSC_G3_IO4	ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M
37	L6	28	20	PB2	I/O	TC	(2)		SDADC1_AIN4P, SDADC2_AIN6P
38	M7			PE7	I/O	TC	(2) (1)		SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	PE8	I/O	TC	(2)		SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	PE9	I/O	TC	(2)		SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8			PE10	I/O	TC	(2) (1)		SDADC1_AIN2P
42	M9			PE11	I/O	TC	(2) (1)		SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0		TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1				USART2_CTS	COMP1_OUT			TIM19_CH1		EVENTOUT
PA1		TIM2_CH2	TIM5_CH2	TSC_G1_IO2			SPI3_SCK/I2S3_CK	USART2_RTS		TIM15_CH1N		TIM19_CH2		EVENTOUT
PA2		TIM2_CH3	TIM5_CH3	TSC_G1_IO3			SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1		TIM19_CH3		EVENTOUT
PA3		TIM2_CH4	TIM5_CH4	TSC_G1_IO4			SPI3_MOSI/I2S3_SD	USART2_RX		TIM15_CH2		TIM19_CH4		EVENTOUT
PA4			TIM3_CH2	TSC_G2_IO1		SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK			TIM12_CH1			EVENTOUT
PA5		TIM2_CH1_ETR		TSC_G2_IO2		SPI1_SCK/I2S1_CK		CEC		TIM14_CH1	TIM12_CH2			EVENTOUT
PA6		TIM16_CH1	TIM3_CH1	TSC_G2_IO3		SPI1_MISO/I2S1_MCK			COMP1_OUT	TIM13_CH1				EVENTOUT
PA7		TIM17_CH1	TIM3_CH2	TSC_G2_IO4		SPI1_MOSI/I2S1_SD			COMP2_OUT	TIM14_CH1				EVENTOUT
PA8	MCO		TIM5_CH1_ETR		I2C2_SMBA	SPI2_SCK/I2S2_CK		USART1_CK			TIM4_ETR			EVENTOUT
PA9			TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK		USART1_TX		TIM15_BKIN	TIM2_CH3			EVENTOUT
PA10		TIM17_BKIN		TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD		USART1_RX		TIM14_CH1	TIM2_CH4			EVENTOUT
PA11			TIM5_CH2			SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1		USB_DM	EVENTOUT
PA12		TIM16_CH1	TIM5_CH3				SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2		USB_DP	EVENTOUT

Table 16. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0		EVENTOUT	TIM4_ETR					USART1_TX
PE1		EVENTOUT						USART1_RX
PE2	TRACECLK	EVENTOUT		TSC_G7_IO1				
PE3	TRACED0	EVENTOUT		TSC_G7_IO2				
PE4	TRACED1	EVENTOUT		TSC_G7_IO3				
PE5	TRACED2	EVENTOUT		TSC_G7_IO4				
PE6	TRACED3	EVENTOUT						
PE7		EVENTOUT						
PE8		EVENTOUT						
PE9		EVENTOUT						
PE10		EVENTOUT						
PE11		EVENTOUT						
PE12		EVENTOUT						
PE13		EVENTOUT						
PE14		EVENTOUT						
PE15		EVENTOUT						USART3_RX

Depending on the SDADCx operation mode, there can be more constraints between V_{REFSD+}, V_{DDSD12} and V_{DDSD3} which are described in reference manual RM0313.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all VDD_x and VDDSDx power lines (source)(1)	160	mA
$I_{VSS(\Sigma)}$	Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1)	-160	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to V_{SS}). V_{DD} (VDD_x) is the external power supply for all remaining I/O pins (the I/O pin ground is internally connected to V_{SS}).
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 62*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33				
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4				

1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Data based on characterization results, not tested in production.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I_{DDA}(1)(2)	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	µA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
$I_{SDADC12}$ + I_{SDADC3}	Supply currents in Run mode from V_{DDSD12} and V_{DDSD3} (SDADCs are off)		-	2.5	1	

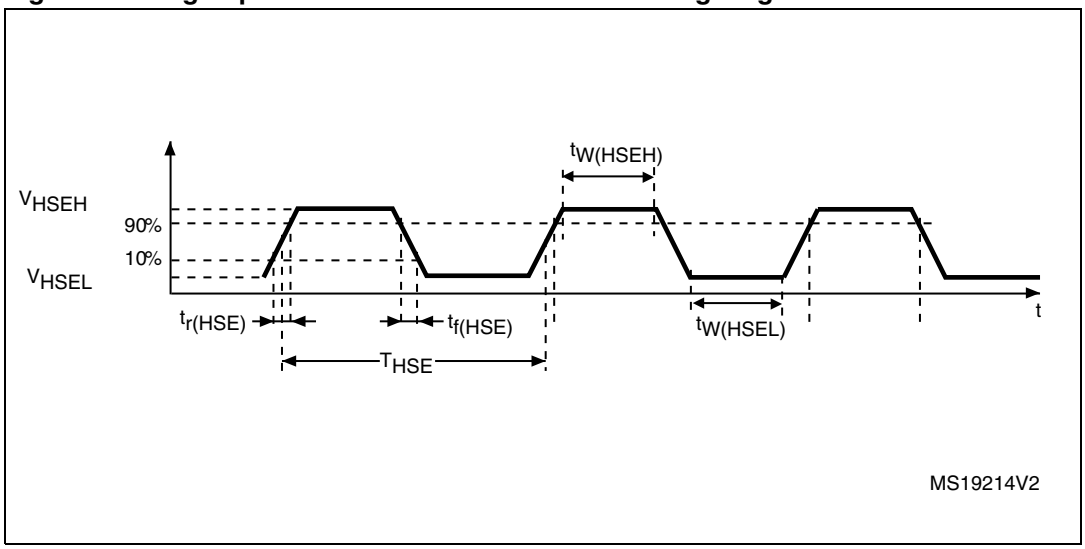
1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.
2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	42.8	6.9	mA
			64 MHz	38.2	6.2	
			48 MHz	28.9	4.8	
			32 MHz	19.5	3.4	
			24 MHz	14.7	2.7	
			16 MHz	10.2	2.0	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	5.2	1.2	
			4 MHz	3.4	1.1	
			2 MHz	2.2	0.9	
			1 MHz	1.6	0.9	
			500 kHz	1.4	0.8	
			125 kHz	1.1	0.8	
I_{DDA}(1)	Supply current in Sleep mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	242.9	241.5	µA
			64 MHz	213.7	212.7	
			48 MHz	158.8	158.0	
			32 MHz	107.6	107.3	
			24 MHz	82.7	82.6	
			16 MHz	58.3	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 39. Low-speed external user clock characteristics

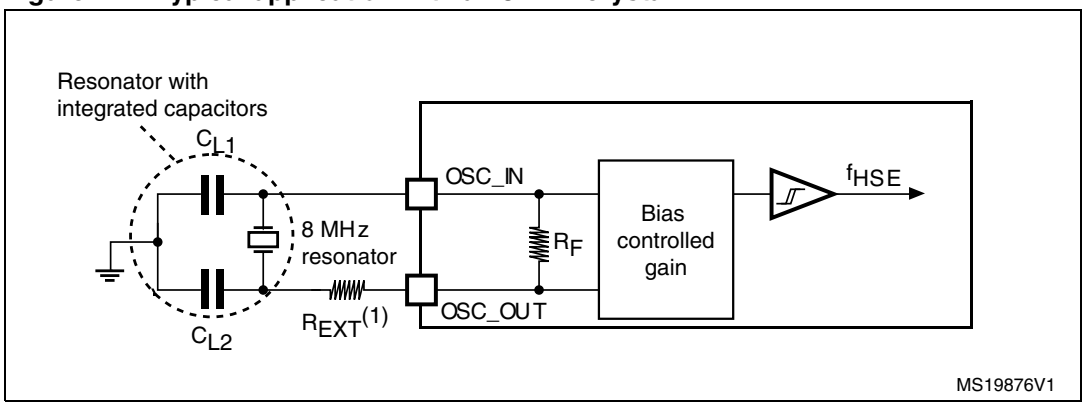
Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time				50	

1. Guaranteed by design, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability		0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability			1	
		LSEDRV[1:0] = 10 medium high driving capability			1.3	
		LSEDRV[1:0]=11 higher driving capability			1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5			µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8			
		LSEDRV[1:0] = 10 medium high driving capability	15			
		LSEDRV[1:0]=11 higher driving capability	25			
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized		2		s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

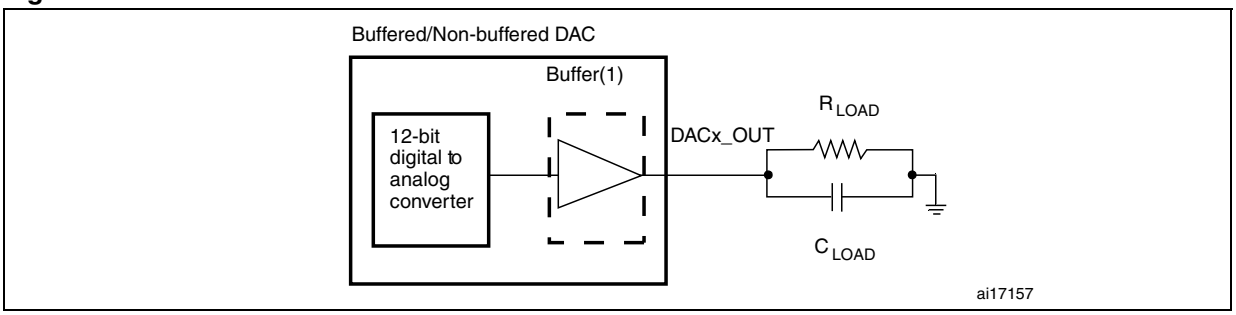
- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Table 63. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization, not tested in production.

Figure 31. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.20 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4		10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1			µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.22 Timer characteristics

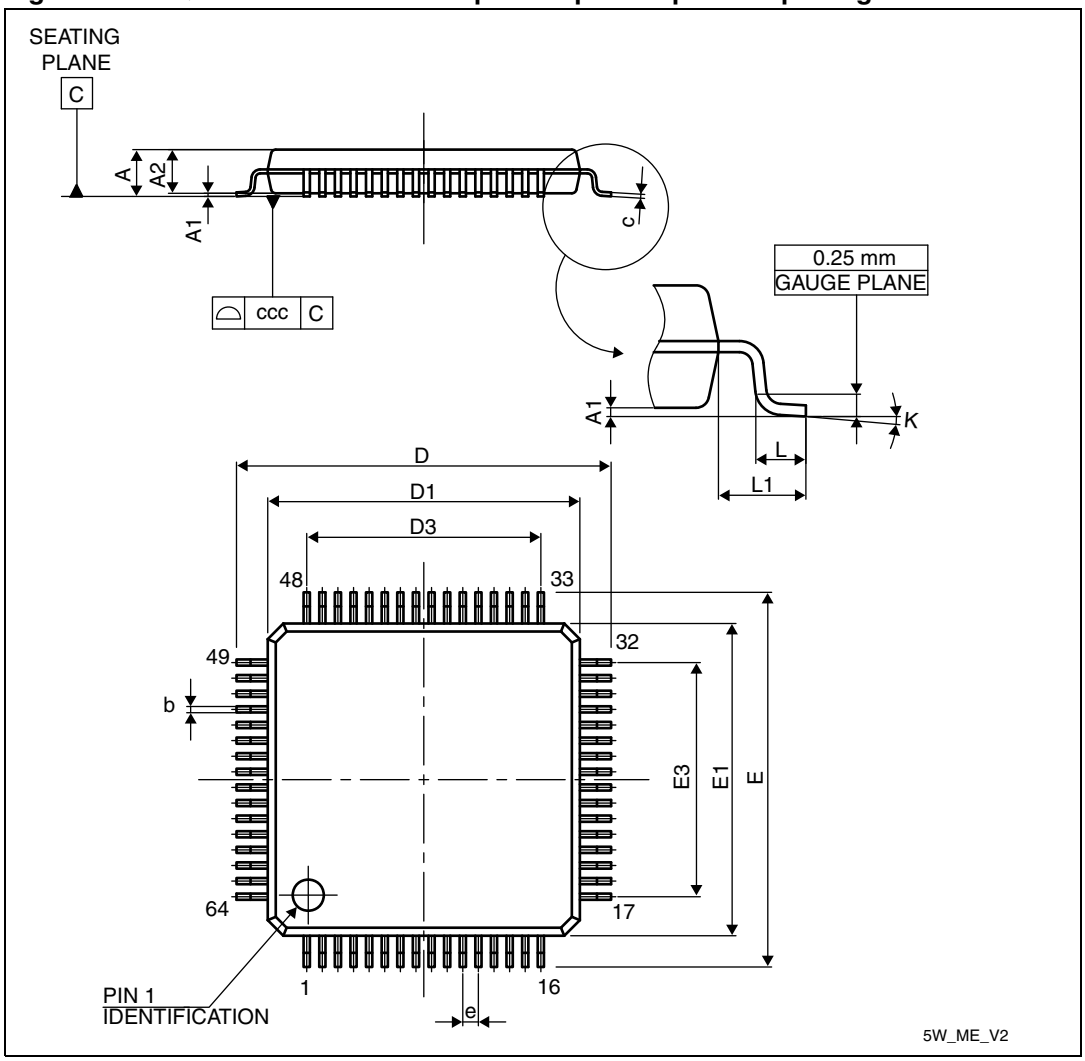
The parameters given in *Table 68* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit	Note
EL	Integral linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2			16	LSB	
					V_{REFSD+} = 3.3			14		
			gain = 8		V_{REFSD+} = 1.2			26		
					V_{REFSD+}= 3.3			14		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2			31		
					V_{REFSD+}= 3.3			23		
			gain = 8		V_{REFSD+}= 1.2			80		
					V_{REFSD+} = 3.3			35		
ED	Differential linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2			2.4	LSB	
					V_{REFSD+} = 3.3			1.8		
			gain = 8		V_{REFSD+}= 1.2			3.6		
					V_{REFSD+} = 3.3			2.9		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2			3.2		
					V_{REFSD+} = 3.3			2.8		
			gain = 8		V_{REFSD+}= 1.2			4.1		
					V_{REFSD+} = 3.3			3.3		

Figure 36. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 78. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3		7.50			0.2953	

Table 82. Document revision history

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 30: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F37x I2C implementation* Added *Table 8: STM32F37x USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F37x BGA100 pinout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F37x pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F37x pin definitions* Modified "x_CK" occurences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Table 9: Power supply scheme* Added Caution after *Table 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.2.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*