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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372cbt6

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F37x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F37x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F37x I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

Table 13. Alternate functions for port PB

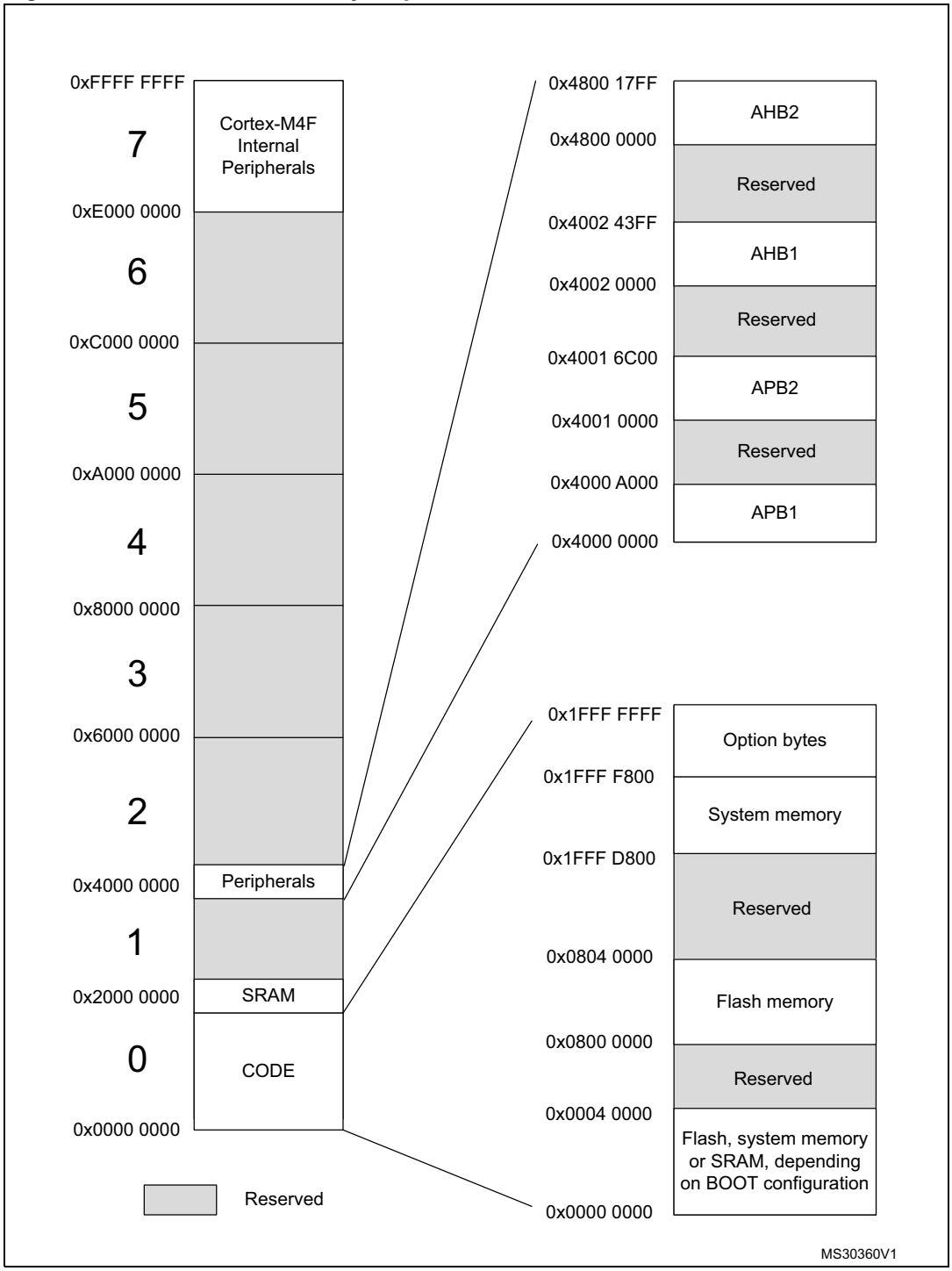
Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0			TIM3_CH3	TSC_ G3_IO3		SPI_MOSI/ I2S1_SD					TIM3_ CH2		EVENTOUT
PB1			TIM3_CH4	TSC_ G3_IO4									EVENTOUT
PB2													EVENTOUT
PB3	JTDO/ TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1		SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX		TIM13_ CH1	TIM3_ ETR		EVENTOUT
PB4	JTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2		SPI1_MISO /I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX		TIM15_ CH1N	TIM17 _BKIN		EVENTOUT
PB5		TIM16_ BKIN	TIM3_CH2		I2C1_ SMBA	SPI1_MOSI /I2S1_SD	SPI3_MOSI /I2S3_SD	USART2_CK			TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6		TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL			USART1_TX		TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7		TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA			USART1_RX		TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8		TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX		TIM19 _CH3	EVENTOUT
PB9		TIM17_ CH1	TIM4_CH4		I2C1_ SDA	SPI2_NSS/ I2S2_WS	IR-OUT	USART3_RX	COMP2 _OUT	CAN_ TX		TIM19 _CH4	EVENTOUT
PB10		TIM2_ CH3		TSC_ SYNCH		SPI2_SCK/ I2S2_CK	CEC	USART3_TX					EVENTOUT
PB14		TIM15_ CH1		TSC_ G6_IO1		SPI2_MISO /I2S2_MCK		USART3_RTS		TIM12_ CH1			EVENTOUT
PB15		TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2		SPI2_MOSI /I2S2_SD				TIM12_ CH2			EVENTOUT

Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0		EVENTOUT	TIM5_CH1_ETR					
PC1		EVENTOUT	TIM5_CH2					
PC2		EVENTOUT	TIM5_CH3			SPI2_MISO/I2S2_MCK		
PC3		EVENTOUT	TIM5_CH4			SPI2_MOSI/I2S2_SD		
PC4		EVENTOUT	TIM13_CH1	TSC_G3_IO1				USART1_TX
PC5		EVENTOUT		TSC_G3_IO2				USART1_RX
PC6		EVENTOUT	TIM3_CH1			SPI1_NSS/I2S1_WS		
PC7		EVENTOUT	TIM3_CH2			SPI1_SCK/I2S1_CK		
PC8		EVENTOUT	TIM3_CH3			SPI1_MISO/I2S1_MCK		
PC9		EVENTOUT	TIM3_CH4			SPI1_MOSI/I2S1_SD		
PC10		EVENTOUT	TIM19_CH1				SPI3_SCK/I2S3_CK	USART3_TX
PC11		EVENTOUT	TIM19_CH2				SPI3_MISO/I2S3_MCK	USART3_RX
PC12		EVENTOUT	TIM19_CH3				SPI3_MOSI/I2S3_SD	USART3_CK
PC13								
PC14								
PC15								

5 Memory mapping

Figure 6. STM32F37x memory map



6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	72	
V_{DD}	Standard operating voltage	Must have a potential equal to or lower than V_{DDA}	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC and DAC used)	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
	Analog operating voltage (ADC and DAC not used)		2	3.6	
V_{DDSD12}	VDDSD12 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD12 operating voltage (SDADC not used)		2.0	3.6	
V_{DDSD3}	VDDSD3 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD3 operating voltage (SDADC not used)		2.0	3.6	
V_{BAT}	Backup operating voltage		1.65	3.6	V
V_{IN}	Input voltage on FT and FTf pins(2)		- 0.3	5.5	V
	Input voltage on TTa pins		- 0.3	V_{DDA} + 0.3	
	Input voltage on TC pins on SDADCx channels inputs(3)		- 0.3	V_{DDSDx} + 0.3	
	Input voltage on BOOT0 pin		0	5.5	
	Input voltage on any other pin		- 0.3	V_{DD} + 0.3	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP100		434	mW
		LQFP64		444	
		LQFP48		364	
		BGA100		338	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(5)	–40	125	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability		0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability			1	
		LSEDRV[1:0] = 10 medium high driving capability			1.3	
		LSEDRV[1:0]=11 higher driving capability			1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5			µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8			
		LSEDRV[1:0] = 10 medium high driving capability	15			
		LSEDRV[1:0]=11 higher driving capability	25			
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized		2		s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	9	dBµV
			30 to 130 MHz	26	
			130 MHz to 1 GHz	30	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101, LQFP100, LQFP64, LQFP48 and BGA100 packages	II	500	
		T_A = +25 °C, conforming to JESD22-C101, WLCSP66 package	II	250	

1. Data based on characterization results, not tested in production.

6.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 56*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I^2C characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		0.26		µs
$t_{su(SDA)}$	SDA setup time	250		100		50		ns
$t_{h(SDA)}$	SDA data hold time	0(2)	3450(3)	0(2)	900(3)	0(4)	450(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300		120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300		120	ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		0.26		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		0.26		µs
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		0.26		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		0.5		µs
C_b	Capacitive load for each bus line		400		400		550	pF

1. The I^2C characteristics are the requirements from I^2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.
2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 120ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

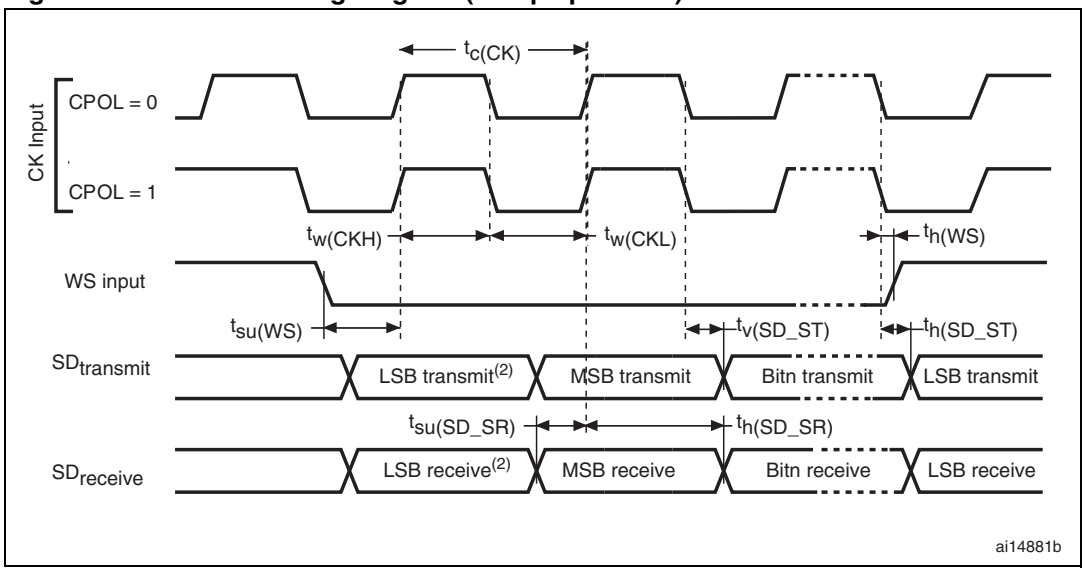
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$ (1)	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$ (1)	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	2Tpclk		ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	4Tpclk		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5.5		
		Slave mode	6.5		
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5		
$t_{h(SI)}$ (1)		Slave mode	5		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		39	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4		

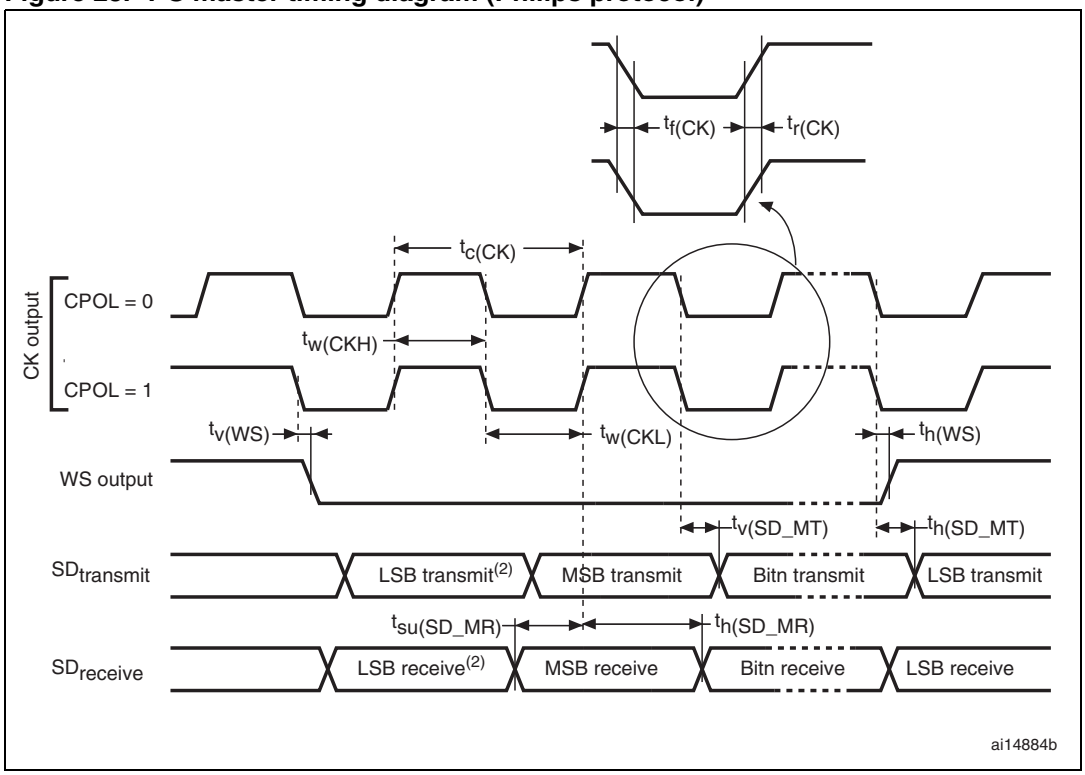
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 27. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 28. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{SRC}(2)	Signal source impedance	See *Equation 1* and *Table 61* for details			50	kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					2(3)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(3)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2		V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)		0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

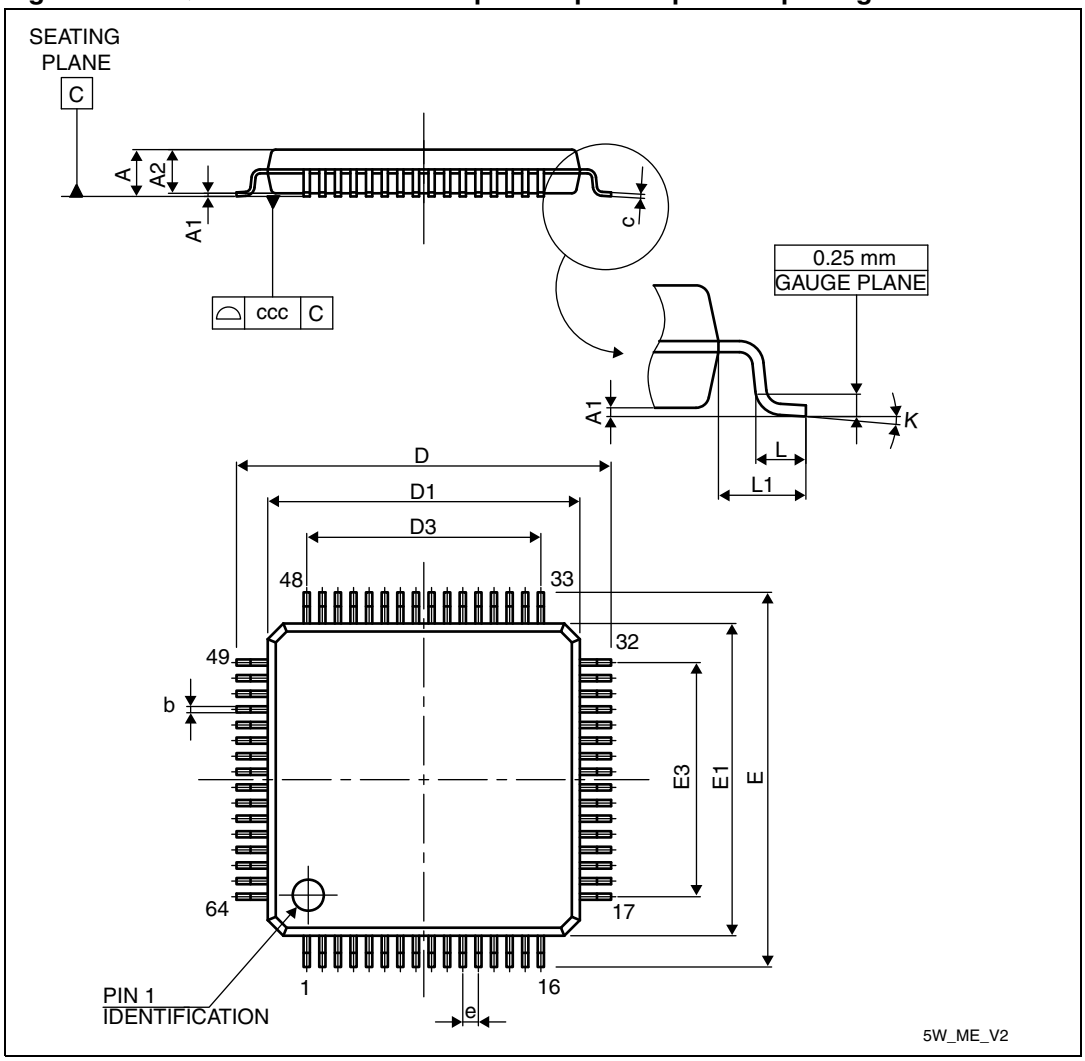
1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SINAD (4)	Signal to noise and distortion ratio	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	76	77		dB	ENOB = SINAD/6.02 -0.292
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	75	76			
						V_{REFSD+} = 3.3	76	77			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	70	74			
						V_{REFSD+} = 3.3	79	85			
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)	75	81			
		Single ended mode	gain =1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	72	73			
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	68	71			
						V_{REFSD+} = 3.3	72	73			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	60	64			
						V_{REF} = 3.3	67	72			
THD(4)	Total harmonic distortion	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)		-77	-76	dB	
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-77	-76		
						V_{REFSD+} = 3.3		-77	-76		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-85	-70		
						V_{REFSD+} = 3.3		-93	-80		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)		-93	-83		
		Single ended mode	gain =1	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-72	-68		
						V_{REFSD+} = 3.3		-74	-72		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-66	-61		
						V_{REFSD+} = 3.3		-75	-70		

1. Data based on characterization results, not tested in production.

Figure 36. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 78. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

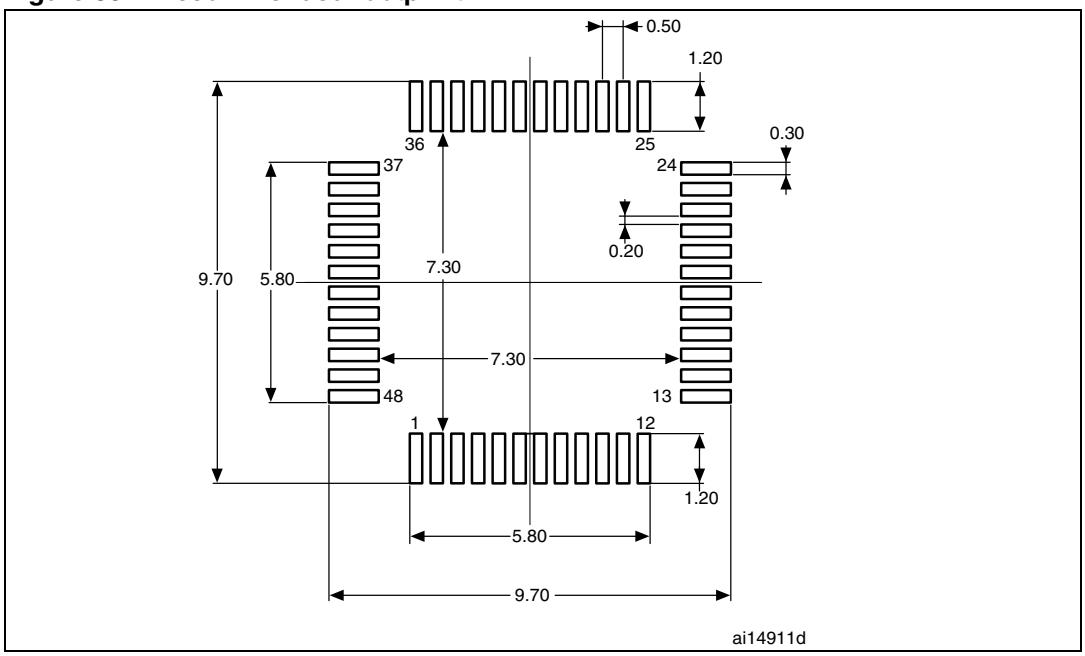
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3		7.50			0.2953	

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
K	0°	3.5°	7°	0°	3.5°	7°
ccc			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. Recommended footprint



1. Dimensions are in millimeters.

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F37x at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 175+ 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 236.6 mW) = 82 °C + 10.65 °C = 92.65 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 81. Ordering information scheme

Example: STM32 F 372 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

372 = STM32F372xx

373 = STM32F373xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Code size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and real

Table 82. Document revision history

Date	Revision	Changes
21-Dec-2012	3	Updated *Table 2: Device overview*, capacitive sensing channels peripheral added. Updated *Table 3: Capacitive sensing GPIOs available on STM32F37x devices* Updated *Section 3.19: Inter-integrated circuit interface (I2C)* Updated the function names in *Table 11: STM32F37x pin definitions* Updated *Table 20: Current characteristics* Updated *Table 22: General operating conditions* Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Updated *Table 32: Typical and maximum current consumption from VBAT supply* Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')* Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 35: Switching output I/O current consumption* Added *Table 36: Peripheral current consumption* *Figure 16: HSI oscillator accuracy characterization results* Updated *Section 6.3.6: Wakeup time from low-power mode* Updated *Table 37: Low-power mode wakeup timings* Updated *Table 47: EMS characteristics* Updated *Table 51: I/O current injection susceptibility* Updated *Table 52: I/O static characteristics* Updated *Figure 17: TC and TTa I/O input characteristics - CMOS port*, *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 19: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port* Updated *Table 53: Output voltage characteristics* Updated *Table 55: NRST pin characteristics* Updated *Table 54: I/O AC characteristics* Updated *Table 63: DAC characteristics* Updated *Table 74: SDADC characteristics* Updated *Figure 7: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 9: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 11: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline* Updated *Table 21: LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 22: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 23: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* Added *Figure 16: HSI oscillator accuracy characterization results*