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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372cct6

List of tables

3.7.4 Low-power modes

The STM32F37x supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC, the USB wakeup, and the RTC alarm.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Digital-to-analog converter (DAC)

The devices feature up to two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Up to two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- triangular-wave generation
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

3.15 Fast comparators (COMP)

The STM32F37x embeds up to 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage (V_{REFINT}) or submultiple (1/4 V_{REFINT}, 1/2 V_{REFINT} and 3/4 V_{REFINT})

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F37x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 9* for the features between SPI1 and SPI2.

Table 9. STM32F37x SPI/I2S implementation

SPI features[1]	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Universal serial bus (USB)

The STM32F37x embeds an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Figure 5. STM32F37x BGA100 pinout

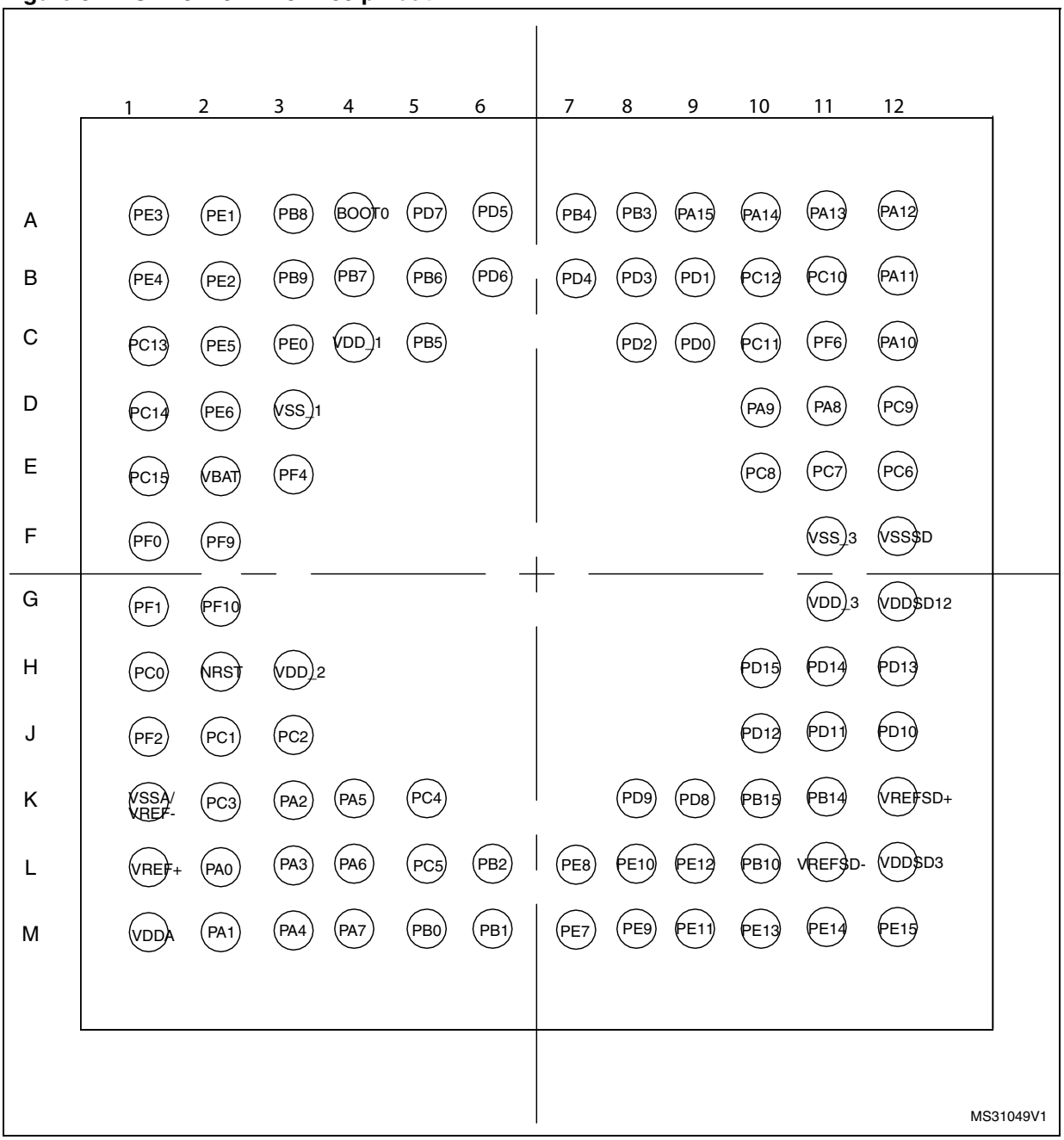


Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
11	G2			PF10	I/O	FT	(1)		
12	F1	5	5	PF0 - OSC_IN	I/O	FTf		I2C2_SDA	OSC_IN
13	G1	6	6	PF1 - OSC_OUT	I/O	FTf		I2C2_SCL	OSC_OUT
14	H2	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
15	H1	8		PC0	I/O	TTa	(1)	TIM5_CH1_ETR	ADC_IN10
16	J2	9		PC1	I/O	TTa	(1)	TIM5_CH2	ADCIN11
17	J3	10		PC2	I/O	TTa	(1)	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11		PC3	I/O	TTa	(1)	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1			PF2	I/O	FT	(1)	I2C2_SMBA	
20	K1	12	8	VSSA/VREF-	S			Analog ground	
			9	VDDA/VREF+	S		(1)	Analog power supply / Reference voltage for ADC, COMP, DAC	
21	M1	13		VDDA	S		(1)	Analog power supply	
22	L1	17		VREF+	S		(1)	Reference voltage for ADC, COMP, DAC	
23	L2	14	10	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT	RTC_ TAMPER2, WKUP1, ADC_IN0, COMP1_INM
24	M2	15	11	PA1	I/O	TTa		SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2,	ADC_IN1, COMP1_INP, RTC_REF_CLK_IN
25	K3	16	12	PA2	I/O	TTa		COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3	ADC_IN2, COMP2_INM
26	L3	18	13	PA3	I/O	TTa		SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4	ADC_IN3, COMP2_INP
27	E3			PF4	I/O	FT	(1)		
28	H3	19	17	VDD_2	S			Digital power supply	

Table 11. STM32F37x pin definitions (continued)

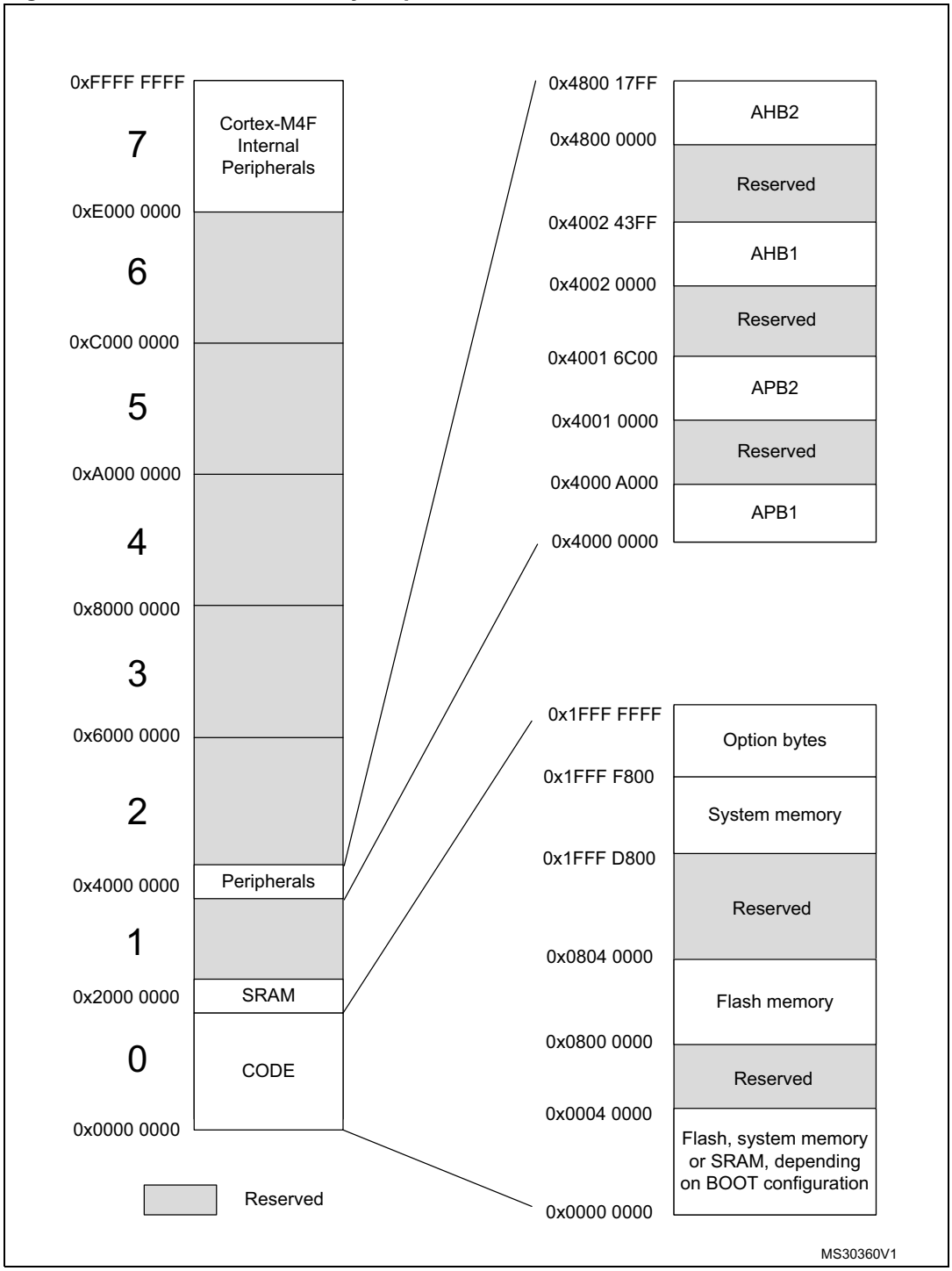
Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
60	H12			PD13	I/O	TC	(3) (1)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11			PD14	I/O	TC	(3) (1)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10			PD15	I/O	TC	(3) (1)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37		PC6	I/O	FT	(1)	TIM3_CH1, SPI1_NSS/I2S1_WS	
64	E11	38		PC7	I/O	FT	(1)	TIM3_CH2, SPI1_SCK/I2S1_CK,	
65	E10	39		PC8	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, TIM3_CH3	
66	D12	40		PC9	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, TIM3_CH4	
67	D11	41	29	PA8	I/O	FT		SPI2_SCK/I2S2_CK, I2C2_SMBA, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, MCO	
68	D10	42	30	PA9	I/O	FTf		SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1	
69	C12	43	31	PA10	I/O	FTf		SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2	
70	B12	44	32	PA11	I/O	FT		SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, USB_DM, TIM5_CH2, COMP1_OUT	
71	A12	45	33	PA12	I/O	FT		SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, USB_DP, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT	
72	A11	46	34	PA13	I/O	FT		SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, TSC_G4_IO3, SWDIO-JTMS	

Table 13. Alternate functions for port PB

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0			TIM3_CH3	TSC_ G3_IO3		SPI_MOSI/ I2S1_SD					TIM3_ CH2		EVENTOUT
PB1			TIM3_CH4	TSC_ G3_IO4									EVENTOUT
PB2													EVENTOUT
PB3	JTDO/ TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1		SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX		TIM13_ CH1	TIM3_ ETR		EVENTOUT
PB4	JTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2		SPI1_MISO /I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX		TIM15_ CH1N	TIM17 _BKIN		EVENTOUT
PB5		TIM16_ BKIN	TIM3_CH2		I2C1_ SMBA	SPI1_MOSI /I2S1_SD	SPI3_MOSI /I2S3_SD	USART2_CK			TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6		TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL			USART1_TX		TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7		TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA			USART1_RX		TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8		TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX		TIM19 _CH3	EVENTOUT
PB9		TIM17_ CH1	TIM4_CH4		I2C1_ SDA	SPI2_NSS/ I2S2_WS	IR-OUT	USART3_RX	COMP2 _OUT	CAN_ TX		TIM19 _CH4	EVENTOUT
PB10		TIM2_ CH3		TSC_ SYNCH		SPI2_SCK/ I2S2_CK	CEC	USART3_TX					EVENTOUT
PB14		TIM15_ CH1		TSC_ G6_IO1		SPI2_MISO /I2S2_MCK		USART3_RTS		TIM12_ CH1			EVENTOUT
PB15		TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2		SPI2_MOSI /I2S2_SD				TIM12_ CH2			EVENTOUT

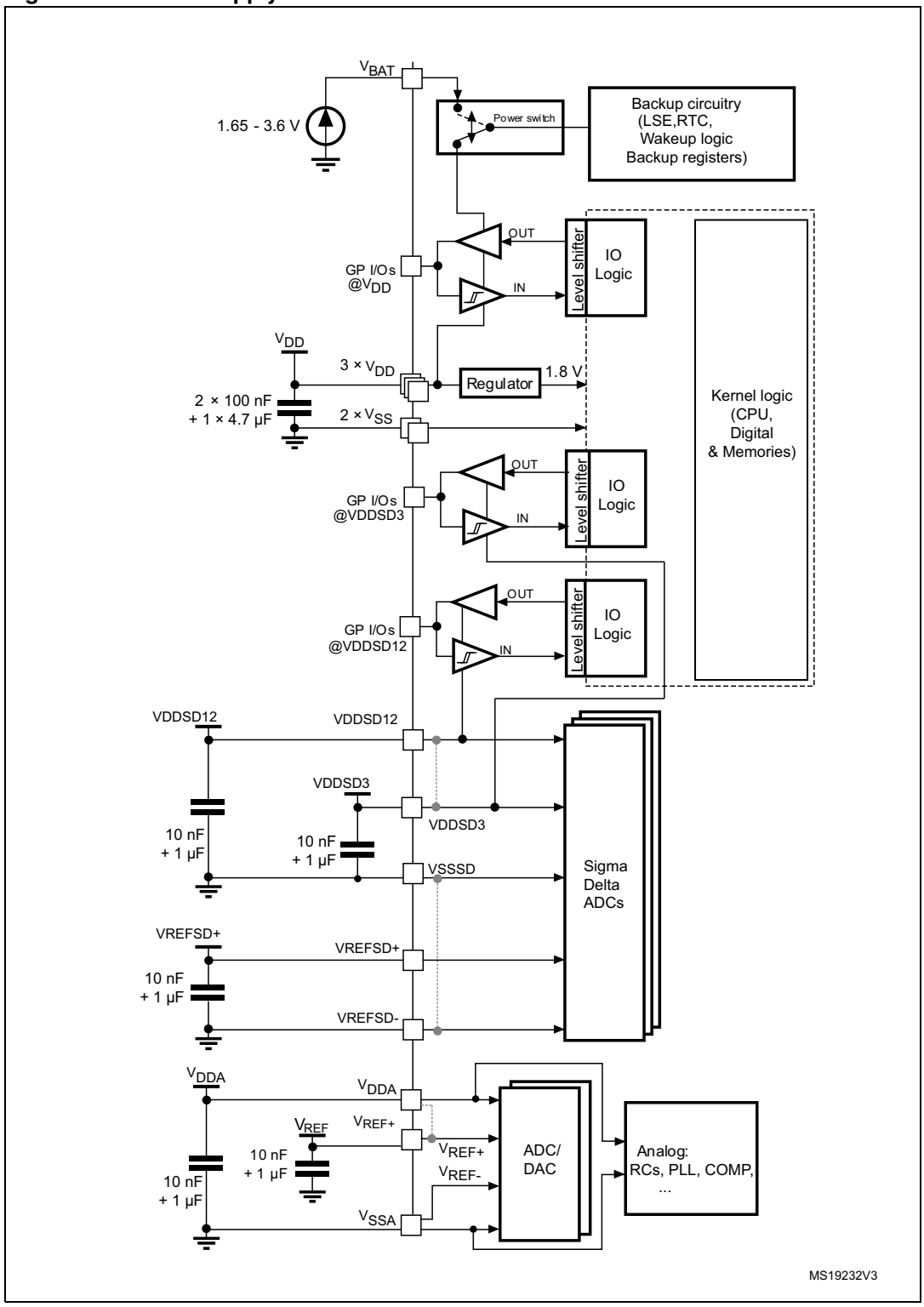
5 Memory mapping

Figure 6. STM32F37x memory map



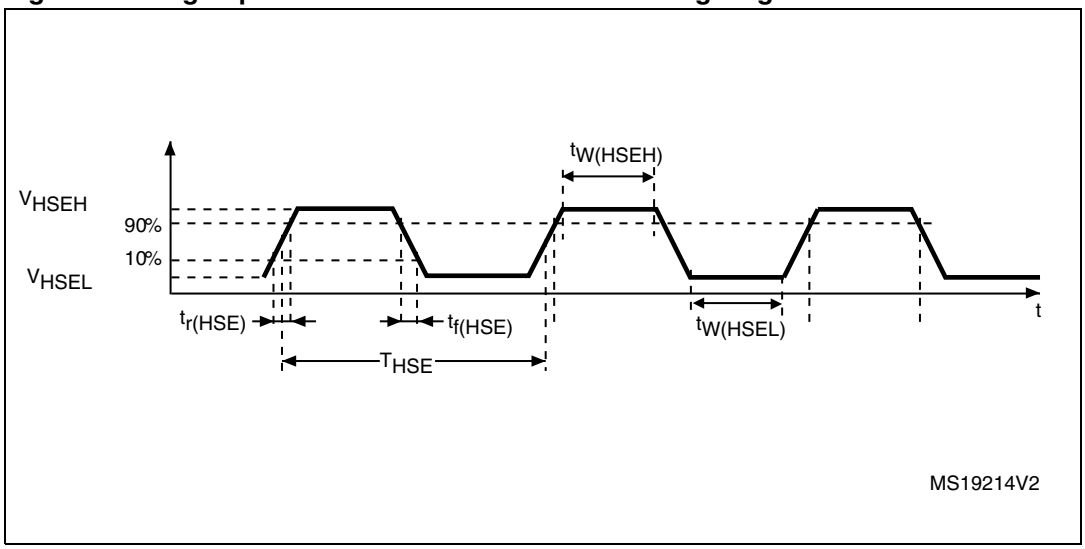
6.1.6 Power supply scheme

Figure 9. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time				50	

1. Guaranteed by design, not tested in production.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	9	dBµV
			30 to 130 MHz	26	
			130 MHz to 1 GHz	30	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101, LQFP100, LQFP64, LQFP48 and BGA100 packages	II	500	
		T_A = +25 °C, conforming to JESD22-C101, WLCSP66 package	II	250	

1. Data based on characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 21* and *Table 54*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 54. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)	CL = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time			12	ns
	$t_{r(IO)out}$	Output low to high level rise time			34	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0313 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 21*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F37xx and STM32F38xx reference manual RM0313 for a description of FM+ I/O mode configuration

Figure 24. SPI timing diagram - slave mode and CPHA = 0

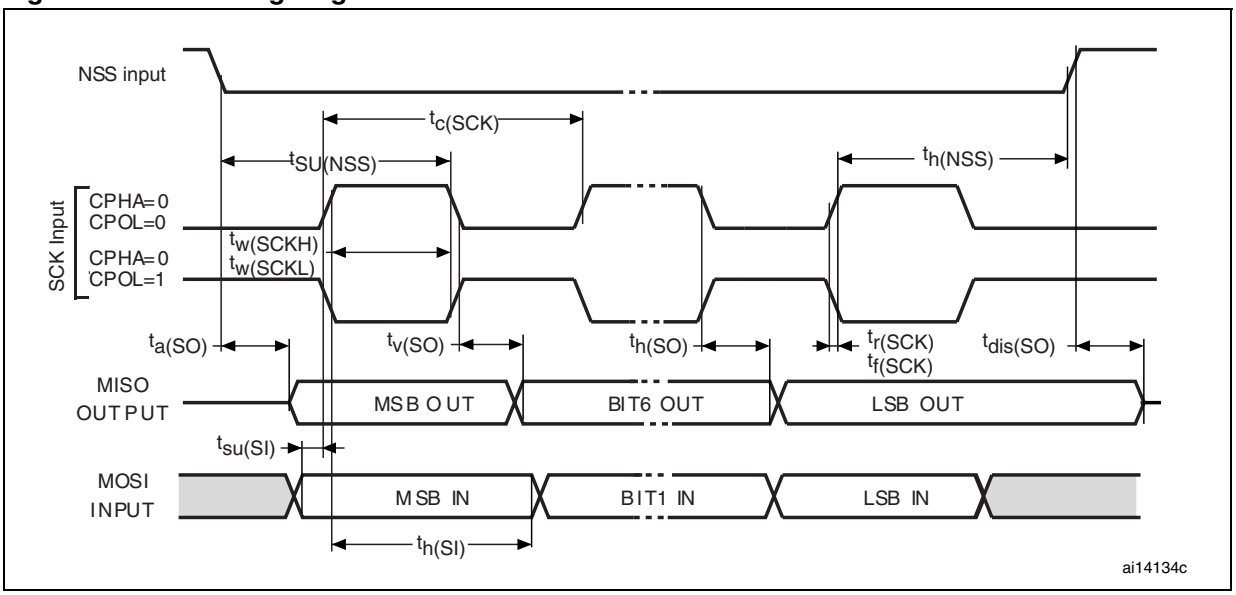
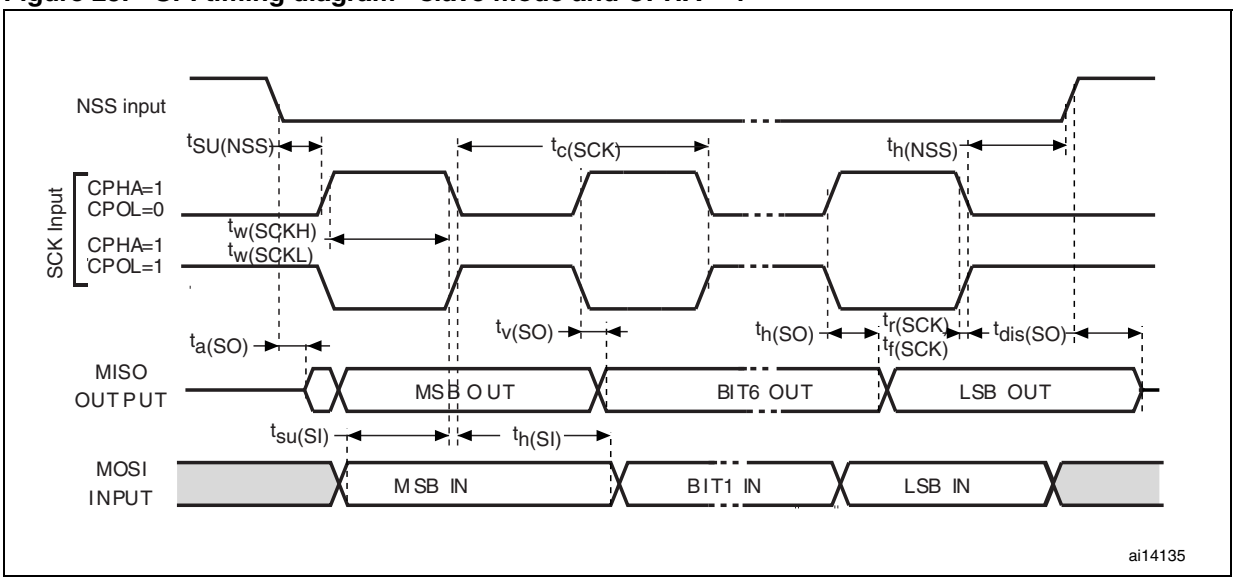


Figure 25. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
I_{DDSDx}	Supply current (V_{DDSDx} = 3.3 V)	Fast mode (f_{ADC} = 6 MHz)		800	1200	µA	
		Slow mode (f_{ADC} = 1.5 MHz)			600		
		Standby			200		
		Power down			2.5		
		SD_ADC off			1		
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{SSA}		V_{REFSD+} /gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{SSA}		V_{REFSD+} /gain/2		
		Differential mode	V_{SSA}		V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	$-V_{REFSD+}$/ gain/2		V_{REFSD+}/ gain/2		Differential voltage between AINP and AINN
f_S	Sampling rate	Slow mode (f_{ADC} = 1.5 MHz)		4.166		kHz	f_{ADC}/360
		Slow mode one channel only (f_{ADC} = 1.5 MHz)		12.5			f_{ADC}/120
		Fast mode multiplexed channel (f_{ADC} = 6 MHz)		16.66			f_{ADC}/360
		Fast mode one channel only (f_{ADC} = 6 MHz)		50			f_{ADC}/120
t_{CONV}	Conversion time			1/fs		s	
Rain	Analog input impedance	One channel, gain = 0.5, f_{ADC} = 1.5 MHz		540		kΩ	see reference manual for detailed description
		One channel, gain = 0.5, f_{ADC} = 6 MHz		135			
		One channel, gain = 8, f_{ADC} = 6 MHz		47			
t_{CALIB}	Calibration time	f_{ADC} = 6 MHz, one offset calibration		5120		µs	30720/f_{ADC}
t_{STAB}	Stabilization time	From power down f_{ADC} = 6 MHz		100		µs	600/f_{ADC}, 75/f_{ADC} if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	f_{ADC} = 6 MHz		50		µs	300/f_{ADC}
		f_{ADC} = 1.5 MHz		50			75/f_{ADC} if SLOWCK = 1

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SINAD (4)	Signal to noise and distortion ratio	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	76	77		dB	ENOB = SINAD/6.02 -0.292
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	75	76			
						V_{REFSD+} = 3.3	76	77			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	70	74			
						V_{REFSD+} = 3.3	79	85			
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)	75	81			
		Single ended mode	gain =1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	72	73			
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	68	71			
						V_{REFSD+} = 3.3	72	73			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	60	64			
						V_{REF} = 3.3	67	72			
THD(4)	Total harmonic distortion	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)		-77	-76	dB	
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-77	-76		
						V_{REFSD+} = 3.3		-77	-76		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-85	-70		
						V_{REFSD+} = 3.3		-93	-80		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)		-93	-83		
		Single ended mode	gain =1	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-72	-68		
						V_{REFSD+} = 3.3		-74	-72		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-66	-61		
						V_{REFSD+} = 3.3		-75	-70		

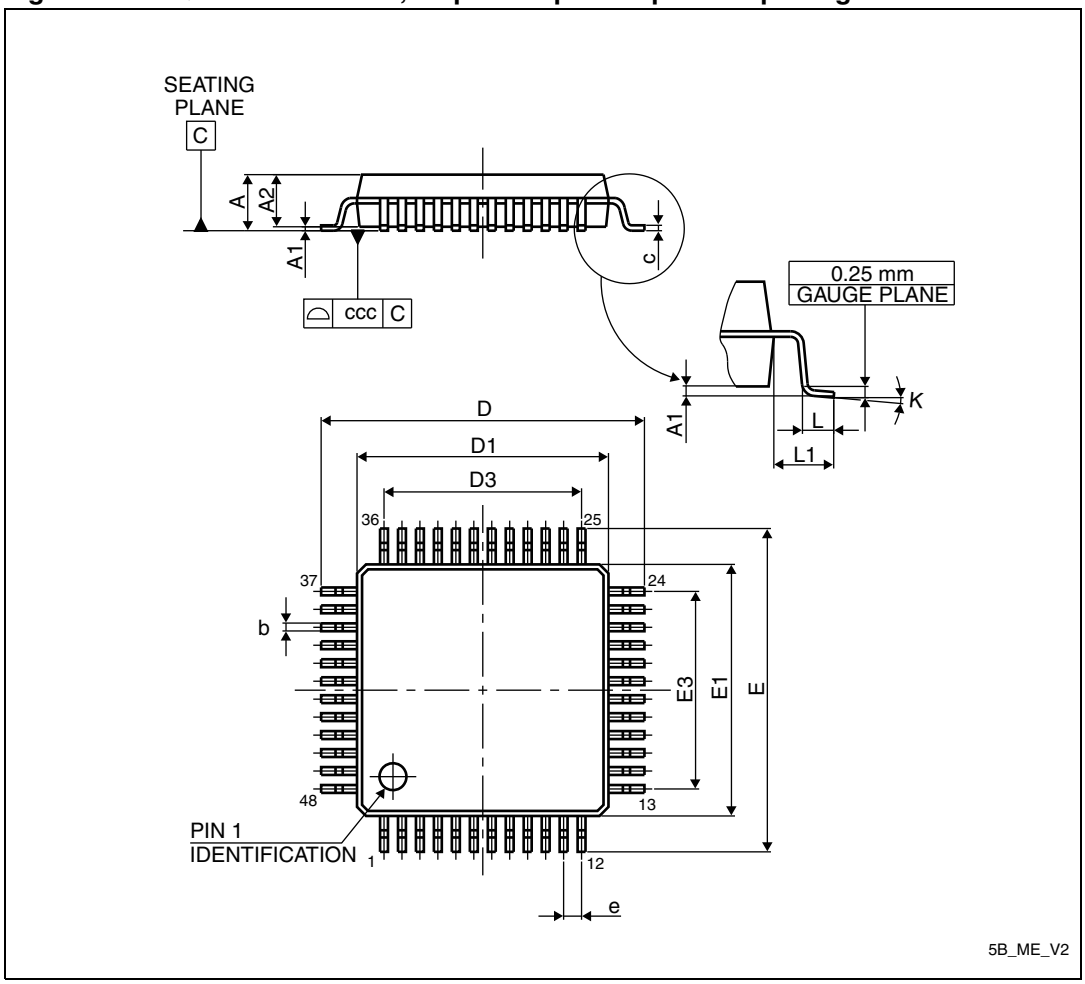
1. Data based on characterization results, not tested in production.

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 38. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3		5.50			0.2165	
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3		5.50			0.2165	