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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

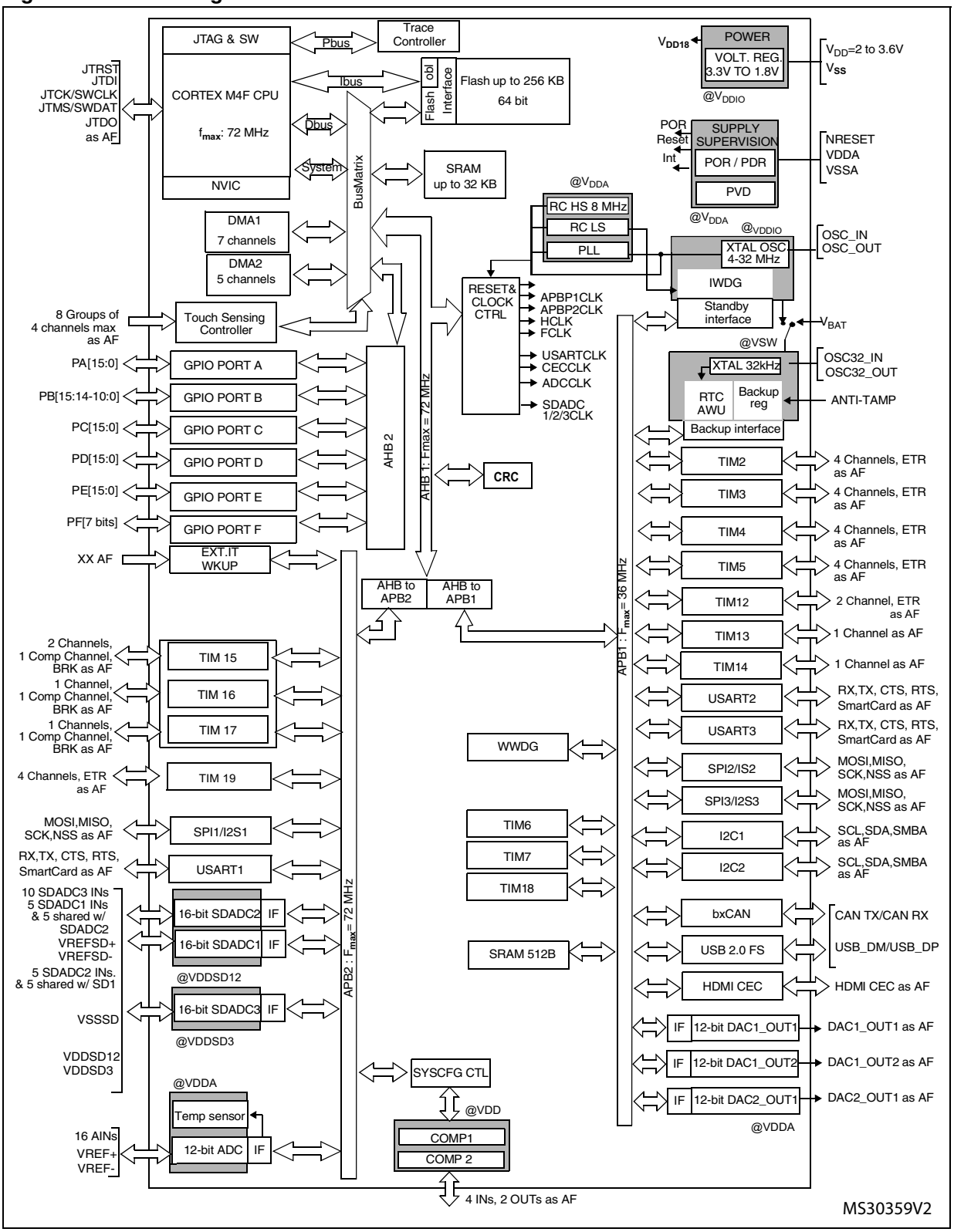
Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372r8t6

Table 2. Device overview

Peripheral		STM32F 372Cx			STM32F 372Rx			STM32F 372Vx			STM32F 373Cx			STM32F 373Rx			STM32F 373Vx		
Flash (Kbytes)		64	128	256	64	128	256	64	128	256	64	128	256	64	128	256	64	128	256
SRAM (Kbytes)		16	24	32	16	24	32	16	24	32	16	24	32	16	24	32	16	24	32
Timers	General purpose	9 (16-bit) 2 (32 bit)									9 (16-bit) 2 (32 bit)								
	Basic	3 (16-bit)									3 (16-bit)								
Comm. interfaces	SPI/I2S	3									3								
	I^2C	2									2								
	USART	3									3								
	CAN	1									1								
	USB	1									1								
GPIOs	Normal I/Os (TC, TTa)	36			52			84			36			52			84		
	5 volts Tolerant I/Os (FT, Ftf)	20			28			45			20			28			45		
12-bit ADCs		1									1								
16-bit ADCs Sigma- Delta		1 (SDADC1)									3								
12-bit DACs outputs		1 (DAC2)									3								
Analog comparator		1 (COMP1)									2								
Capacitive sensing channels		14			17			24			14			17			24		
Max. CPU frequency		72 MHz									72 MHz								
Main operating voltage		2.0 to 3.6 V									2.0 to 3.6 V								
16-bit SDADC operating voltage		2.2 to 3.6 V									2.2 to 3.6 V								
Operating temperature		Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 125 °C									Ambient operating temperature: −40 to 85 °C / −40 to 105 °C Junction temperature: −40 to 125 °C								
Packages		LQFP48			LQFP64			LQFP100, UFBGA100(1)			LQFP48			LQFP64			LQFP100, UFBGA100(1)		

1. UFBGA100 package available on 256-KB versions only.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.
2. Example given for STM32F373xx device.

3.3 Embedded Flash memory

All STM32F37x devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F37x devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
29	M3	20	14	PA4	I/O	TTa		SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1,	ADC_IN4, DAC1_OUT1
30	K4	21	15	PA5	I/O	TTa		SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2	ADC_IN5, DAC1_OUT2
31	L4	22	16	PA6	I/O	TTa		SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3	ADC_IN6, DAC2_OUT1,
32	M4	23		PA7	I/O	TTa	(1)	TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT	ADC_IN7
33	K5	24		PC4	I/O	TTa	(1)	TIM13_CH1, TSC_G3_IO1, USART1_TX	ADC_IN14
34	L5	25		PC5	I/O	TTa	(1)	TSC_G3_IO2, USART1_RX	ADC_IN15
35	M5	26	18	PB0	I/O	TTa		SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2	ADC_IN8, SDADC1_AIN6P
36	M6	27	19	PB1	I/O	TTa		TIM3_CH4, TSC_G3_IO4	ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M
37	L6	28	20	PB2	I/O	TC	(2)		SDADC1_AIN4P, SDADC2_AIN6P
38	M7			PE7	I/O	TC	(2) (1)		SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	PE8	I/O	TC	(2)		SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	PE9	I/O	TC	(2)		SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8			PE10	I/O	TC	(2) (1)		SDADC1_AIN2P
42	M9			PE11	I/O	TC	(2) (1)		SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
90	A7	56	40	PB4	I/O	FT		SPI1_MISO/I2S1_MCK, SPI3_MISO/I2S3_MCK, USART2_RX, TIM16_CH1, TIM3_CH1, TIM17_BKIN, TIM15_CH1N, TSC_G5_IO2, JNTRST	
91	C5	57	41	PB5	I/O	FT		SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAI, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR	
92	B5	58	42	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3	
93	B4	59	43	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	
94	A4	60	44	BOOT0	I	B		Boot memory selection	
95	A3	61	45	PB8	I/O	FTf		SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	
96	B3	62	46	PB9	I/O	FTf		SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	
97	C3			PE0	I/O	FT	(1)	USART1_TX, TIM4_ETR	
98	A2			PE1	I/O	FT	(1)	USART1_RX	
99	D3	63	47	VSS_1	S			Ground	
100	C4	64	48	VDD_1	S			Digital power supply	

1. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. these pins are powered by VDDSD12.
3. these pins are powered by VDDSD3.

Table 13. Alternate functions for port PB

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0			TIM3_CH3	TSC_ G3_IO3		SPI_MOSI/ I2S1_SD					TIM3_ CH2		EVENTOUT
PB1			TIM3_CH4	TSC_ G3_IO4									EVENTOUT
PB2													EVENTOUT
PB3	JTDO/ TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1		SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX		TIM13_ CH1	TIM3_ ETR		EVENTOUT
PB4	JTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2		SPI1_MISO /I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX		TIM15_ CH1N	TIM17 _BKIN		EVENTOUT
PB5		TIM16_ BKIN	TIM3_CH2		I2C1_ SMBA	SPI1_MOSI /I2S1_SD	SPI3_MOSI /I2S3_SD	USART2_CK			TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6		TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL			USART1_TX		TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7		TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA			USART1_RX		TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8		TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX		TIM19 _CH3	EVENTOUT
PB9		TIM17_ CH1	TIM4_CH4		I2C1_ SDA	SPI2_NSS/ I2S2_WS	IR-OUT	USART3_RX	COMP2 _OUT	CAN_ TX		TIM19 _CH4	EVENTOUT
PB10		TIM2_ CH3		TSC_ SYNCH		SPI2_SCK/ I2S2_CK	CEC	USART3_TX					EVENTOUT
PB14		TIM15_ CH1		TSC_ G6_IO1		SPI2_MISO /I2S2_MCK		USART3_RTS		TIM12_ CH1			EVENTOUT
PB15		TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2		SPI2_MOSI /I2S2_SD				TIM12_ CH2			EVENTOUT

Table 16. Alternate functions for port PE

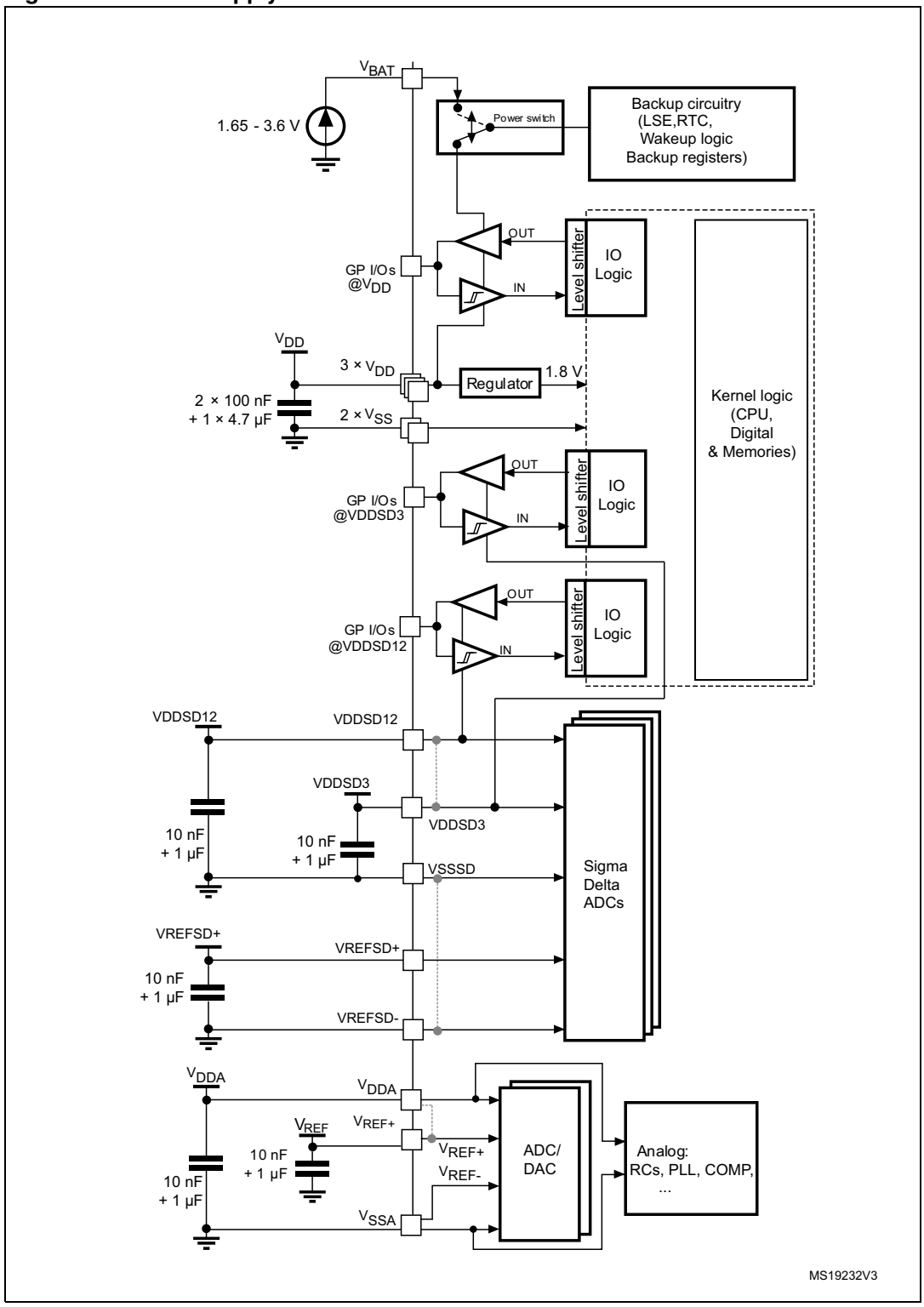
Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0		EVENTOUT	TIM4_ETR					USART1_TX
PE1		EVENTOUT						USART1_RX
PE2	TRACECLK	EVENTOUT		TSC_G7_IO1				
PE3	TRACED0	EVENTOUT		TSC_G7_IO2				
PE4	TRACED1	EVENTOUT		TSC_G7_IO3				
PE5	TRACED2	EVENTOUT		TSC_G7_IO4				
PE6	TRACED3	EVENTOUT						
PE7		EVENTOUT						
PE8		EVENTOUT						
PE9		EVENTOUT						
PE10		EVENTOUT						
PE11		EVENTOUT						
PE12		EVENTOUT						
PE13		EVENTOUT						
PE14		EVENTOUT						
PE15		EVENTOUT						USART3_RX

Table 18. STM32F37x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800- 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
	0x4001 6C00 - 0x4001 FFFF	37 KB	Reserved

6.1.6 Power supply scheme

Figure 9. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Table 35. Switching output I/O current consumption

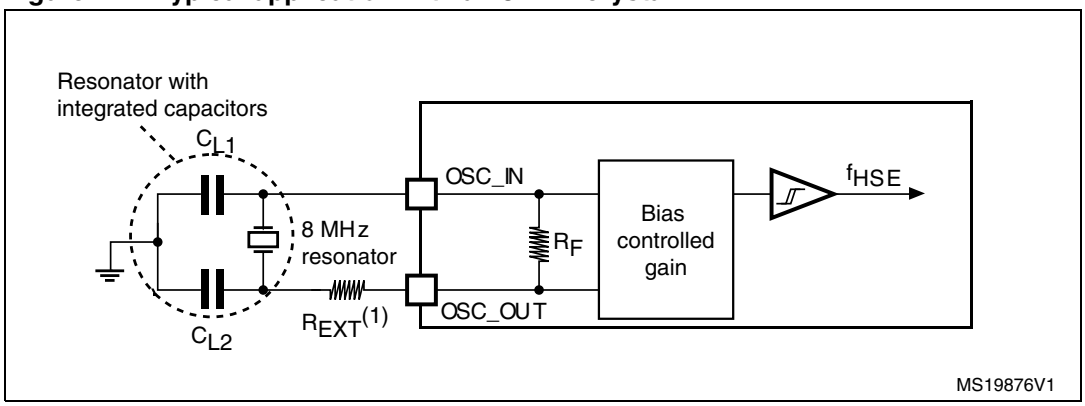
Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.77	mA
			4 MHz	0.87	
			8 MHz	0.95	
			18 MHz	1.59	
			36 MHz	2.57	
			48 MHz	3.11	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + CS$	2 MHz	0.96	
			4 MHz	1.0	
			8 MHz	1.08	
			18 MHz	2.17	
			36 MHz	3.42	
			48 MHz	5.50	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + CS$	2 MHz	0.98	
			4 MHz	1.23	
			8 MHz	1.48	
			18 MHz	2.93	
			36 MHz	6.59	
			48 MHz	7.03	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	mA
			4 MHz	1.3	
			8 MHz	1.81	
			18 MHz	3.42	
			36 MHz	8.27	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.09	
			4 MHz	1.55	
			8 MHz	2.18	
			18 MHz	4.38	
			36 MHz	9.65	

1. C_S = 5 pF (estimated value).

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

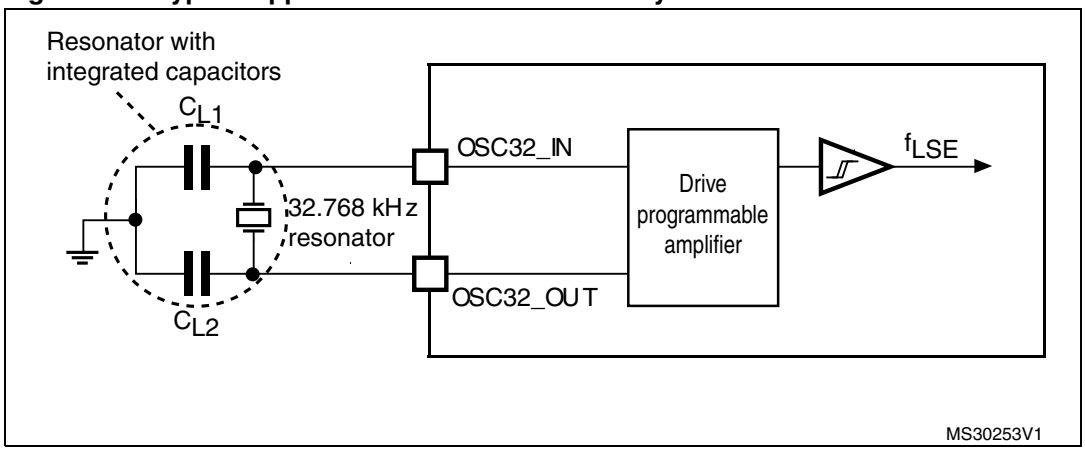
Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

The provided curves are chararacterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
TRIM	HSI user trimming step				1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)		55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8(3)		4.6(3)	%
		T_A = –10 to 85 °C	–2.9(3)		2.9(3)	%
		T_A = 0 to 70 °C				%
		T_A = 25 °C	–1		1	%
$t_{su(HSI)}$	HSI oscillator startup time		1(3)		2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100(3)	µA

1. V_{DDA} =3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	9	dBµV
			30 to 130 MHz	26	
			130 MHz to 1 GHz	30	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101, LQFP100, LQFP64, LQFP48 and BGA100 packages	II	500	
		T_A = +25 °C, conforming to JESD22-C101, WLCSP66 package	II	250	

1. Data based on characterization results, not tested in production.

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- PB2, PB10 and PE7 to PE15 I/O pins are powered from VDDSD12.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from VDDSD3. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 52 represents power voltage for a given I/O pin (VDD or VDDSD12 or VDDSD3).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* and *Figure 18* for standard I/Os, and in *Figure 19* and *Figure 20* for 5 V tolerant I/Os.

Figure 17. TC and TTa I/O input characteristics - CMOS port

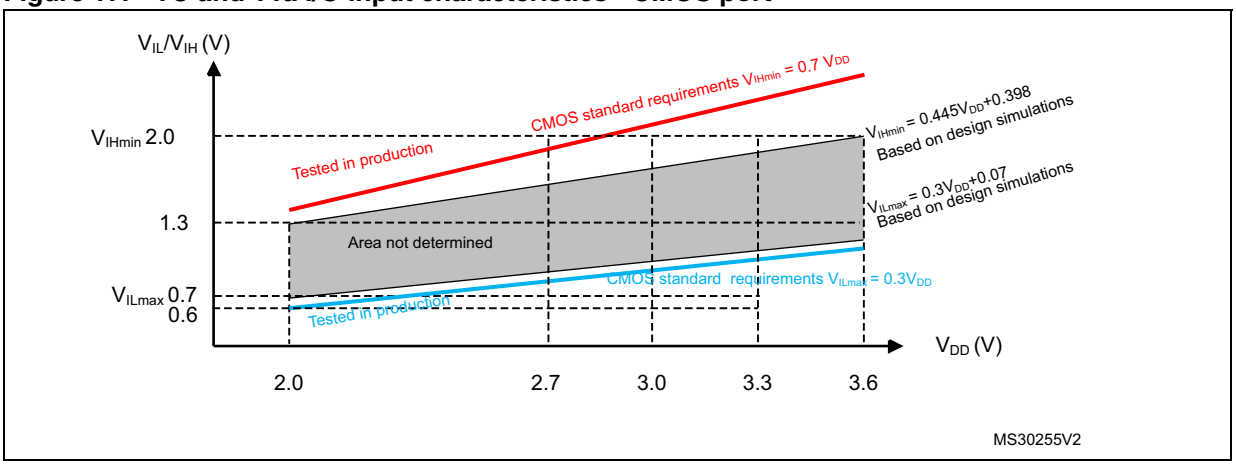


Figure 18. TC and TTa I/O input characteristics - TTL port

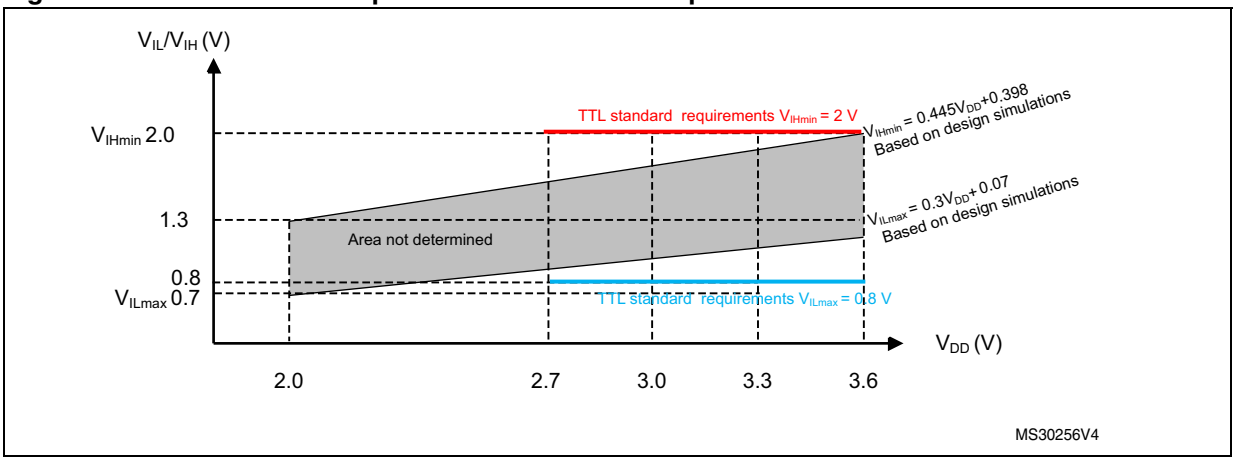


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

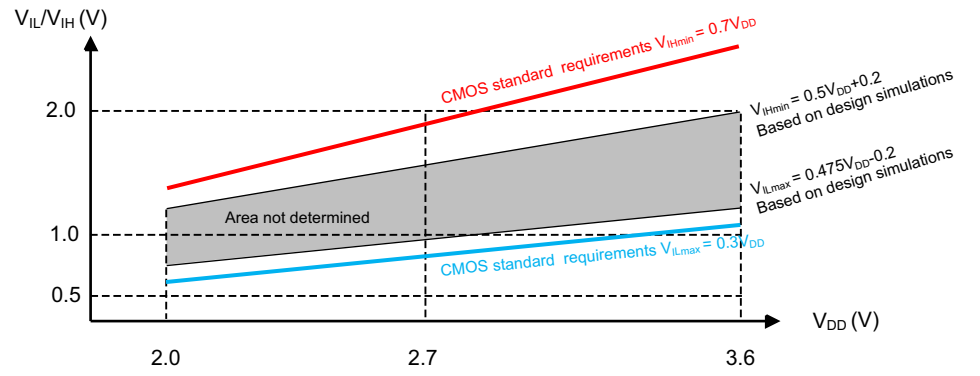
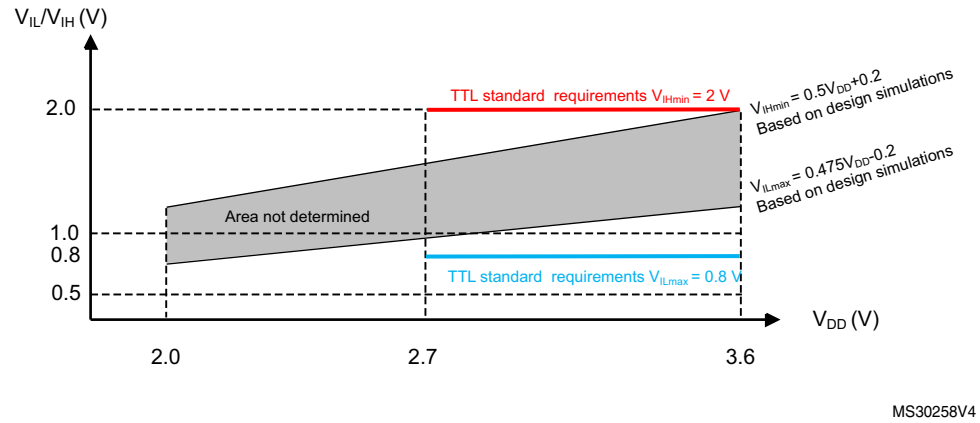


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on all VDD_x and VDDSDx, plus the maximum Run consumption of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 20*).
- The sum of the currents sunk by all the I/Os on all VSS_x and VSSSD, plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 20*).

6.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 56*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I^2C characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		0.26		µs
$t_{su(SDA)}$	SDA setup time	250		100		50		ns
$t_{h(SDA)}$	SDA data hold time	0(2)	3450(3)	0(2)	900(3)	0(4)	450(3)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300		120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300		120	ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		0.26		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		0.26		µs
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		0.26		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		0.5		µs
C_b	Capacitive load for each bus line		400		400		550	pF

1. The I^2C characteristics are the requirements from I^2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.
2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 120ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 29. ADC accuracy characteristics

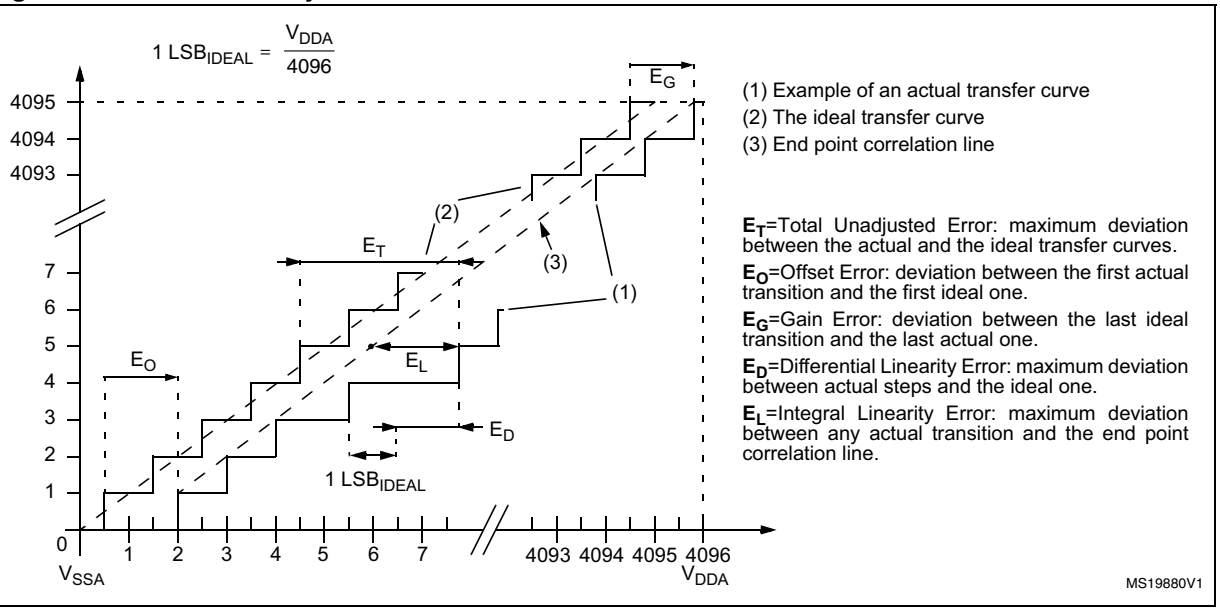
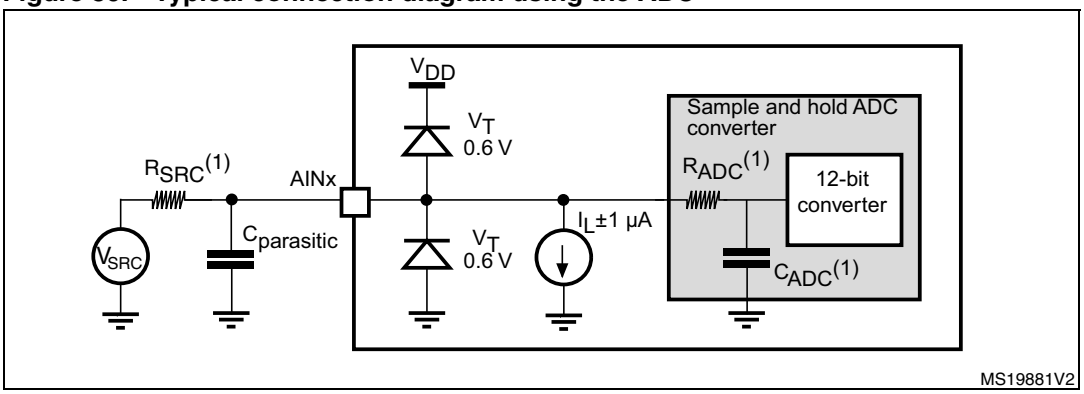


Figure 30. Typical connection diagram using the ADC



1. Refer to *Table 60* for the values of R_{SRC}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

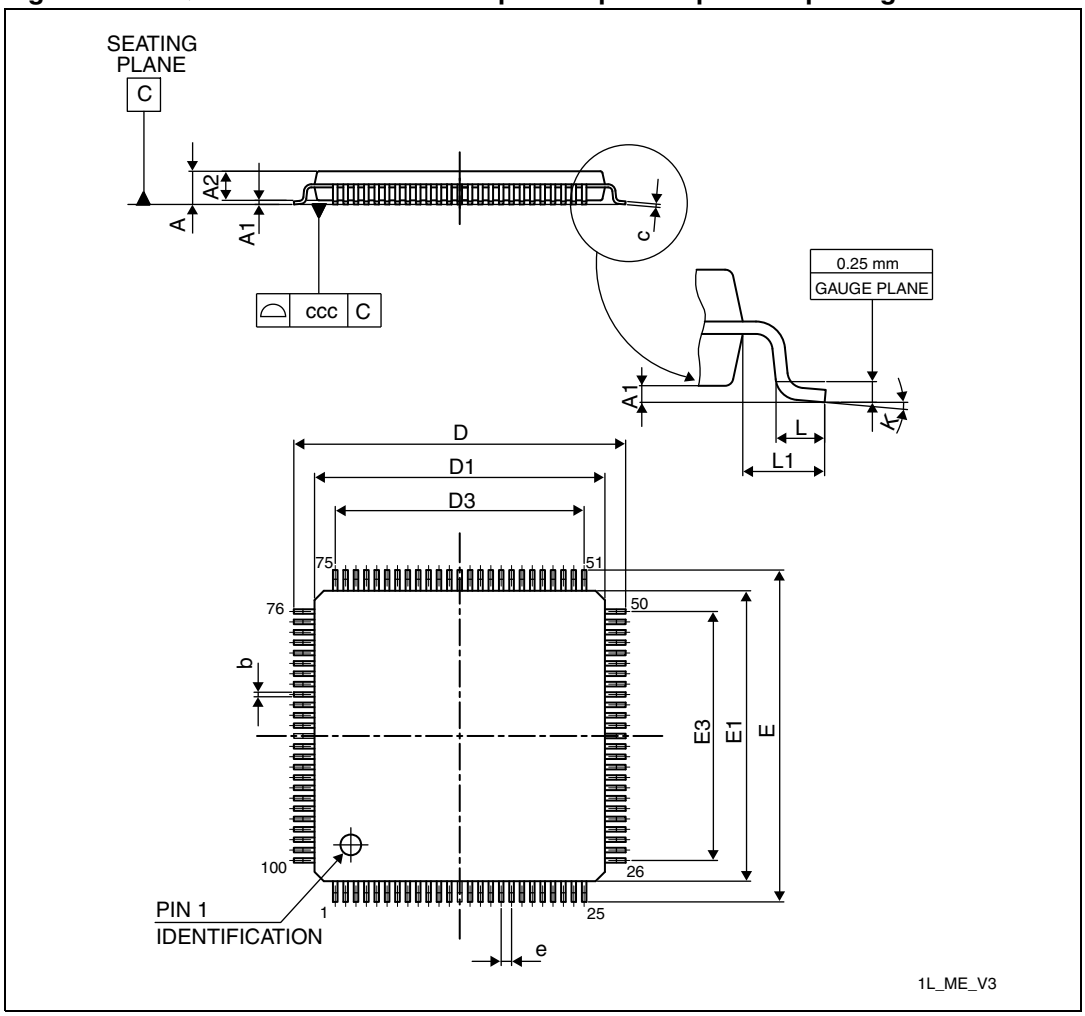
Power supply decoupling should be performed as shown in *Figure 9*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SINAD (4)	Signal to noise and distortion ratio	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	76	77		dB	ENOB = SINAD/6.02 -0.292
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	75	76			
						V_{REFSD+} = 3.3	76	77			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	70	74			
						V_{REFSD+} = 3.3	79	85			
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)	75	81			
		Single ended mode	gain =1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	72	73			
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	68	71			
						V_{REFSD+} = 3.3	72	73			
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	60	64			
						V_{REF} = 3.3	67	72			
THD(4)	Total harmonic distortion	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)		-77	-76	dB	
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-77	-76		
						V_{REFSD+} = 3.3		-77	-76		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-85	-70		
						V_{REFSD+} = 3.3		-93	-80		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)		-93	-83		
		Single ended mode	gain =1	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-72	-68		
						V_{REFSD+} = 3.3		-74	-72		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)		-66	-61		
						V_{REFSD+} = 3.3		-75	-70		

1. Data based on characterization results, not tested in production.

Figure 34. LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 77. LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data

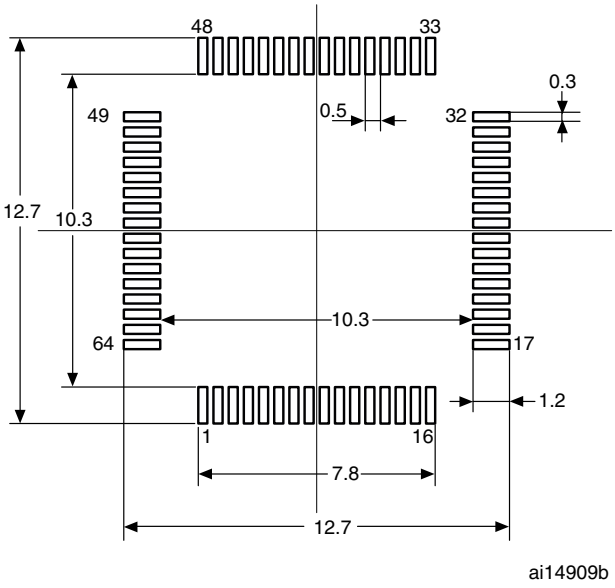
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	15.80	16.00	16.20	0.622	0.6299	0.6378
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.20	0.622	0.6299	0.6378

Table 78. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	11.80	12.00	12.20	0.4646	0.4724	0.4803
E1	9.80	10.00	10.20	0.3858	0.3937	0.4016
E3		7.50			0.2953	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
K	0°	3.5°	7°	0°	3.5°	7°
ccc			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint



1. Dimensions are in millimeters.