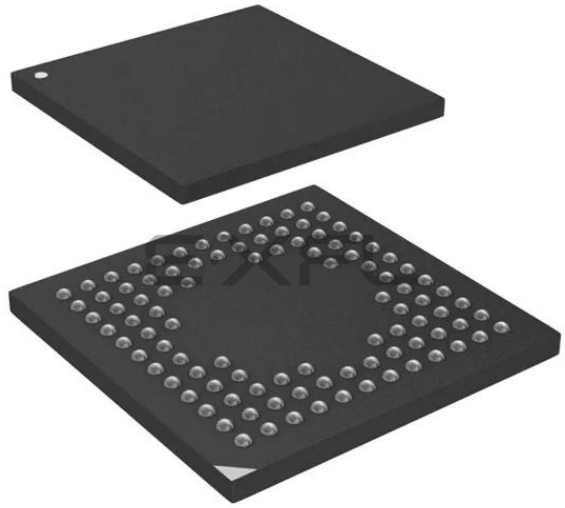

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372v8h6

List of figures

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins, and can be 2.0 to 3.6 V.
- V_{DDA} = 2.0 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR, without the need for an external reset circuit. The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either from V_{DD} supply when present or through the V_{BAT} pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28th, 29th (leap year), 30th and 31st day of the month.
- 2 programmable alarms with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

4 Pinouts and pin description

Figure 2. STM32F37x LQFP48 pinout

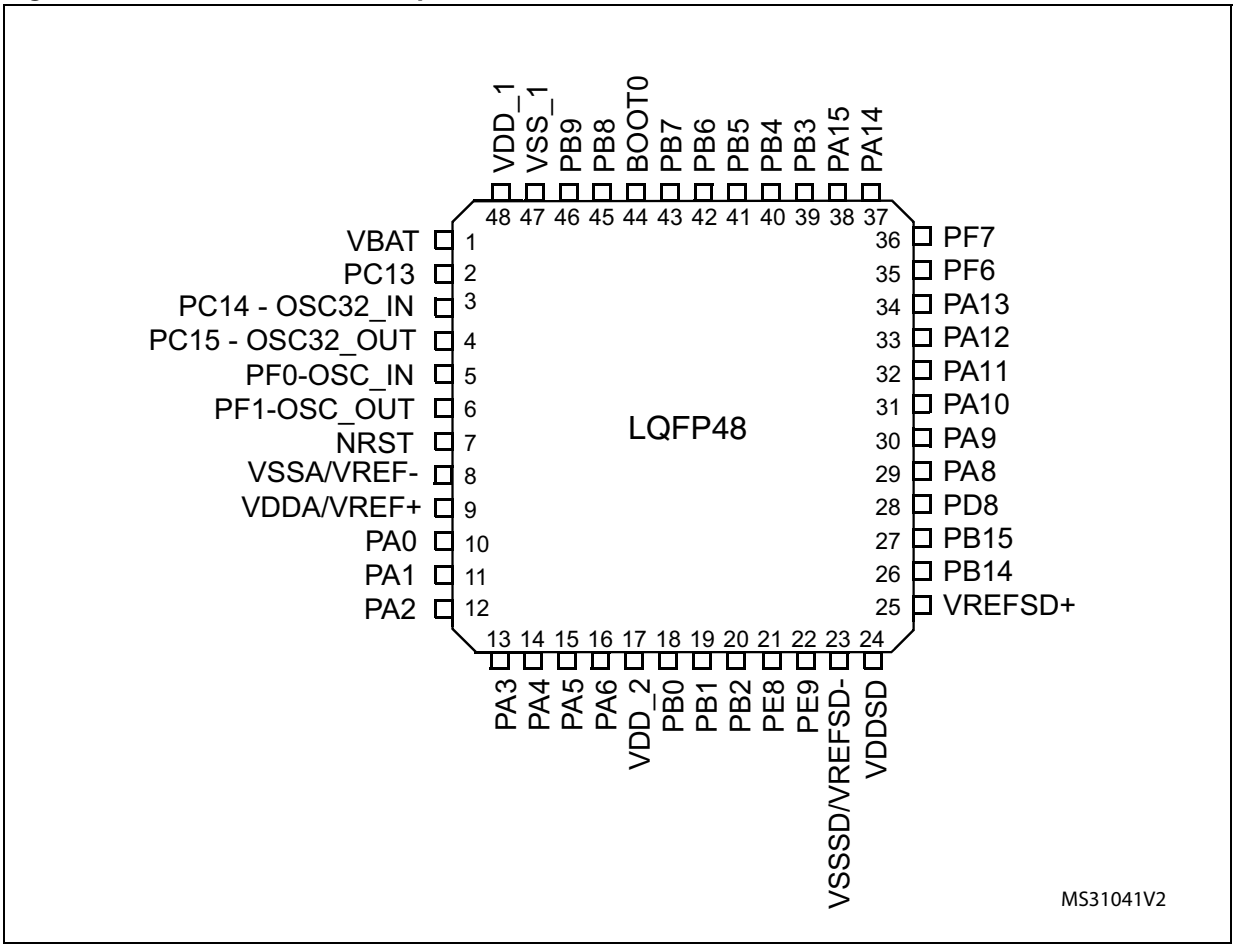


Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
43	L9			PE12	I/O	TC	(2) (1)		SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10			PE13	I/O	TC	(2) (1)		SDADC1_AIN0M , SDADC2_AIN2P
45	M11			PE14	I/O	TC	(2) (1)		SDADC2_AIN1P, SDADC2_AIN2M
46	M12			PE15	I/O	TC	(2) (1)	USART3_RX	SDADC2_AIN0P
47	L10			PB10	I/O	TC	(2) (1)	SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	SDADC2_AIN0M
48	L11			VREFSD-	S		(1)	External reference voltage for SDADC1, SDADC2, SDADC3 (negative input)	
49	F12			VSSSD	S		(1)	SDADC1, SDADC2, SDADC3 ground	
		31	23	VSSSD/ VREFSD-	S			SDADC1, SDADC2, SDADC3 ground / External reference voltage for SDADC1, SDADC2, SDADC3 (negative input)	
50	G12			VDDSD12	S		(1)	SDADC1 and SDADC2 power supply	
		32	24	VDDSD	S			SDADC1, SDADC2, SDADC3 power supply	
51	L12			VDDSD3	S		(1)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S			External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(3)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(3)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2	SDADC3_AIN7P, SDADC3_AIN8M, RTC_REFCLKIN
55	K9	36	28	PD8	I/O	TC	(3)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8			PD9	I/O	TC	(3) (1)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12			PD10	I/O	TC	(3) (1)	USART3_CK	SDADC3_AIN4P
58	J11			PD11	I/O	TC	(3) (1)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10			PD12	I/O	TC	(3) (1)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
73	C11	47	35	PF6	I/O	FTf		SPI1_MOSI/I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	
74	F11			VSS_3	S		(1)	Ground	
75	G11			VDD_3	S		(1)	Digital power supply	
		48	36	PF7	I/O	FTf		I2C2_SDA, USART2_CK	
76	A10	49	37	PA14	I/O	FTf		I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK	
77	A9	50	38	PA15	I/O	FTf		SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, I2C1_SCL, TIM2_CH1_ETR, TIM12_CH2, TSC_SYNC, JTDI	
78	B11	51		PC10	I/O	FT	(1)	SPI3_SCK/I2S3_CK, USART3_TX, TIM19_CH1	
79	C10	52		PC11	I/O	FT	(1)	SPI3_MISO/I2S3_MCK, USART3_RX, TIM19_CH2	
80	B10	53		PC12	I/O	FT	(1)	SPI3_MOSI/I2S3_SD, USART3_CK, TIM19_CH3	
81	C9			PD0	I/O	FT	(1)	CAN_RX, TIM19_CH4	
82	B9			PD1	I/O	FT	(1)	CAN_TX, TIM19_ETR	
83	C8	54		PD2	I/O	FT	(1)	TIM3_ETR	
84	B8			PD3	I/O	FT	(1)	SPI2_MISO/I2S2_MCK, USART2_CTS	
85	B7			PD4	I/O	FT	(1)	SPI2_MOSI/I2S2_SD, USART2_RTS	
86	A6			PD5	I/O	FT	(1)	USART2_TX	
87	B6			PD6	I/O	FT	(1)	SPI2_NSS/I2S2_WS, USART2_RX	
88	A5			PD7	I/O	FT	(1)	SPI2_SCK/I2S2_CK, USART2_CK	
89	A8	55	39	PB3	I/O	FT		SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM13_CH1, TSC_G5_IO1, JTDO-TRACESWO	

Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0		EVENTOUT	TIM5_CH1_ETR					
PC1		EVENTOUT	TIM5_CH2					
PC2		EVENTOUT	TIM5_CH3			SPI2_MISO/I2S2_MCK		
PC3		EVENTOUT	TIM5_CH4			SPI2_MOSI/I2S2_SD		
PC4		EVENTOUT	TIM13_CH1	TSC_G3_IO1				USART1_TX
PC5		EVENTOUT		TSC_G3_IO2				USART1_RX
PC6		EVENTOUT	TIM3_CH1			SPI1_NSS/I2S1_WS		
PC7		EVENTOUT	TIM3_CH2			SPI1_SCK/I2S1_CK		
PC8		EVENTOUT	TIM3_CH3			SPI1_MISO/I2S1_MCK		
PC9		EVENTOUT	TIM3_CH4			SPI1_MOSI/I2S1_SD		
PC10		EVENTOUT	TIM19_CH1				SPI3_SCK/I2S3_CK	USART3_TX
PC11		EVENTOUT	TIM19_CH2				SPI3_MISO/I2S3_MCK	USART3_RX
PC12		EVENTOUT	TIM19_CH3				SPI3_MOSI/I2S3_SD	USART3_CK
PC13								
PC14								
PC15								

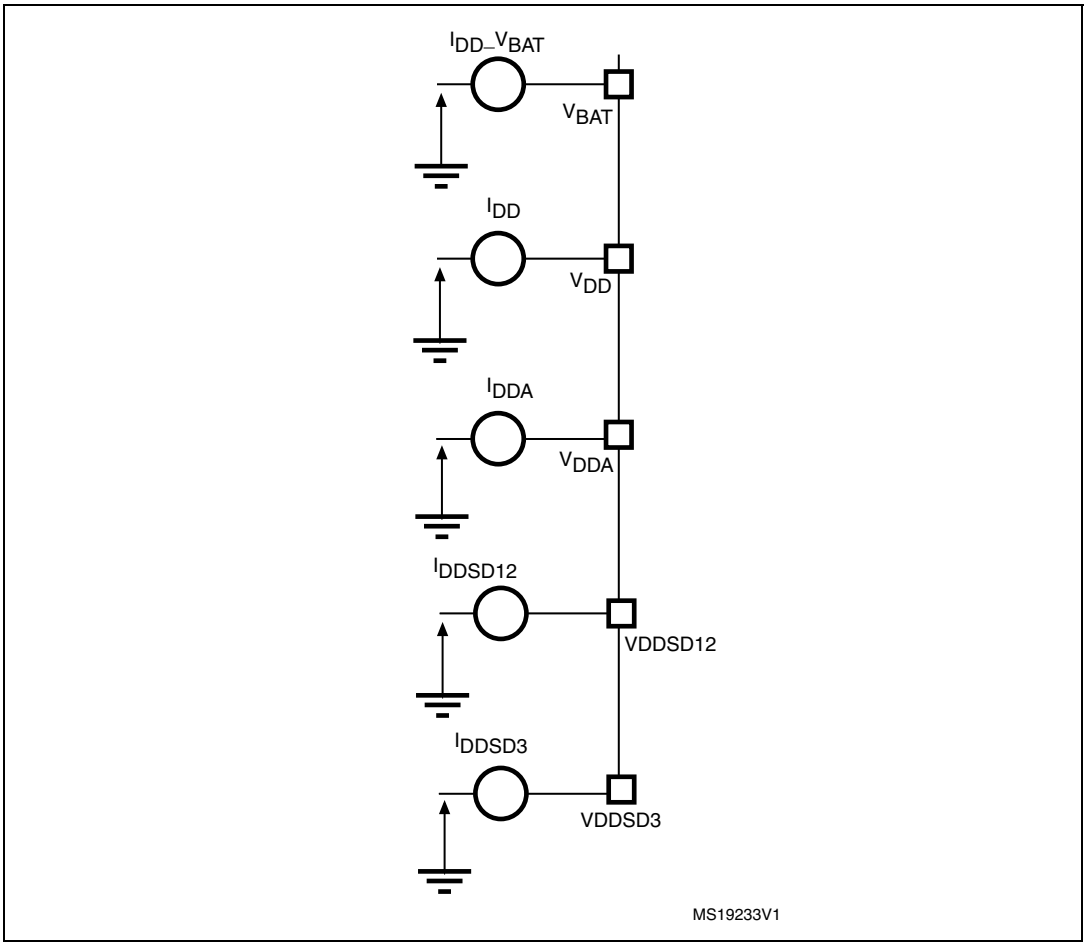
Table 18. STM32F37x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DDSDx}, V_{BAT} and V_{DD})	– 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$		0.4	
$V_{DDSDx} – V_{DDA}$	Allowed voltage difference for $V_{DDSDx} > V_{DDA}$		0.4	
$V_{REFSD+} – V_{DDSD3}$	Allowed voltage difference for $V_{REFSD+} > V_{DDSD3}$		0.4	
$V_{REF+} – V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$		0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	
	Input voltage on TC pins on SDADCx channels inputs(3)	V_{SS} – 0.3	4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert V_{SSX} – V_{SS}\rvert$	Variations between all the different ground pins		50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to V_{SS}).

All main power (VDD, VDDSD12, VDDSD3 and VDDA) and ground (VSS, VSSSD, and VSSA) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

The following relationship must be respected between V_{DDA} and V_{DDSD12}: V_{DDA} must power on before or at the same time as V_{DDSD12} or V_{DDSD3} in the power up sequence. V_{DDA} must be greater than or equal to V_{DDSD12} or V_{DDSD3}.

The following relationship must be respected between V_{DDSD12} and V_{DDSD3}: V_{DDSD3} must power on before or at the same time as V_{DDSD12} in the power up sequence.
After power up (V_{DDSD12} > Vrefint = 1.2 V) V_{DDSD3} can be higher or lower than V_{DDSD12}.

The following relationship must be respected between V_{REFSD+} and V_{DDSD12}, V_{DDSD3}: V_{REFSD+} must be lower than V_{DDSD3}.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

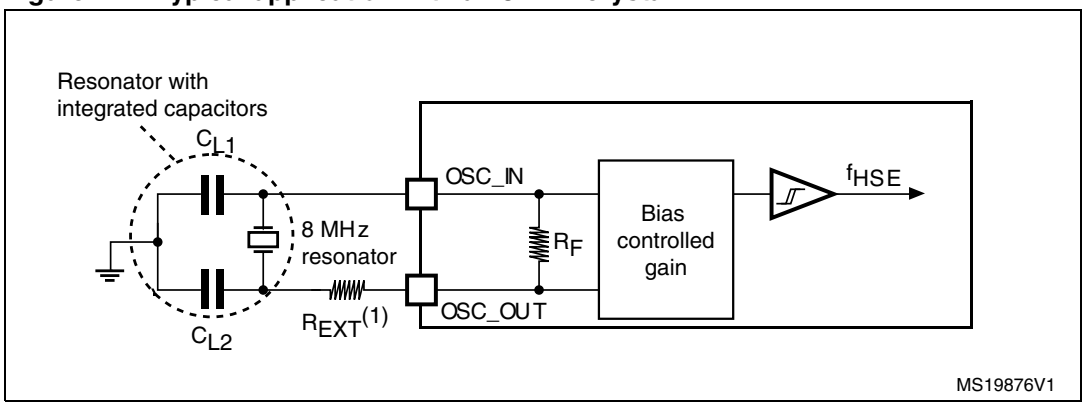
Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from RAM	HSE bypass, PLL on	72 MHz	63.6 (2)	70.7(2)	75.7(2)	72.3(2)	30.0 (2)	31.9(2)	32.6(2)	33.8(2)	mA
			64 MHz	56.7	62.5	67.1	64.0	26.7	28.6	29.3	30.0	
			48 MHz	42.0	50.5	47.4	50.1	20.2	21.5	22.1	22.7	
			32 MHz	28.3	32.1	31.8	33.7	13.4	14.6	14.8	15.7	
			24 MHz	21.1	25.0	24.2	25.9	10.0	11.3	11.2	12.6	
		HSE bypass, PLL off	8 MHz	6.9	7.4	8.3	8.7	3.4	3.7	4.1	4.8	
			1 MHz	0.8	1.2	1.5	2.0	0.4	0.6	1.0	1.5	
		HSI clock, PLL on	64 MHz	51.9	59.5	59.4	58.6	26.4	28.1	28.7	29.5	
			48 MHz	38.1	44.7	43.8	45.4	20.0	21.3	21.9	22.3	
			32 MHz	25.9	31.2	29.4	30.5	13.2	14.3	14.6	15.5	
			24 MHz	19.6	22.7	22.6	23.2	6.5	7.0	7.9	8.2	
		HSI clock, PLL off	8 MHz	6.6	7.1	8.0	8.4	3.3	3.7	4.0	4.7	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	72 MHz	43.2	46.9	48.7	52.5	6.7	7.2	7.6	8.3	
			64 MHz	38.5	41.6	43.7	46.6	5.9	6.5	6.8	7.5	
			48 MHz	29.1	31.3	32.5	34.1	4.5	4.9	5.3	5.9	
			32 MHz	19.4	21.1	24.6	23.0	3.0	3.4	3.8	4.4	
			24 MHz	14.7	16.1	18.5	17.6	2.4	2.6	3.0	3.6	
		HSE bypass, PLL off	8 MHz	4.9	5.3	6.1	6.6	0.8	1.0	1.4	1.9	
			1 MHz	0.6	0.9	1.3	1.8	0.1	0.3	0.6	1.2	
		HSI clock, PLL on	64 MHz	34.5	37.1	39.6	42.0	5.6	6.1	6.5	7.1	
			48 MHz	26.1	28.0	29.0	30.7	4.2	4.6	5.0	5.6	
			32 MHz	17.4	19.1	21.1	20.8	2.9	3.2	3.6	4.2	
			24 MHz	13.3	14.6	16.1	16.0	1.5	1.8	2.2	2.6	
		HSI clock, PLL off	8 MHz	4.5	4.9	5.5	6.1	0.7	0.9	1.3	1.8	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

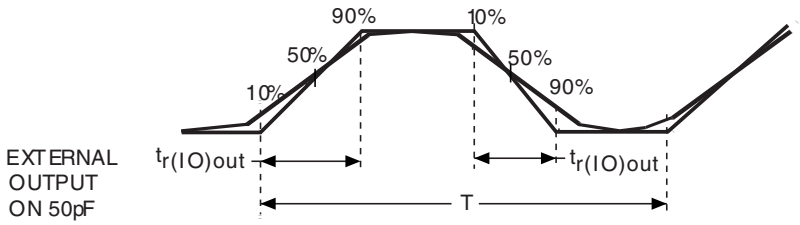
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability		0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability			1	
		LSEDRV[1:0] = 10 medium high driving capability			1.3	
		LSEDRV[1:0]=11 higher driving capability			1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5			µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8			
		LSEDRV[1:0] = 10 medium high driving capability	15			
		LSEDRV[1:0]=11 higher driving capability	25			
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized		2		s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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6.3.15 NRST characteristics

NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 52*).

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage				$0.3V_{DD}$ +0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.445 V_{DD}+ 0.398 (1)			
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		500			ns

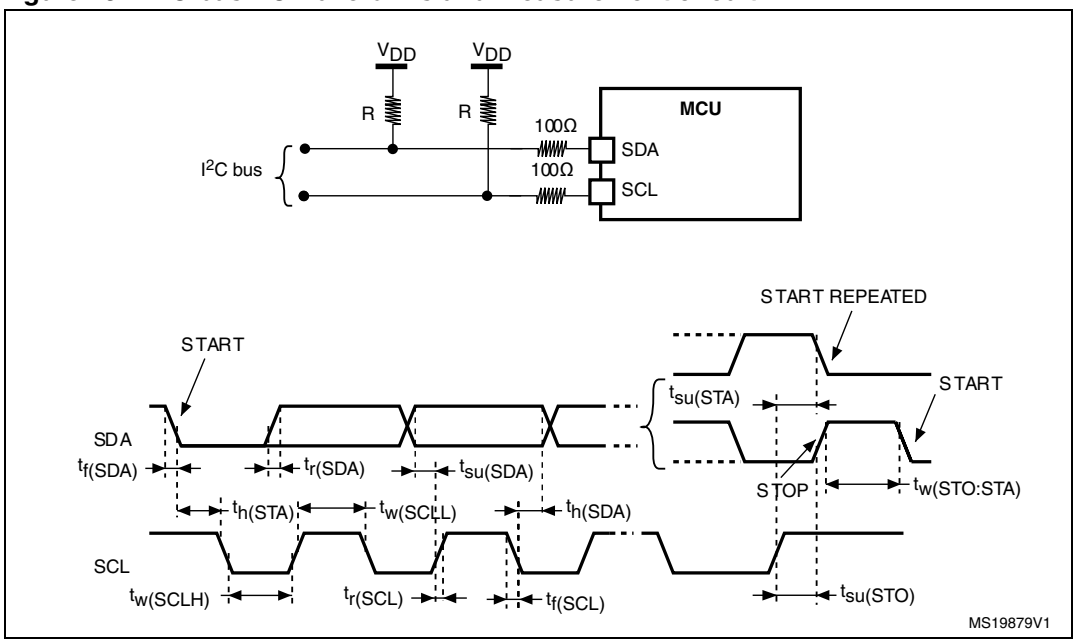
1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Table 57. I^2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 23. I^2C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Equation 1: R_{SRC} max formula

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{SRC} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{SRC} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	50
239.5	17.1	50

1. Guaranteed by design, not tested in production.

Table 62. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±3	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V T_A = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

2. For f_{ADC} lower than 5 MHz, there will be a performance degradation of around 2 dB due to flicker noise increase.
3. If the reference value is lower than 2.4 V, there will be a performance degradation proportional to the reference supply drop, according to this formula: $20*\log10(V_{REF}/2.4)$ dB
4. SNR, THD, SINAD parameters are valid for frequency bandwidth 20Hz - 1kHz. Input signal frequency is 300Hz (for f_{ADC}=6MHz) and 100Hz (for f_{ADC}=1.5MHz).

Table 75. VREFSD+ pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{REFINT}	Internal reference voltage	Buffered embedded reference voltage (1.2 V)		1.2		V	See *Section 6.3.4: Embedded reference voltage on page 58*
		Embedded reference voltage amplified by factor 1.5		1.8			
$C_{VREFSD+}$(2)	Reference voltage filtering capacitor	$V_{REFSD+} = V_{REFINT}$	1000		10000	nF	
$R_{VREFSD+}$	Reference voltage input impedance	Fast mode (f_{ADC} = 6 MHz)		238		kΩ	See RM0313 reference manual for detailed description
		Slow mode (f_{ADC} = 1.5 MHz)		952			

1. Data based on characterization results, not tested in production.
2. If internal reference voltage is selected then this capacitor is charged through internal resistance - typ. 300 ohm. If internal reference source is selected through the reference voltage selection bits (REFV<>"00" in SDADC_CR1 register), the application must first configure REFV bits and then wait for capacitor charging. Recommended waiting time is 3 ms if 1 µF capacitor is used.

7 Package characteristics

7.1 Package mechanical data

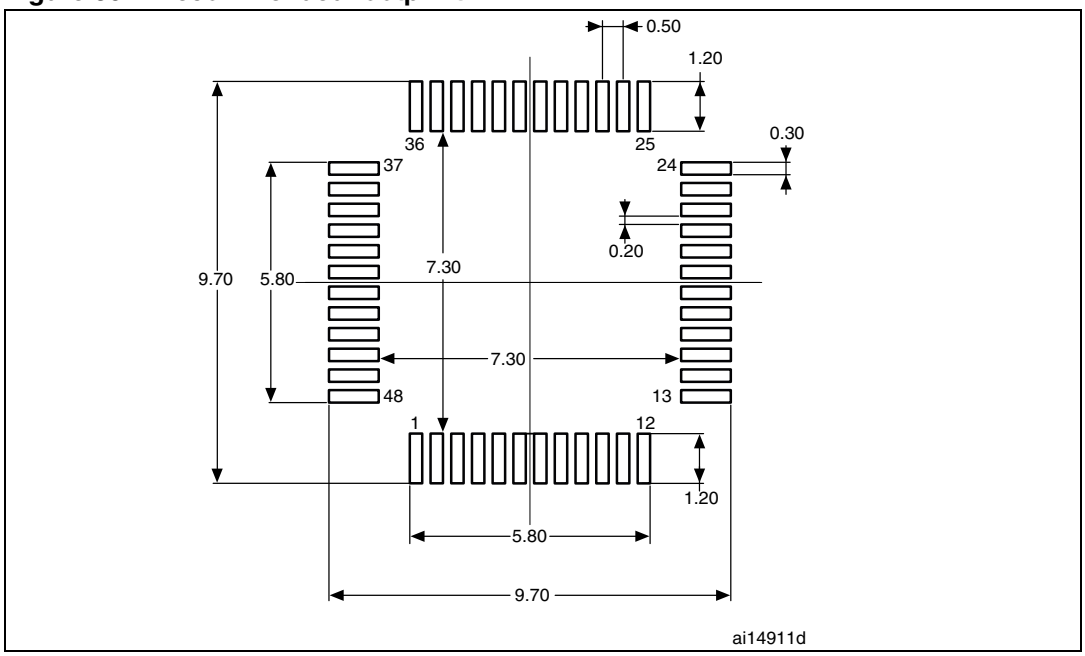
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
K	0°	3.5°	7°	0°	3.5°	7°
ccc			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. Recommended footprint



1. Dimensions are in millimeters.