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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 1x12b, 1x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372v8t6 |

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F37x microcontrollers.

This STM32F37x datasheet should be read in conjunction with the STM32F37x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.subset.cortexm.m4/index.html and also refer to the STM32F3xxx and STM32F4xxx Cortex-M4 programming manual (PM0214) at address: http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/PROGRAMMING_MANUAL/DM00046982.pdf

# 2 Description

The STM32F37x family is based on the high-performance ARM® Cortex™-M4F 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F37x devices offer one fast 12-bit ADC (1 Msps), up to three 16-bit Sigma delta ADCs, up to two comparators, up to two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: up to two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F37x family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F37x family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

## 3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F37x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F37x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

## 3.14 Digital-to-analog converter (DAC)

The devices feature up to two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Up to two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- triangular-wave generation
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

## 3.15 Fast comparators (COMP)

The STM32F37x embeds up to 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage ($V_{REFINT}$) or submultiple (1/4 $V_{REFINT}$, 1/2 $V_{REFINT}$ and 3/4 $V_{REFINT}$)

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

Table 11. STM32F37x pin definitions (continued)

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 29 | M3 | 20 | 14 | PA4 | I/O | TTa | | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1, | ADC_IN4, DAC1_OUT1 |
| 30 | K4 | 21 | 15 | PA5 | I/O | TTa | | SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2 | ADC_IN5, DAC1_OUT2 |
| 31 | L4 | 22 | 16 | PA6 | I/O | TTa | | SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3 | ADC_IN6, DAC2_OUT1, |
| 32 | M4 | 23 | | PA7 | I/O | TTa | (1) | TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT | ADC_IN7 |
| 33 | K5 | 24 | | PC4 | I/O | TTa | (1) | TIM13_CH1, TSC_G3_IO1, USART1_TX | ADC_IN14 |
| 34 | L5 | 25 | | PC5 | I/O | TTa | (1) | TSC_G3_IO2, USART1_RX | ADC_IN15 |
| 35 | M5 | 26 | 18 | PB0 | I/O | TTa | | SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2 | ADC_IN8, SDADC1_AIN6P |
| 36 | M6 | 27 | 19 | PB1 | I/O | TTa | | TIM3_CH4, TSC_G3_IO4 | ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M |
| 37 | L6 | 28 | 20 | PB2 | I/O | TC | (2) | | SDADC1_AIN4P, SDADC2_AIN6P |
| 38 | M7 | | | PE7 | I/O | TC | (2) (1) | | SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M |
| 39 | L7 | 29 | 21 | PE8 | I/O | TC | (2) | | SDADC1_AIN8P, SDADC2_AIN8P |
| 40 | M8 | 30 | 22 | PE9 | I/O | TC | (2) | | SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M |
| 41 | L8 | | | PE10 | I/O | TC | (2) (1) | | SDADC1_AIN2P |
| 42 | M9 | | | PE11 | I/O | TC | (2) (1) | | SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P |

Table 11. STM32F37x pin definitions (continued)

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | BGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 90 | A7 | 56 | 40 | PB4 | I/O | FT | | SPI1_MISO/I2S1_MCK, SPI3_MISO/I2S3_MCK, USART2_RX, TIM16_CH1, TIM3_CH1, TIM17_BKIN, TIM15_CH1N, TSC_G5_IO2, JNTRST | |
| 91 | C5 | 57 | 41 | PB5 | I/O | FT | | SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAI, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR | |
| 92 | B5 | 58 | 42 | PB6 | I/O | FTf | | I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3 | |
| 93 | B4 | 59 | 43 | PB7 | I/O | FTf | | I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4 | |
| 94 | A4 | 60 | 44 | BOOT0 | I | B | | Boot memory selection | |
| 95 | A3 | 61 | 45 | PB8 | I/O | FTf | | SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC | |
| 96 | B3 | 62 | 46 | PB9 | I/O | FTf | | SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT | |
| 97 | C3 | | | PE0 | I/O | FT | (1) | USART1_TX, TIM4_ETR | |
| 98 | A2 | | | PE1 | I/O | FT | (1) | USART1_RX | |
| 99 | D3 | 63 | 47 | VSS_1 | S | | | Ground | |
| 100 | C4 | 64 | 48 | VDD_1 | S | | | Digital power supply | |

1. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. these pins are powered by VDDSD12.
3. these pins are powered by VDDSD3.

**Table 14. Alternate functions for port PC**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| PC0 | | EVENTOUT | TIM5_CH1_ETR | | | | | |
| PC1 | | EVENTOUT | TIM5_CH2 | | | | | |
| PC2 | | EVENTOUT | TIM5_CH3 | | | SPI2_MISO/I2S2_MCK | | |
| PC3 | | EVENTOUT | TIM5_CH4 | | | SPI2_MOSI/I2S2_SD | | |
| PC4 | | EVENTOUT | TIM13_CH1 | TSC_G3_IO1 | | | | USART1_TX |
| PC5 | | EVENTOUT | | TSC_G3_IO2 | | | | USART1_RX |
| PC6 | | EVENTOUT | TIM3_CH1 | | | SPI1_NSS/I2S1_WS | | |
| PC7 | | EVENTOUT | TIM3_CH2 | | | SPI1_SCK/I2S1_CK | | |
| PC8 | | EVENTOUT | TIM3_CH3 | | | SPI1_MISO/I2S1_MCK | | |
| PC9 | | EVENTOUT | TIM3_CH4 | | | SPI1_MOSI/I2S1_SD | | |
| PC10 | | EVENTOUT | TIM19_CH1 | | | | SPI3_SCK/I2S3_CK | USART3_TX |
| PC11 | | EVENTOUT | TIM19_CH2 | | | | SPI3_MISO/I2S3_MCK | USART3_RX |
| PC12 | | EVENTOUT | TIM19_CH3 | | | | SPI3_MOSI/I2S3_SD | USART3_CK |
| PC13 | | | | | | | | |
| PC14 | | | | | | | | |
| PC15 | | | | | | | | |

Table 18. STM32F37x peripheral register boundary addresses

| Bus | Boundary address | Size | Peripheral |
|---|---|---|---|
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1KB | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1KB | GPIOE |
| | 0x4800 0C00 - 0x4800 0FFF | 1KB | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1KB | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1KB | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1KB | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 MB | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 KB | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 KB | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 KB | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 KB | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 KB | FLASH memory interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 KB | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 KB | RCC |
| | 0x4002 0800- 0x4002 0FFF | 2 KB | Reserved |
| | 0x4002 0400 - 0x4002 07FF | 1 KB | DMA2 |
| | 0x4002 0000 - 0x4002 03FF | 1 KB | DMA1 |
| | 0x4001 6C00 - 0x4001 FFFF | 37 KB | Reserved |

Depending on the SDADCx operation mode, there can be more constraints between $V_{REFSD+}$, $V_{DDSD12}$ and $V_{DDSD3}$ which are described in reference manual RM0313.

**Table 20. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD(\Sigma)}$ | Total current into sum of all VDD_x and VDDSDx power lines (source)(1) | 160 | mA |
| $I_{VSS(\Sigma)}$ | Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1) | -160 | |
| $I_{VDD(PIN)}$ | Maximum current into each VDD_x or VDDSDx power pin (source)(1) | 100 | |
| $I_{VSS(PIN)}$ | Maximum current out of each VSS_x or VSSSD ground pin (sink)(1) | -100 | |
| $I_{IO(PIN)}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/O and control pin | - 25 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all IOs and control pins(2) | 80 | |
| | Total output current sourced by sum of all IOs and control pins(2) | -80 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FTf and B pins(3) | -5/+0 | |
| | Injected current on TC and RST pin(4) | ± 5 | |
| | Injected current on TTa pins(5) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(6) | ± 25 | |

1. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to $V_{SS}$). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to $V_{SS}$). $V_{DD}$ (VDD_x) is the external power supply for all remaining I/O pins (the I/O pin ground is internally connected to $V_{SS}$).
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ}$(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 62*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 21. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

**Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on | 72 MHz | 42.8 | 6.9 | mA |
| | | | 64 MHz | 38.2 | 6.2 | |
| | | | 48 MHz | 28.9 | 4.8 | |
| | | | 32 MHz | 19.5 | 3.4 | |
| | | | 24 MHz | 14.7 | 2.7 | |
| | | | 16 MHz | 10.2 | 2.0 | |
| | | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off | 8 MHz | 5.2 | 1.2 | |
| | | | 4 MHz | 3.4 | 1.1 | |
| | | | 2 MHz | 2.2 | 0.9 | |
| | | | 1 MHz | 1.6 | 0.9 | |
| | | | 500 kHz | 1.4 | 0.8 | |
| | | | 125 kHz | 1.1 | 0.8 | |
| $I_{DDA}$(1) | Supply current in Sleep mode from $V_{DDA}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on | 72 MHz | 242.9 | 241.5 | µA |
| | | | 64 MHz | 213.7 | 212.7 | |
| | | | 48 MHz | 158.8 | 158.0 | |
| | | | 32 MHz | 107.6 | 107.3 | |
| | | | 24 MHz | 82.7 | 82.6 | |
| | | | 16 MHz | 58.3 | 58.2 | |
| | | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off | 8 MHz | 1.2 | 1.2 | |
| | | | 4 MHz | 1.2 | 1.2 | |
| | | | 2 MHz | 1.2 | 1.2 | |
| | | | 1 MHz | 1.2 | 1.2 | |
| | | | 500 kHz | 1.2 | 1.2 | |
| | | | 125 kHz | 1.2 | 1.2 | |

1. $V_{DDA}$ monitoring is off, $V_{DDSD12}$ monitoring is off.

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature at 25°C and $V_{DD} = V_{DDA}$= 3.3 Volts

**Table 36. Peripheral current consumption**

| Peripheral | Typical consumption(1) | Unit |
|---|---|---|
| **AHB peripherals** | | |
| BusMatrix(2) | 6.9 | µA/MHz |
| DMA1 | 18.3 | |
| DMA2 | 4.8 | |
| CRC | 2.6 | |
| GPIOA | 12.2 | |
| GPIOB | 11.9 | |
| GPIOC | 4.3 | |
| GPIOD | 12.0 | |
| GPIOE | 4.4 | |
| GPIOF | 3.7 | |
| TSC | 5.7 | |
| **APB2 peripherals** | | |
| APB2-Bridge(3) | 4.2 | |
| SYSCFG | 2.8 | |
| ADC1 | 17.7 | |
| SPI1 | 12.3 | |
| USART1 | 22.9 | |
| TIM15 | 15.7 | |
| TIM16 | 12.2 | |
| TIM17 | 12.1 | |
| TIM19 | 18.5 | |
| SDAC1 | 10.8 | |
| SDAC2 | 10.5 | |
| SDAC3 | 10.3 | |

**Table 36. Peripheral current consumption**

| Peripheral | Typical consumption[1] | Unit |
|---|---|---|
| **APB1 peripherals** | | µA/MHz |
| APB1-Bridge[3] | 6.9 | |
| TIM2 | 47.9 | |
| TIM3 | 36.8 | |
| TIM4 | 36.9 | |
| TIM5 | 45.5 | |
| TIM6 | 8.4 | |
| TIM7 | 8.2 | |
| TIM12 | 21.3 | |
| TIM13 | 14.2 | |
| TIM14 | 14.4 | |
| TIM18 | 10.1 | |
| WWDG | 4.7 | |
| SPI2 | 24.3 | |
| SPI3 | 25.3 | |
| USART2 | 45.3 | |
| USART3 | 43.1 | |
| I2C1 | 14.0 | |
| I2C2 | 13.9 | |
| USB | 27.9 | |
| CAN | 38.1 | |
| DAC2 | 7.7 | |
| PWR | 5.4 | |
| DAC1 | 14.8 | |
| CEC | 5.4 | |

1. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.
2. The BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 41. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]= 01 medium low driving capability | | | 1 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | | | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | | | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | | | µA/V |
| | | LSEDRV[1:0]= 01 medium low driving capability | 8 | | | |
| | | LSEDRV[1:0] = 10 medium high driving capability | 15 | | | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | | | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | | 2 | | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 48. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | 9 | dBµV |
| | | | 30 to 130 MHz | 26 | |
| | | | 130 MHz to 1 GHz | 30 | |
| | | | SAE EMI Level | 4 | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 49. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to JESD22-C101, LQFP100, LQFP64, LQFP48 and BGA100 packages | II | 500 | |
| | | $T_A$ = +25 °C, conforming to JESD22-C101, WLCSP66 package | II | 250 | |

1. Data based on characterization results, not tested in production.

**Table 51. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 pin | -0 | NA | mA |
| | Injected current on PC0 pin | -0 | +5 | |
| | Injected current on TC type I/O pins on VDDSD12 power domain: PB0, PB1, PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with induced leakage current on other pins from this group less than -50 µA | -5 | +5 | |
| | Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with induced leakage current on other pins from this group less than -50 µA | -5 | +5 | |
| | Injected current on TTa type pins: PA4, PA5, PA6 with induced leakage current on adjacent pins less than -10 µA | -5 | +5 | |
| | Injected current on any other FT and FTf pins | -5 | NA | |
| | Injected current on any other pins | -5 | +5 | |

*Note: 1 It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

**Equation 1: $R_{SRC}$ max formula**

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 61. $R_{SRC}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{SRC}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | 50 |
| 239.5 | 17.1 | 50 |

1. Guaranteed by design, not tested in production.

**Table 62. ADC accuracy(1)(2) (3)**

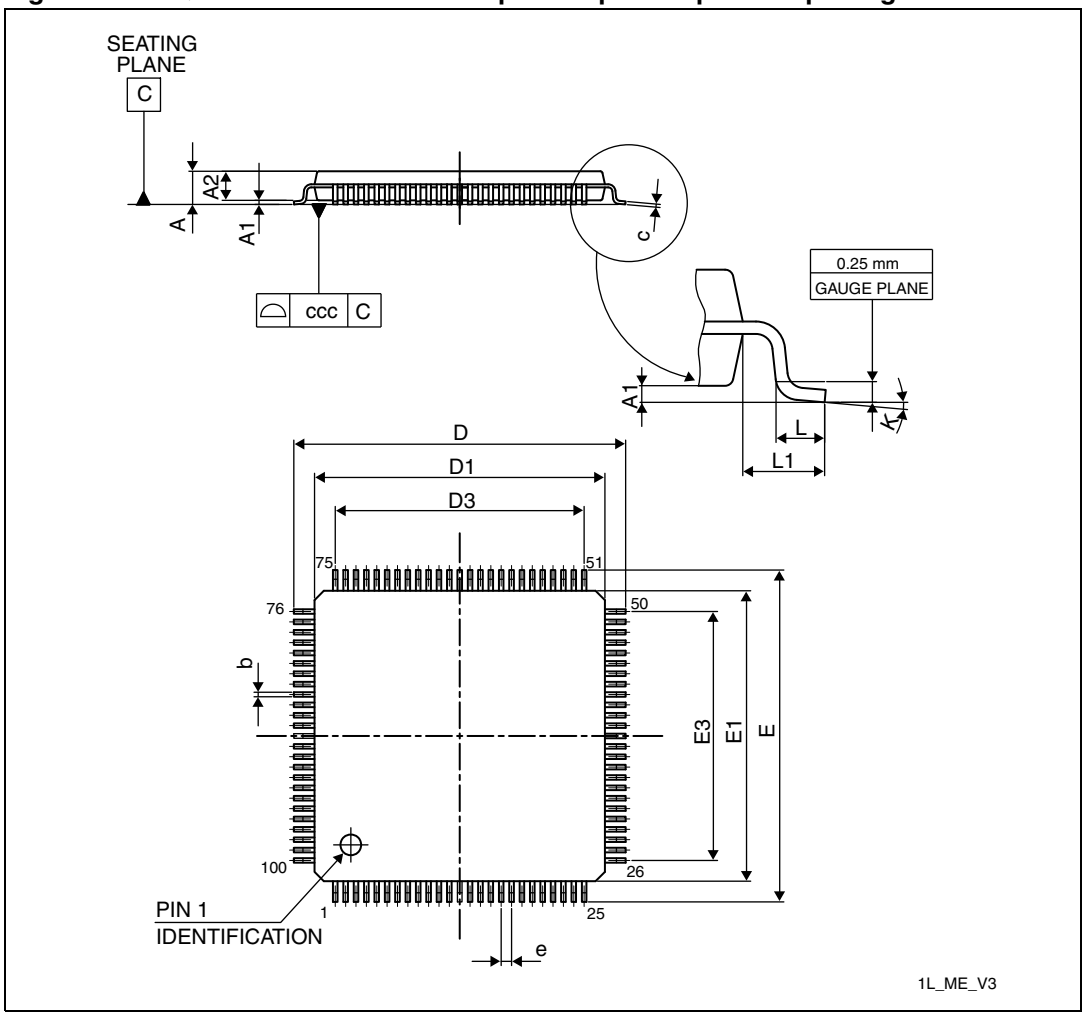
| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V $T_A$ = 25 °C | ±1.3 | ±3 | LSB |
| EO | Offset error | | ±1 | ±2 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 2.7 V to 3.6 V $T_A$ = -40 to 105 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |
| ET | Total unadjusted error | $f_{ADC}$ = 14 MHz, $R_{SRC}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V $T_A$ = 25 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |

1. ADC DC accuracy values are measured after internal calibration.

**Table 74. SDADC characteristics (continued)[1]**

| Symbol | Parameter | Conditions | | | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNR[4] | Signal to noise ratio | Differential mode | gain = 1 | $f_{ADC}$ = 1.5 MHz | $V_{DDSDx}$ = 3.3 | $V_{REFSD+}$ = 3.3[2] | 84 | 85 | | dB | |
| | | | | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$= 1.2[3] | 86 | 88 | | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | 88 | 92 | | | |
| | | | gain = 8 | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$ = 1.2[3] | 76 | 78 | | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | 82 | 86 | | | |
| | | | | $f_{ADC}$ = 1.5 MHz | | $V_{REFSD+}$= 3.3[2] | 76 | 80 | | | |
| | | Single ended mode | gain = 1 | $f_{ADC}$ = 1.5MHz | | $V_{REFSD+}$ = 3.3 | 80 | 84 | | | |
| | | | | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$ = 1.2[3] | 77 | 81 | | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | 85 | 90 | | | |
| | | | gain = 8 | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$ = 1.2[3] | 66 | 71 | | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | 74 | 78 | | | |

**Figure 34. LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 77. LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data**

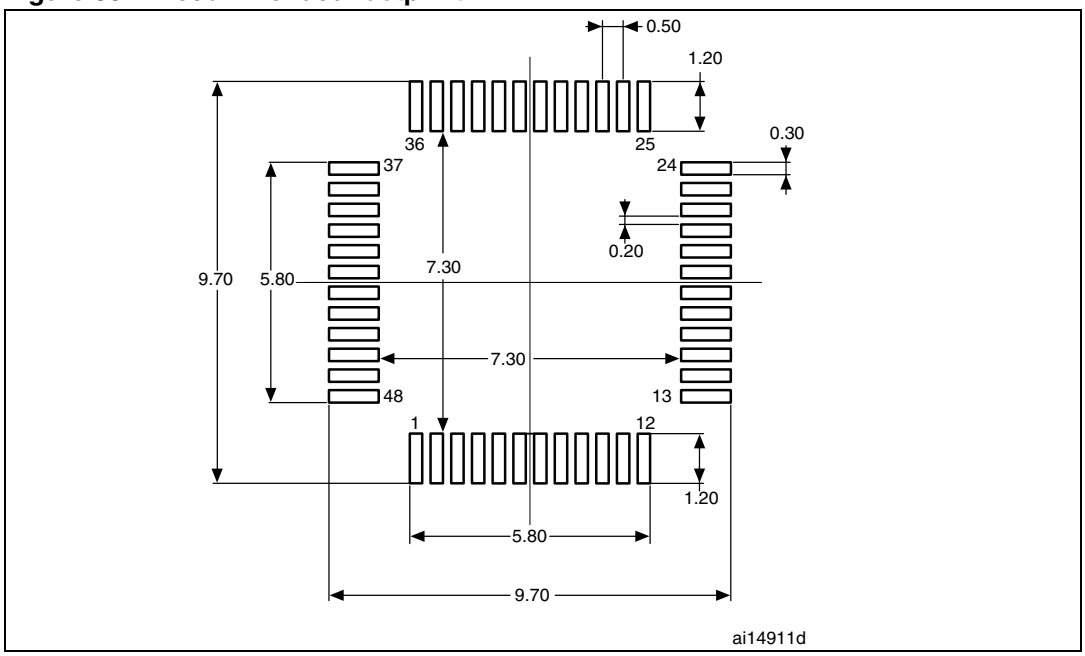
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | 15.80 | 16.00 | 16.20 | 0.622 | 0.6299 | 0.6378 |
| D1 | 13.80 | 14.00 | 14.20 | 0.5433 | 0.5512 | 0.5591 |
| D3 | | 12.00 | | | 0.4724 | |
| E | 15.80 | 16.00 | 16.20 | 0.622 | 0.6299 | 0.6378 |

**Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| e | | 0.50 | | | 0.0197 | |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | | 0.08 | | | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. Recommended footprint**




1. Dimensions are in millimeters.

Using the values obtained in *Table 80* $T_{Jmax}$ is calculated as follows:

– For LQFP100, 46°C/W

$T_{Jmax}$ = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < $T_J$ < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

**Figure 40. LQFP64 $P_D$ max vs. $T_A$**