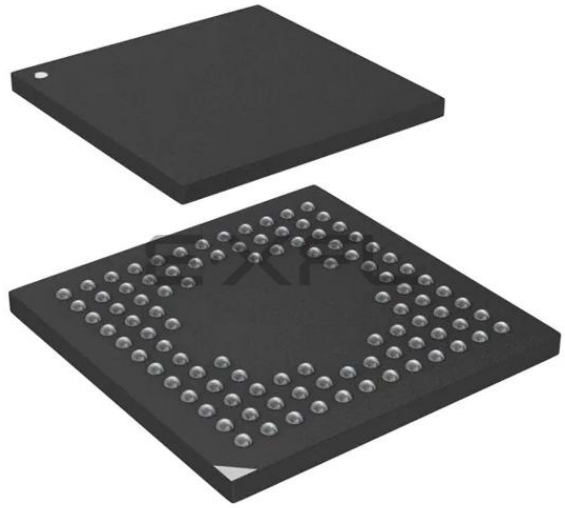


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372vch6

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of µA per pin can be observed if V_{DDA} is higher than V_{DDIO}.

3.10 Direct memory access (DMA)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F37x devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F37x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F37x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F37x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 4. No. of capacitive sensing channels available on STM32F37x devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F37xCx	STM32F37xRx	STM32F37xVx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

3.17 Timers and watchdogs

The STM32F37x includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F37x embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smart Card mode (ISO 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F37x USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in

Table 18. STM32F37x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	72	
V_{DD}	Standard operating voltage	Must have a potential equal to or lower than V_{DDA}	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC and DAC used)	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
	Analog operating voltage (ADC and DAC not used)		2	3.6	
V_{DDSD12}	VDDSD12 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD12 operating voltage (SDADC not used)		2.0	3.6	
V_{DDSD3}	VDDSD3 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD3 operating voltage (SDADC not used)		2.0	3.6	
V_{BAT}	Backup operating voltage		1.65	3.6	V
V_{IN}	Input voltage on FT and FTf pins(2)		- 0.3	5.5	V
	Input voltage on TTa pins		- 0.3	V_{DDA} + 0.3	
	Input voltage on TC pins on SDADCx channels inputs(3)		- 0.3	V_{DDSDx} + 0.3	
	Input voltage on BOOT0 pin		0	5.5	
	Input voltage on any other pin		- 0.3	V_{DD} + 0.3	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP100		434	mW
		LQFP64		444	
		LQFP48		364	
		BGA100		338	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(5)	–40	125	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(3)	PDR hysteresis			40		mV
$t_{RSTTEMPO}$(3)	POR reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD}, V_{DDA} and V_{DDSD12} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
IDD(PVD)(2)	PVD current consumption			0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 26. Embedded internal reference voltage calibration values

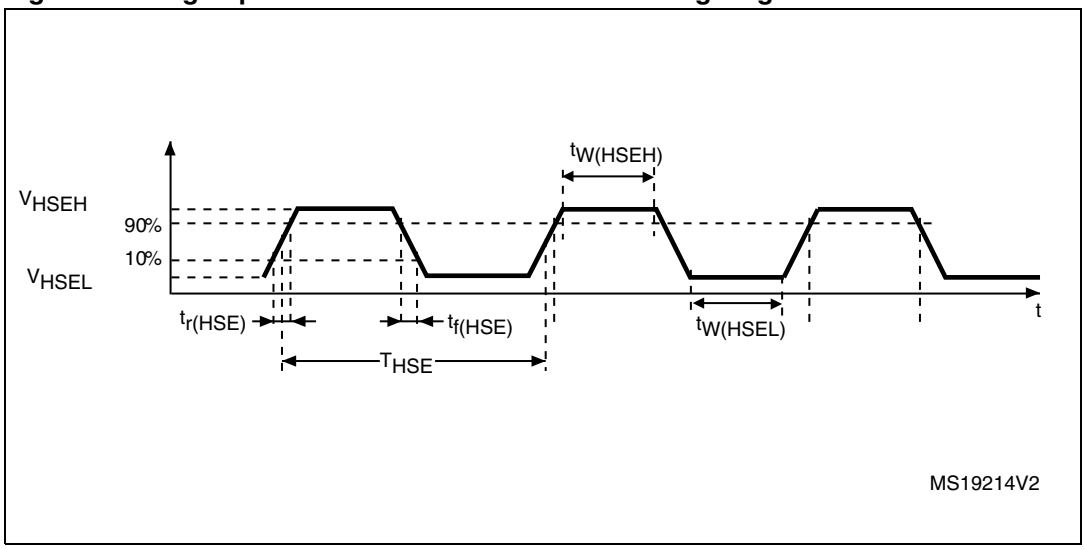
Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

Table 27. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.21	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	
$T_{S\_vrefint}$(2)	ADC sampling time when reading the internal reference voltage		17.1	-	-	µs
V_{REFINT_s}(3)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-		10	mV
T_{Coeff}(3)	Temperature coefficient		-		100	ppm/°C
t_{START}(3)	Startup time		-		10	µs

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 39. Low-speed external user clock characteristics

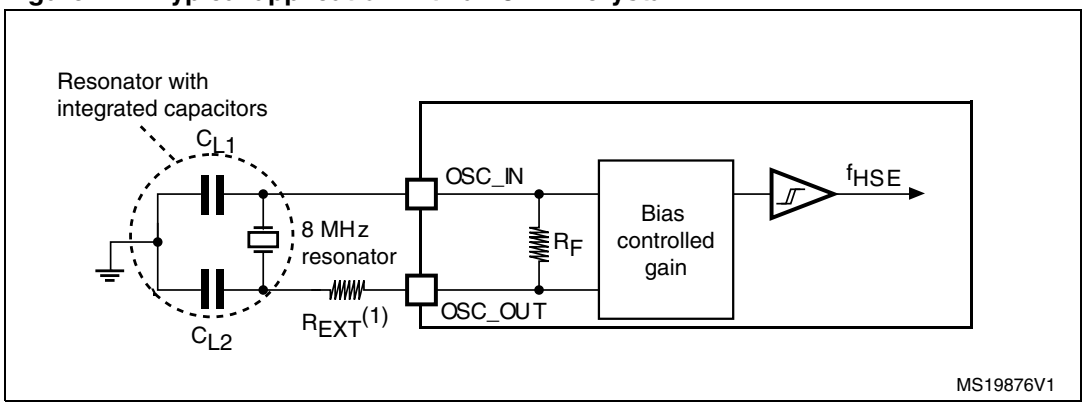
Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time				50	

1. Guaranteed by design, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*.

Output voltage levels

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 53. Output voltage characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (4)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(2)	Output low level voltage for a FTf I/O pins in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (the I/O ground pin is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O ground pin is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
5. Data based on design simulation.

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- PB2, PB10 and PE7 to PE15 I/O pins are powered from VDDSD12.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from VDDSD3. All I/O pin ground is internally connected to V_{SS}.

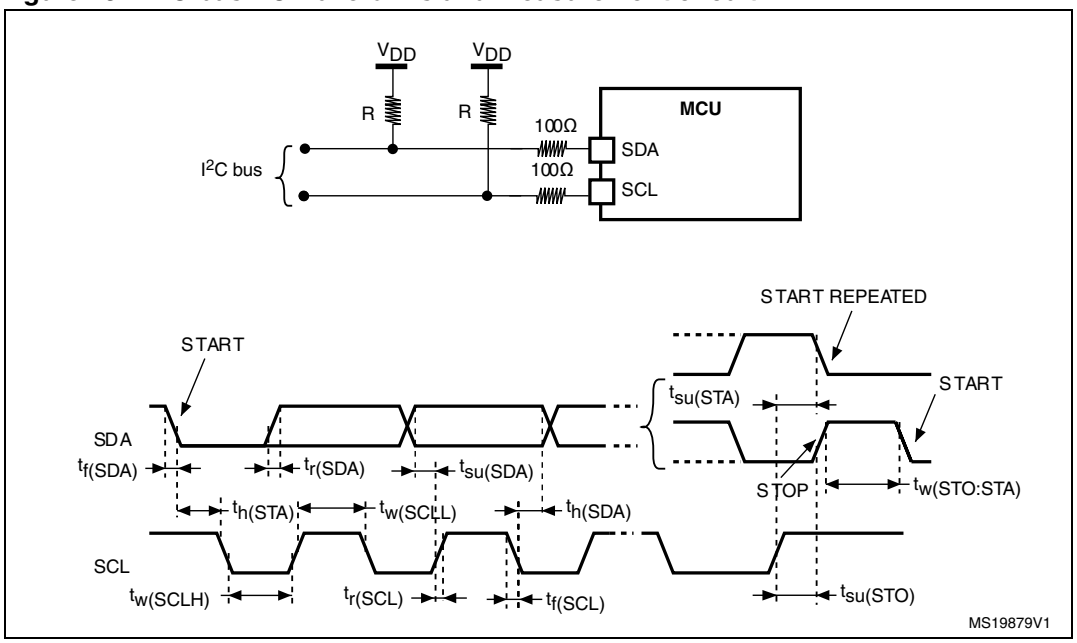
V_{DD} mentioned in the Table 53 represents power voltage for a given I/O pin (VDD or VDDSD12 or VDDSD3).

Table 57. I^2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 23. I^2C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

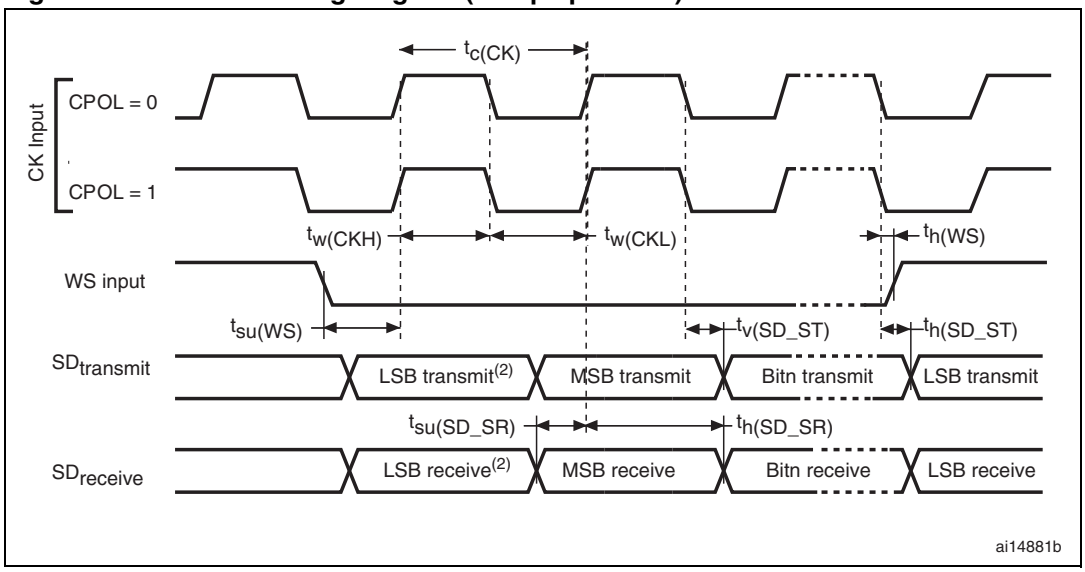
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$ (1)	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$ (1)	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	2Tpclk		ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	4Tpclk		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5.5		
		Slave mode	6.5		
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5		
$t_{h(SI)}$ (1)		Slave mode	5		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		39	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4		

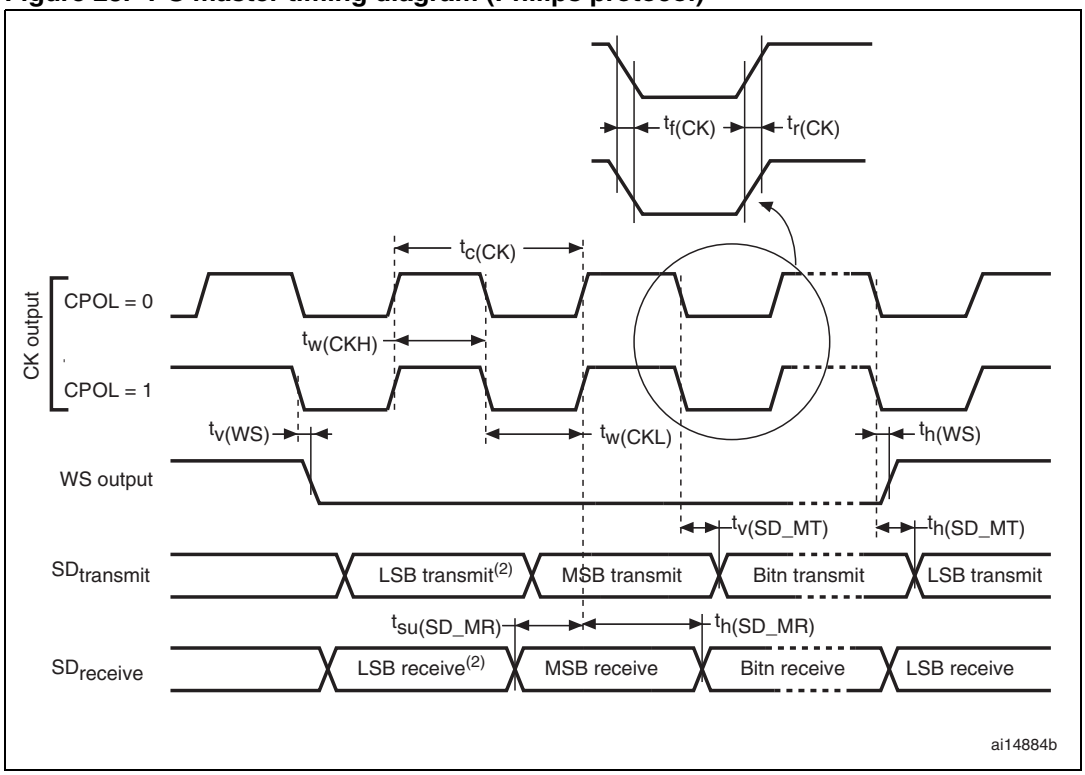
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 27. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 28. I²S master timing diagram (Philips protocol)(1)

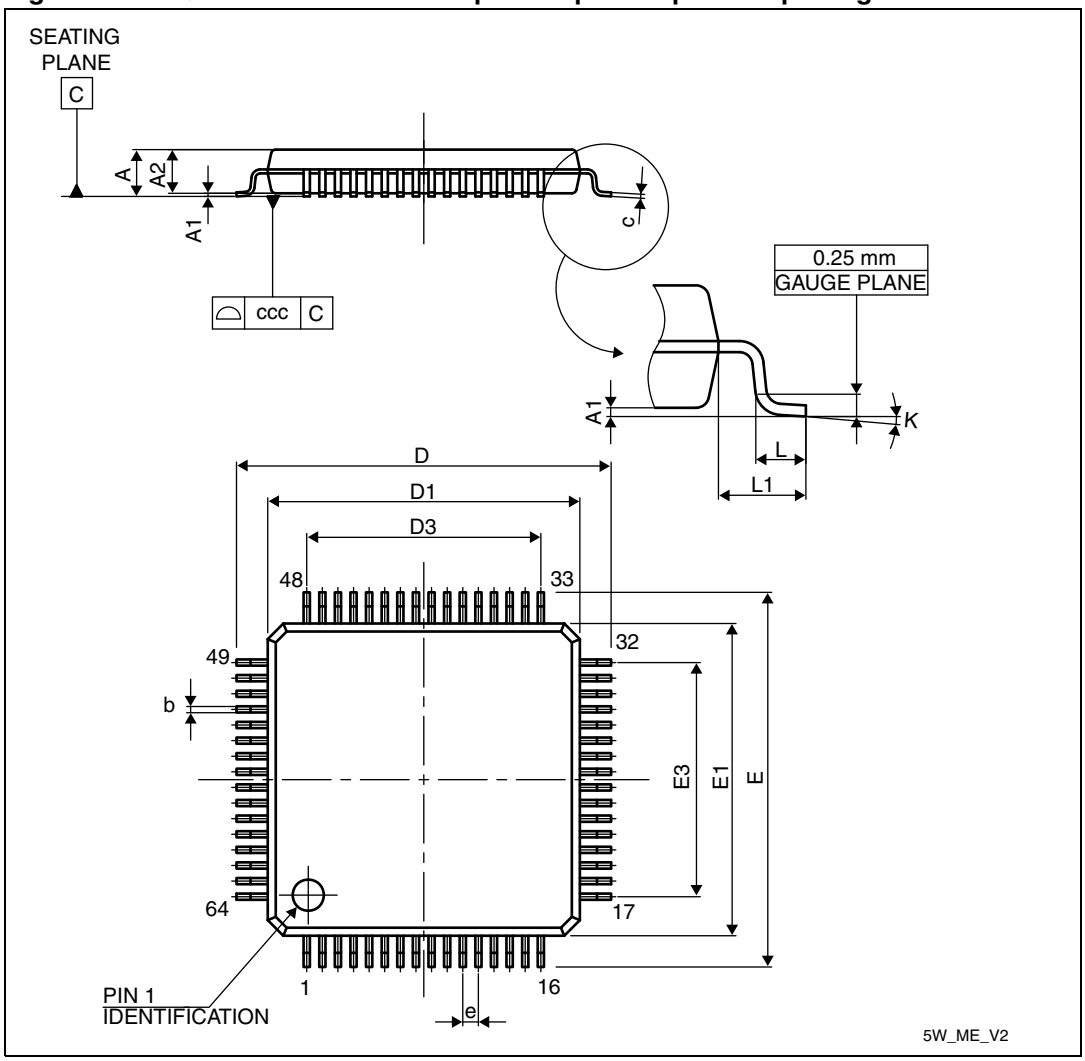


1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
I_{DDSDx}	Supply current (V_{DDSDx} = 3.3 V)	Fast mode (f_{ADC} = 6 MHz)		800	1200	µA	
		Slow mode (f_{ADC} = 1.5 MHz)			600		
		Standby			200		
		Power down			2.5		
		SD_ADC off			1		
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{SSA}		V_{REFSD+} /gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{SSA}		V_{REFSD+} /gain/2		
		Differential mode	V_{SSA}		V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	$-V_{REFSD+}$/ gain/2		V_{REFSD+}/ gain/2		Differential voltage between AINP and AINN
f_S	Sampling rate	Slow mode (f_{ADC} = 1.5 MHz)		4.166		kHz	f_{ADC}/360
		Slow mode one channel only (f_{ADC} = 1.5 MHz)		12.5			f_{ADC}/120
		Fast mode multiplexed channel (f_{ADC} = 6 MHz)		16.66			f_{ADC}/360
		Fast mode one channel only (f_{ADC} = 6 MHz)		50			f_{ADC}/120
t_{CONV}	Conversion time			1/fs		s	
Rain	Analog input impedance	One channel, gain = 0.5, f_{ADC} = 1.5 MHz		540		kΩ	see reference manual for detailed description
		One channel, gain = 0.5, f_{ADC} = 6 MHz		135			
		One channel, gain = 8, f_{ADC} = 6 MHz		47			
t_{CALIB}	Calibration time	f_{ADC} = 6 MHz, one offset calibration		5120		µs	30720/f_{ADC}
t_{STAB}	Stabilization time	From power down f_{ADC} = 6 MHz		100		µs	600/f_{ADC}, 75/f_{ADC} if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	f_{ADC} = 6 MHz		50		µs	300/f_{ADC}
		f_{ADC} = 1.5 MHz		50			75/f_{ADC} if SLOWCK = 1

Figure 36. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline

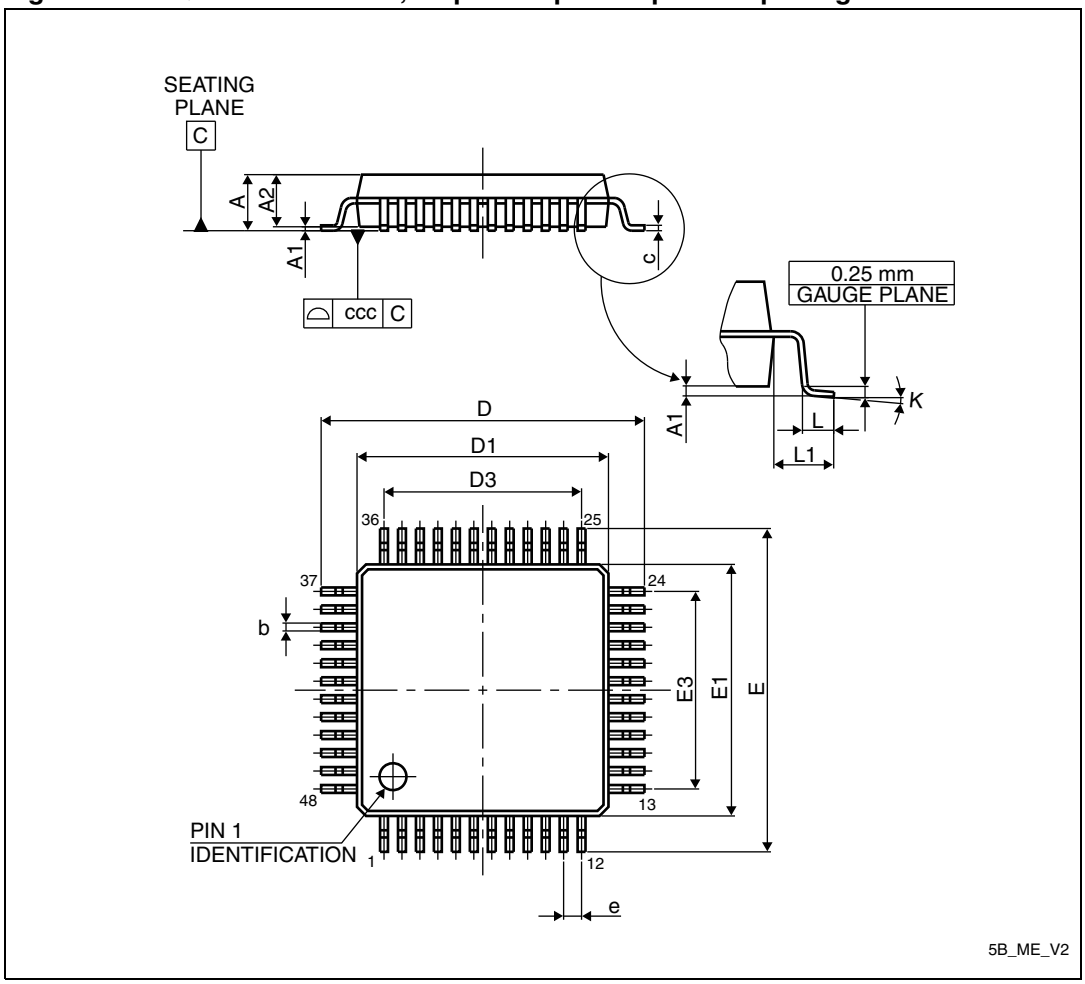


1. Drawing is not to scale.

Table 78. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3		7.50			0.2953	

Figure 38. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3		5.50			0.2165	
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3		5.50			0.2165	

Table 82. Document revision history

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 30: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F37x I2C implementation* Added *Table 8: STM32F37x USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F37x BGA100 pinout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F37x pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F37x pin definitions* Modified "x_CK" occurences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Table 9: Power supply scheme* Added Caution after *Table 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.2.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*