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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f372vct6

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3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins, and can be 2.0 to 3.6 V.
- V_{DDA} = 2.0 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR, without the need for an external reset circuit. The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F37x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
11	G2			PF10	I/O	FT	(1)		
12	F1	5	5	PF0 - OSC_IN	I/O	FTf		I2C2_SDA	OSC_IN
13	G1	6	6	PF1 - OSC_OUT	I/O	FTf		I2C2_SCL	OSC_OUT
14	H2	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
15	H1	8		PC0	I/O	TTa	(1)	TIM5_CH1_ETR	ADC_IN10
16	J2	9		PC1	I/O	TTa	(1)	TIM5_CH2	ADCIN11
17	J3	10		PC2	I/O	TTa	(1)	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11		PC3	I/O	TTa	(1)	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1			PF2	I/O	FT	(1)	I2C2_SMBA	
20	K1	12	8	VSSA/VREF-	S			Analog ground	
			9	VDDA/VREF+	S		(1)	Analog power supply / Reference voltage for ADC, COMP, DAC	
21	M1	13		VDDA	S		(1)	Analog power supply	
22	L1	17		VREF+	S		(1)	Reference voltage for ADC, COMP, DAC	
23	L2	14	10	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT	RTC_ TAMPER2, WKUP1, ADC_IN0, COMP1_INM
24	M2	15	11	PA1	I/O	TTa		SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2,	ADC_IN1, COMP1_INP, RTC_REF_CLK_IN
25	K3	16	12	PA2	I/O	TTa		COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3	ADC_IN2, COMP2_INM
26	L3	18	13	PA3	I/O	TTa		SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4	ADC_IN3, COMP2_INP
27	E3			PF4	I/O	FT	(1)		
28	H3	19	17	VDD_2	S			Digital power supply	

Table 11. STM32F37x pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
43	L9			PE12	I/O	TC	(2) (1)		SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10			PE13	I/O	TC	(2) (1)		SDADC1_AIN0M , SDADC2_AIN2P
45	M11			PE14	I/O	TC	(2) (1)		SDADC2_AIN1P, SDADC2_AIN2M
46	M12			PE15	I/O	TC	(2) (1)	USART3_RX	SDADC2_AIN0P
47	L10			PB10	I/O	TC	(2) (1)	SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	SDADC2_AIN0M
48	L11			VREFSD-	S		(1)	External reference voltage for SDADC1, SDADC2, SDADC3 (negative input)	
49	F12			VSSSD	S		(1)	SDADC1, SDADC2, SDADC3 ground	
		31	23	VSSSD/ VREFSD-	S			SDADC1, SDADC2, SDADC3 ground / External reference voltage for SDADC1, SDADC2, SDADC3 (negative input)	
50	G12			VDDSD12	S		(1)	SDADC1 and SDADC2 power supply	
		32	24	VDDSD	S			SDADC1, SDADC2, SDADC3 power supply	
51	L12			VDDSD3	S		(1)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S			External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(3)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(3)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2	SDADC3_AIN7P, SDADC3_AIN8M, RTC_REFCLKIN
55	K9	36	28	PD8	I/O	TC	(3)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8			PD9	I/O	TC	(3) (1)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12			PD10	I/O	TC	(3) (1)	USART3_CK	SDADC3_AIN4P
58	J11			PD11	I/O	TC	(3) (1)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10			PD12	I/O	TC	(3) (1)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P

Table 11. STM32F37x pin definitions (continued)

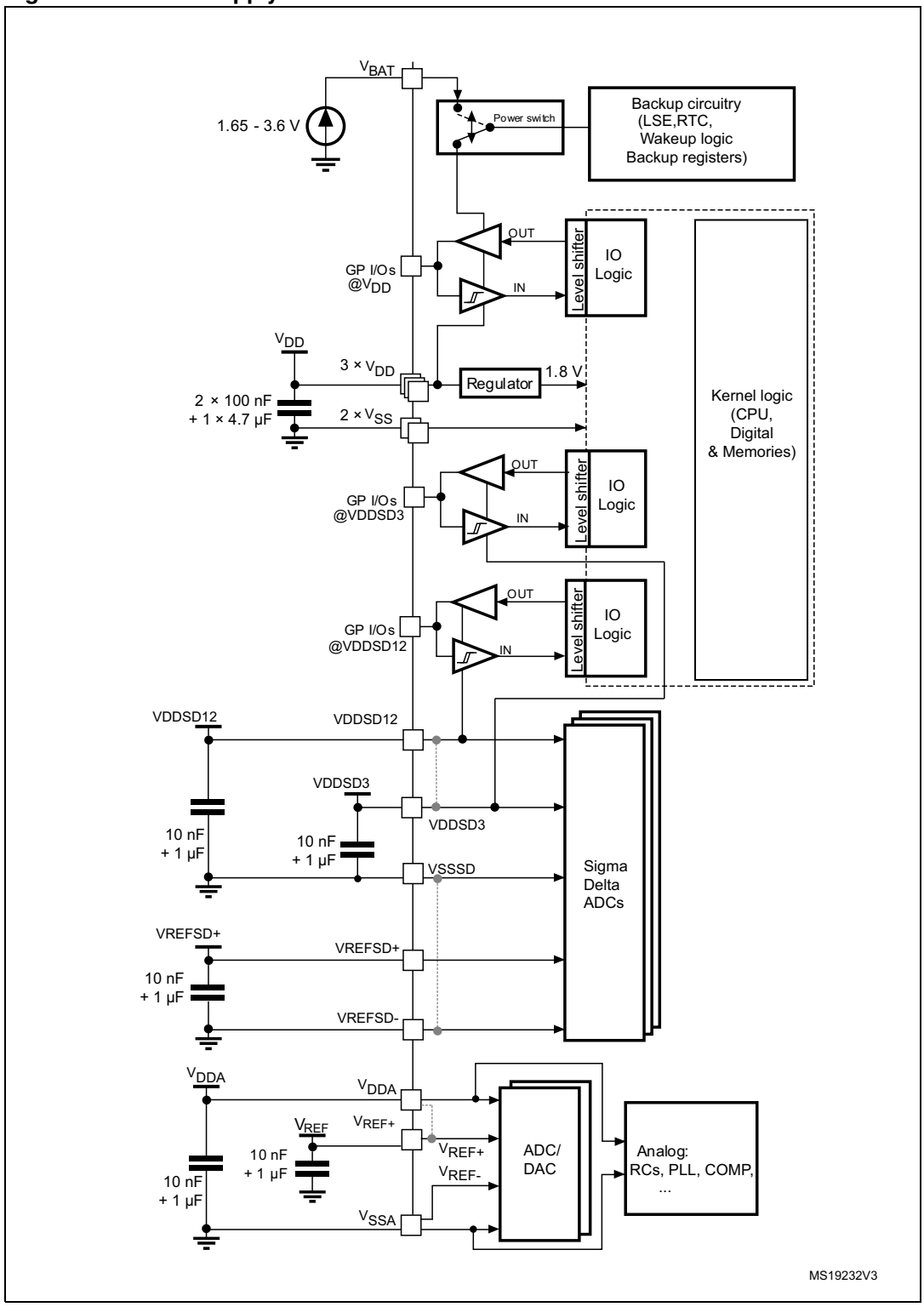
Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
73	C11	47	35	PF6	I/O	FTf		SPI1_MOSI/I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	
74	F11			VSS_3	S		(1)	Ground	
75	G11			VDD_3	S		(1)	Digital power supply	
		48	36	PF7	I/O	FTf		I2C2_SDA, USART2_CK	
76	A10	49	37	PA14	I/O	FTf		I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK	
77	A9	50	38	PA15	I/O	FTf		SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, I2C1_SCL, TIM2_CH1_ETR, TIM12_CH2, TSC_SYNC, JTDI	
78	B11	51		PC10	I/O	FT	(1)	SPI3_SCK/I2S3_CK, USART3_TX, TIM19_CH1	
79	C10	52		PC11	I/O	FT	(1)	SPI3_MISO/I2S3_MCK, USART3_RX, TIM19_CH2	
80	B10	53		PC12	I/O	FT	(1)	SPI3_MOSI/I2S3_SD, USART3_CK, TIM19_CH3	
81	C9			PD0	I/O	FT	(1)	CAN_RX, TIM19_CH4	
82	B9			PD1	I/O	FT	(1)	CAN_TX, TIM19_ETR	
83	C8	54		PD2	I/O	FT	(1)	TIM3_ETR	
84	B8			PD3	I/O	FT	(1)	SPI2_MISO/I2S2_MCK, USART2_CTS	
85	B7			PD4	I/O	FT	(1)	SPI2_MOSI/I2S2_SD, USART2_RTS	
86	A6			PD5	I/O	FT	(1)	USART2_TX	
87	B6			PD6	I/O	FT	(1)	SPI2_NSS/I2S2_WS, USART2_RX	
88	A5			PD7	I/O	FT	(1)	SPI2_SCK/I2S2_CK, USART2_CK	
89	A8	55	39	PB3	I/O	FT		SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM13_CH1, TSC_G5_IO1, JTDO-TRACESWO	

Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	JTMS-SWDIO	TIM16_CH1N	TIM5_CH4	TSC_G4_IO3		IR-OUT	SPI1_MISO/I2S1_MCK	USART3_CTS			TIM4_CH3			EVENTOUT
PA14	JTCK-SWCLK			TSC_G4_IO4	I2C1_SDA						TIM12_CH1			EVENTOUT
PA15	JTDI	TIM2_CH1_ETR		TSC_SYNC	I2C1_SCL	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS				TIM12_CH2			EVENTOUT

6.1.6 Power supply scheme

Figure 9. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(3)	PDR hysteresis			40		mV
$t_{RSTTEMPO}$(3)	POR reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD}, V_{DDA} and V_{DDSD12} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
IDD(PVD)(2)	PVD current consumption			0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33				
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4				

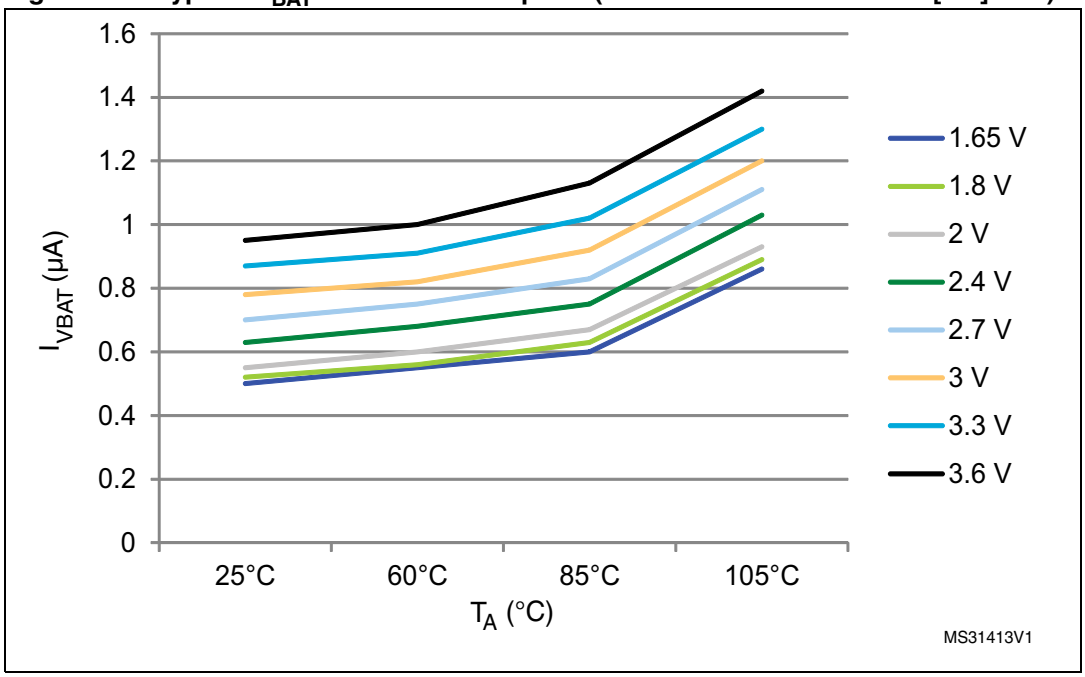
1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Data based on characterization results, not tested in production.

Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00')



Typical current consumption

The MCU is placed under the following conditions:

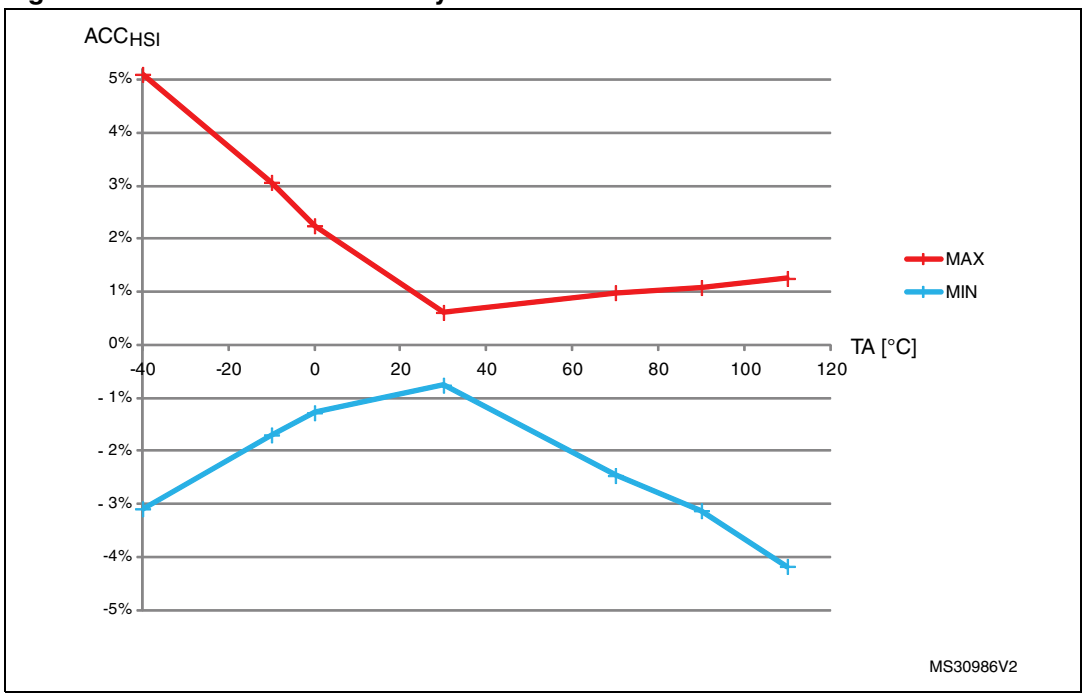
- $V_{DD} = V_{DDA} = V_{DDSD12} = V_{DDSD3} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I_{DDA}(1)(2)	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	µA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
$I_{SDADC12}$ + I_{SDADC3}	Supply currents in Run mode from V_{DDSD12} and V_{DDSD3} (SDADCs are off)		-	2.5	1	

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.
2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

Figure 16. HSI oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption		0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)		24(2)	MHz
	PLL input clock duty cycle	40(2)		60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)		72	MHz
t_{LOCK}	PLL lock time			200(2)	µs
Jitter	Cycle-to-cycle jitter			300(2)	ps

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$ (1)	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$ (1)	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	2Tpclk		ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	4Tpclk		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5.5		
		Slave mode	6.5		
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5		
$t_{h(SI)}$ (1)		Slave mode	5		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		39	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4		

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{SRC}(2)	Signal source impedance	See *Equation 1* and *Table 61* for details			50	kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					2(3)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(3)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

Equation 1: R_{SRC} max formula

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{SRC} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{SRC} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	50
239.5	17.1	50

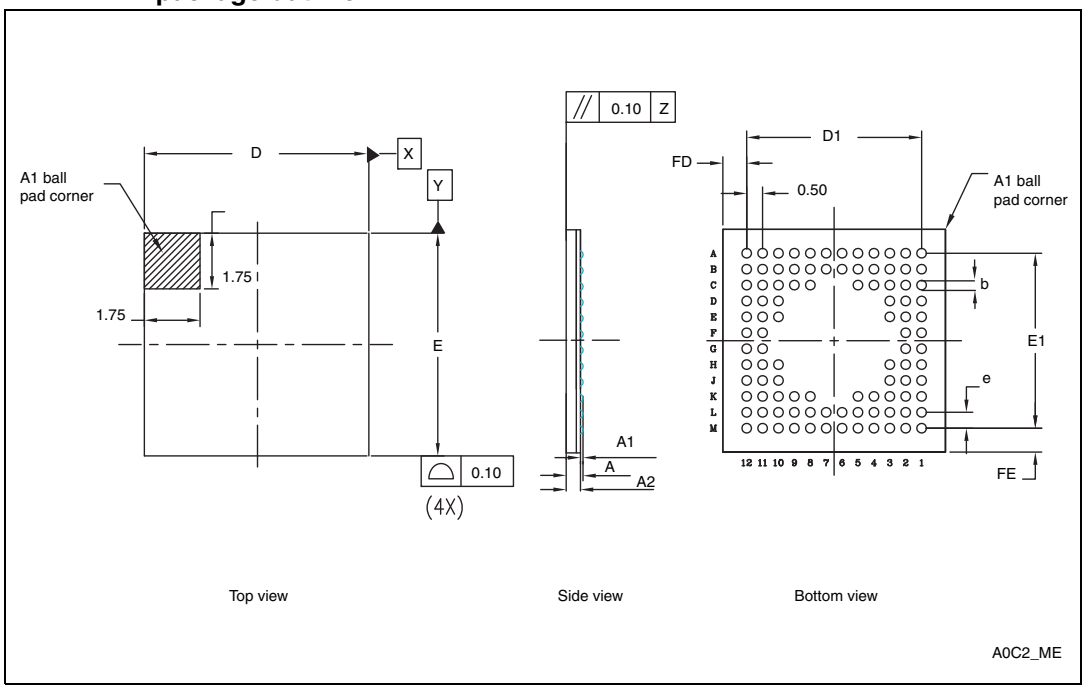
1. Guaranteed by design, not tested in production.

Table 62. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±3	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V T_A = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

Figure 33. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline



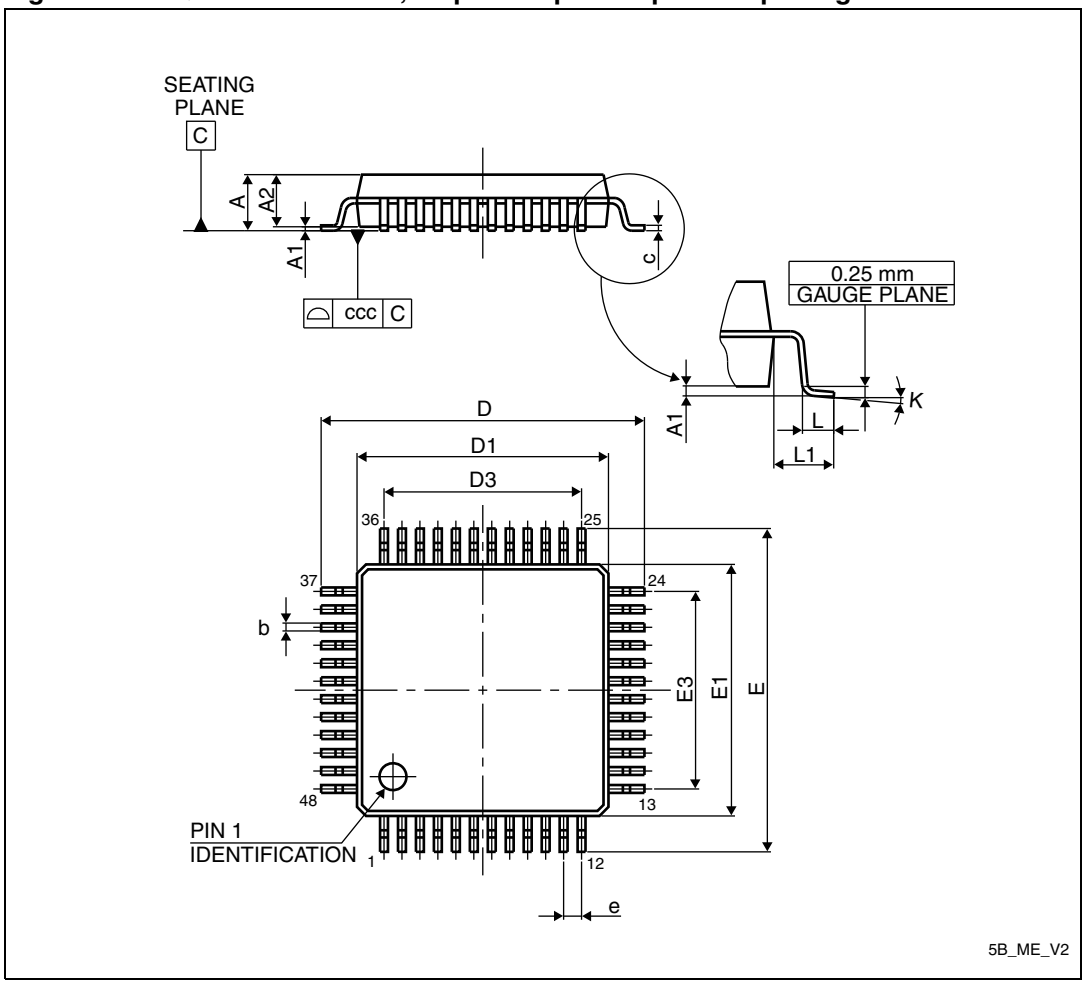
1. Drawing is not to scale.

Table 76. UFBGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.46	0.53	0.6	0.0181	0.0209	0.0236
A1	0.06	0.08	0.1	0.0024	0.0031	0.0039
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D		7			0.2756	
D1		5.5			0.2165	
E		7			0.2756	
E1		5.5			0.2165	
e		0.5			0.0197	
FD		0.75			0.0295	
FE		0.75			0.0295	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3		5.50			0.2165	
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3		5.50			0.2165	

Table 82. Document revision history

Date	Revision	Changes
21-Dec-2012	3	Updated *Table 2: Device overview*, capacitive sensing channels peripheral added. Updated *Table 3: Capacitive sensing GPIOs available on STM32F37x devices* Updated *Section 3.19: Inter-integrated circuit interface (I2C)* Updated the function names in *Table 11: STM32F37x pin definitions* Updated *Table 20: Current characteristics* Updated *Table 22: General operating conditions* Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Updated *Table 32: Typical and maximum current consumption from VBAT supply* Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')* Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 35: Switching output I/O current consumption* Added *Table 36: Peripheral current consumption* *Figure 16: HSI oscillator accuracy characterization results* Updated *Section 6.3.6: Wakeup time from low-power mode* Updated *Table 37: Low-power mode wakeup timings* Updated *Table 47: EMS characteristics* Updated *Table 51: I/O current injection susceptibility* Updated *Table 52: I/O static characteristics* Updated *Figure 17: TC and TTa I/O input characteristics - CMOS port*, *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 19: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port* Updated *Table 53: Output voltage characteristics* Updated *Table 55: NRST pin characteristics* Updated *Table 54: I/O AC characteristics* Updated *Table 63: DAC characteristics* Updated *Table 74: SDADC characteristics* Updated *Figure 7: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 9: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 11: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline* Updated *Table 21: LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 22: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 23: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data* Added *Figure 16: HSI oscillator accuracy characterization results*