E·XFL

Renesas Electronics America Inc - DF38524HV Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38524hv

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2.4.2 Basic Instruction Formats

H8/300H CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op), a register field (r), an effective address extension (EA), and a condition field (cc).

Figure 2.7 shows examples of instruction formats.

(1) Operation Field

Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.

(2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension

8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A24-bit address or displacement is treated as a 32-bit data in which the first 8 bits are 0 (H'00).

(4) Condition Field

Specifies the branching condition of Bcc instructions.

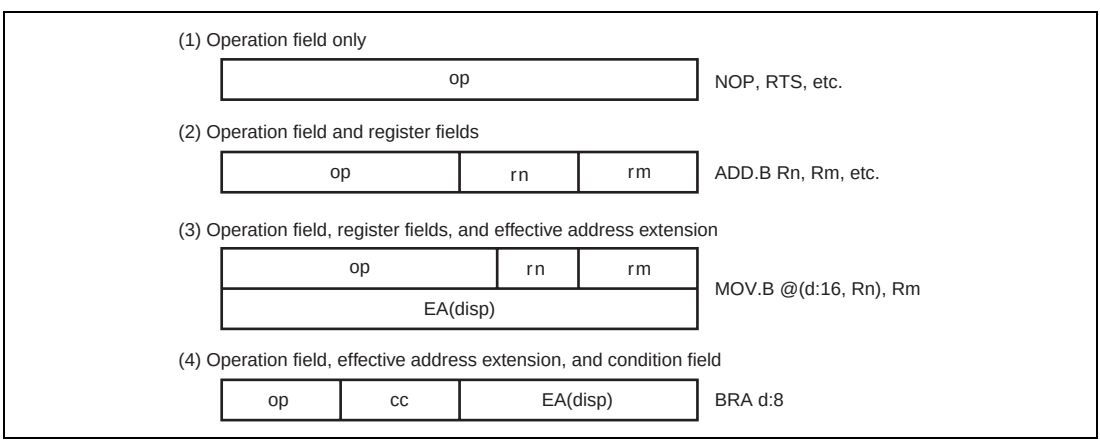


Figure 2.7 Instruction Formats

Bit 7 SUBSTP	Description	
0	Subclock oscillator operates	(initial value)
1	Subclock oscillator stopped	

Bit 6—Reserved

This bit is reserved. It is always read as 0 and cannot be written to.

Bits 5 to 3—Reserved

These bits are read/write enabled reserved bits.

Bit 2—IRQAEC Flag (IRQAECF)

This bit indicates the IRQAEC pin input level set during resets.

Bit 2 IRQAECF	Description
0	IRQAEC pin set to GND during resets
1	IRQAEC pin set to V_{CC} during resets

Bit 1—OSC Flag (OSCF)

This bit indicates the oscillator operating with the system clock pulse generator.

Bit 1 OSCF	Description
0	System clock oscillator operating (on-chip oscillator stopped)
1	On-chip oscillator operating (system clock oscillator stopped)

Bit 0—Reserved

This bit is reserved. Never write 1 to this bit, as it can cause the LSI to malfunction.

6.2.3 Block Configuration

Figure 6.2 shows the block configuration of the flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. In versions with 32 Kbytes of flash memory, the flash memory is divided into 1 Kbyte × 4 blocks and 28 Kbytes × 1 block. In versions with 16 Kbytes of flash memory, the flash memory is divided into 1 Kbyte × 4 blocks and 12 Kbytes × 1 block. Erasing is performed in these units. Programming is performed in 128-byte units starting from an address with lower eight bits H'00 or H'80.

	H'0000	H'0001	H'0002	← Programming unit: 128 bytes →	H'007F
Erase unit	H'0080	H'0081	H'0082		H'00FF
1 Kbyte					
	H'0380	H'0381	H'0382		H'03FF
	H'0400	H'0401	H'0402	← Programming unit: 128 bytes →	H'047F
Erase unit	H'0480	H'0481	H'0482		H'04FF
1 Kbyte					
	H'0780	H'0781	H'0782		H'07FF
	H'0800	H'0801	H'0802	← Programming unit: 128 bytes →	H'087F
Erase unit	H'0880	H'0881	H'0882		H'08FF
1 Kbyte					
	H'0B80	H'0B81	H'0B82		H'0BFF
	H'0C00	H'0C01	H'0C02	← Programming unit: 128 bytes →	H'0C7F
Erase unit	H'0C80	H'0C81	H'0C82		H'0CFF
1 Kbyte					
	H'0F80	H'0F81	H'0F82		H'0FFF
	H'1000	H'1001	H'1002	← Programming unit: 128 bytes →	H'107F
Erase unit	H'1080	H'1081	H'1082		H'10FF
28 Kbytes					
	H'7F80	H'7F81	H'7F82		H'7FFF

Figure 6.2(1) Block Configuration of 32-Kbyte Flash Memory

(3) Port Pull-Up Control Register 3 (PUCR3)

Bit	7	6	5	4	3	2	1	0
	$PUCR3_7$	$PUCR3_6$	$PUCR3_5$	$PUCR3_4$	$PUCR3_3$	$PUCR3_2$	$PUCR3_1$	$PUCR3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PUCR3 controls whether the MOS pull-up of each of the port 3 pins $P3_7$ to $P3_0$ is on or off. When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR3 is initialized to H'00.

(4) Port Mode Register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	WDCKS	NCS	IRQ0
Initial value	1	1	0	1	1	0	0	0
Read/Write	—	—	R/W	—	—	R/W	R/W	R/W

PMR2 is an 8-bit read/write register. It controls whether the PMOS transistor internal to $P3_5$ is on or off, the selection of the watchdog timer clock, the selection of TMIG noise cancellation, and switching of the $P4_3/\overline{IRQ_0}$ pin functions.

Upon reset, PMR2 is initialized to H'D8.

This section only deals with the bit that controls whether the PMOS transistor internal to pin $P3_5$ is on or off. For the functions of the other bits, see the descriptions of port 1 (WDCKS and NCS) and port 4 (IRQ0).

Bit 5—Pin $P3_5$ PMOS Transistor Control (POF1)

This bit selects whether the PMOS transistor of the output buffer for pin $P3_5$ is on or off.

Bit 5 POF1	Description
0	CMOS output (initial value)
1	NMOS open-drain output

Note: The pin is an NMOS open-drain output when this bit is set to 1 and $P3_5$ is an output.

Bits 3 to 0—Internal Clock Select (TMA3 to TMA0)

Bits 3 to 0 select the clock input to TCA. The selection is made as follows.

				Description	
Bit 3 TMA3	**Bit 2 TMA2**	**Bit 1 TMA1**	**Bit 0 TMA0**	**Prescaler and Divider Ratio or Overflow Period**	**Function**
0	0	0	0	PSS, ϕ/8192 (initial value)	Interval timer
			1	PSS, ϕ/4096	
		1	0	PSS, ϕ/2048	
			1	PSS, ϕ/512	
	1	0	0	PSS, ϕ/256	
			1	PSS, ϕ/128	
		1	0	PSS, ϕ/32	
			1	PSS, ϕ/8	
1	0	0	0	PSW, 1 s	Clock time base (when using 32.768 kHz)
			1	PSW, 0.5 s	
		1	0	PSW, 0.25 s	
			1	PSW, 0.03125 s	
	1	0	0	PSW and TCA are reset	
			1		
		1	0		
			1		

9.2.3 Timer Operation

(1) Interval Timer Operation

When bit TMA3 in timer mode register A (TMA) is cleared to 0, timer A functions as an 8-bit interval timer.

Upon reset, TCA is cleared to H'00 and bit TMA3 is cleared to 0, so up-counting and interval timing resume immediately. The clock input to timer A is selected by bits TMA2 to TMA0 in TMA; any of eight internal clock signals output by prescaler S can be selected.

After the count value in TCA reaches H'FF, the next clock signal input causes timer A to overflow, setting bit IRRTA to 1 in interrupt request register 1 (IRR1). If IENTA = 1 in interrupt enable register 1 (IENR1), a CPU interrupt is requested.*

At overflow, TCA returns to H'00 and starts counting up again. In this mode timer A functions as an interval timer that generates an overflow output at intervals of 256 input clock pulses.

Note: * For details on interrupts, see section 3.3, Interrupts.

(2) Real-Time Clock Time Base Operation

When bit TMA3 in TMA is set to 1, timer A functions as a real-time clock time base by counting clock signals output by prescaler W. The overflow period of timer A is set by bits TMA1 and TMA0 in TMA. A choice of four periods is available. In time base operation (TMA3 = 1), setting bit TMA2 to 1 clears both TCA and prescaler W to their initial values of H'00.

9.6.2 Register Descriptions

(1) Timer Control/Status Register W (TCSRW)

Bit	7	6	5	4	3	2	1	0
	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	B0WI	WRST
Initial value	1	0	1	0	1	1	1	0
Read/Write	R	(R/W)*	R	(R/W)*	R	(R/W)*	R	(R/W)*

Note: * Write is enabled only under certain conditions, which are given in the descriptions of the individual bits.

TCSRW is an 8-bit read/write register that controls write access to TCW and TCSRW itself, controls watchdog timer operations, and indicates operating status.

Bit 7—Bit 6 Write Disable (B6WI)

Bit 7 controls the writing of data to bit 6 in TCSRW.

Bit 7 B6WI	Description	
0	Bit 6 is write-enabled	
1	Bit 6 is write-protected	(initial value)

This bit is always read as 1. Data written to this bit is not stored.

Bit 6—Timer Counter W Write Enable (TCWE)

Bit 6 controls the writing of data to TCW.

Bit 6 TCWE	Description	
0	Data cannot be written to TCW	(initial value)
1	Data can be written to TCW	

Bit 2—Transmit End (TEND)

Bit 2 indicates that bit TDRE is set to 1 when the last bit of a transmit character is sent.

Bit 2 is a read-only bit and cannot be modified.

Bit 2 TEND	Description
0	Transmission in progress Clearing conditions: After reading TDRE = 1, cleared by writing 0 to TDRE When data is written to TDR by an instruction
1	Transmission ended (initial value) Setting conditions: When bit TE in SCR3 is cleared to 0 When bit TDRE is set to 1 when the last bit of a transmit character is sent

Bit 1—Reserved (MPBR)

Bit 1 is read-only and reserved. It cannot be written to.

Bit 0— Reserved (MPBT)

Bit 0 is reserved. The write value should always be 0.

10.2.8 Bit Rate Register (BRR)

Bit	7	6	5	4	3	2	1	0
	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRR is an 8-bit register that designates the transmit/receive bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 of the serial mode register (SMR).

BRR can be read or written by the CPU at any time.

BRR is initialized to H'FF upon reset, and in standby, module standby, or watch mode.

Table 10.3 shows examples of BRR settings in asynchronous mode. The values shown are for active (high-speed) mode.

10.2.10 Serial Port Control Register (SPCR)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	—	0	0	—	—
Read/Write	—	—	R/W	W	R/W	R/W	W	W

SPCR is an 8-bit readable/writable register that performs RXD_{32} and TXD_{32} pin input/output data inversion switching.

Bits 7 and 6—Reserved

Bits 7 and 6 are reserved; they are always read as 1 and cannot be modified.

Bit 5—$P4_2$/TXD_{32} Pin Function Switch (SPC32)

This bit selects whether pin $P4_2$/TXD_{32} is used as $P4_2$ or as TXD_{32}.

Bit 5 SPC32	Description	
0	Functions as $P4_2$ I/O pin	(initial value)
1	Functions as TXD_{32} output pin*	

Note: * Set the TE bit in SCR3 after setting this bit to 1.

Bit 4—Reserved

Bit 4 is reserved; only 0 can be written to this bit.

Bit 3—TXD_{32} Pin Output Data Inversion Switch

Bit 3 specifies whether or not TXD_{32} pin output data is to be inverted.

Bit 3 SCINV3	Description	
0	TXD_{32} output data is not inverted	(initial value)
1	TXD_{32} output data is inverted	

12.3 Operation

12.3.1 A/D Conversion Operation

The A/D converter operates by successive approximations, and yields its conversion result as 10-bit data.

A/D conversion begins when software sets the A/D start flag (bit ADSF) to 1. Bit ADSF keeps a value of 1 during A/D conversion, and is cleared to 0 automatically when conversion is complete.

The completion of conversion also sets bit IRRAD in interrupt request register 2 (IRR2) to 1. An A/D conversion end interrupt is requested if bit IENAD in interrupt enable register 2 (IENR2) is set to 1.

If the conversion time or input channel needs to be changed in the A/D mode register (AMR) during A/D conversion, bit ADSF should first be cleared to 0, stopping the conversion operation, in order to avoid malfunction.

12.3.2 Start of A/D Conversion by External Trigger Input

The A/D converter can be made to start A/D conversion by input of an external trigger signal. External trigger input is enabled at pin $\overline{\text{ADTRG}}$ when bit IRQ4 in PMR1 is set to 1 and bit TRGE in AMR is set to 1. Then when the input signal edge designated in bit IEG4 of interrupt edge select register (IEGR) is detected at pin $\overline{\text{ADTRG}}$, bit ADSF in ADSR will be set to 1, starting A/D conversion.

Figure 12.2 shows the timing.

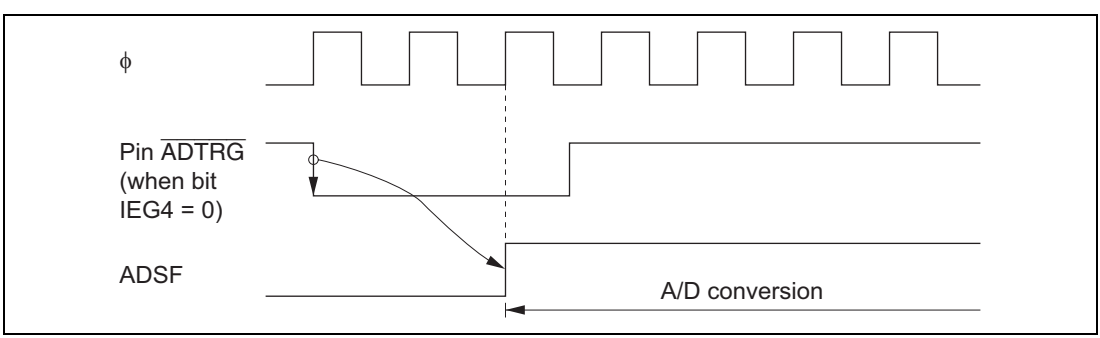


Figure 12.2 External Trigger Input Timing

Bits 3 to 0—Segment Driver Select 3 to 0 (SGS3 to SGS0)

Bits 3 to 0 select the segment drivers to be used.

				Function of Pins SEG_{32} to SEG_1								
Bit 3 SGS3	**Bit 2 SGS2**	**Bit 1 SGS1**	**Bit 0 SGS0**	**SEG_{32} to SEG_{29}**	**SEG_{28} to SEG_{25}**	**SEG_{24} to SEG_{21}**	**SEG_{20} to SEG_{17}**	**SEG_{16} to SEG_{13}**	**SEG_{12} to SEG_9**	**SEG_8 to SEG_5**	**SEG_4 to SEG_1**	**Notes**
0	0	0	0	Port	Port	Port	Port	Port	Port	Port	Port	(Initial value)
			1	Port	Port	Port	Port	Port	Port	Port	SEG	
		1	0	Port	Port	Port	Port	Port	Port	SEG	SEG	
			1	Port	Port	Port	Port	Port	SEG	SEG	SEG	
	1	0	0	Port	Port	Port	Port	SEG	SEG	SEG	SEG	
			1	Port	Port	Port	SEG	SEG	SEG	SEG	SEG	
		1	0	Port	Port	SEG	SEG	SEG	SEG	SEG	SEG	
			1	Port	SEG	SEG	SEG	SEG	SEG	SEG	SEG	
1	0	0	0	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	
			1	SEG	SEG	SEG	SEG	SEG	SEG	SEG	Port	
		1	0	SEG	SEG	SEG	SEG	SEG	SEG	Port	Port	
			1	SEG	SEG	SEG	SEG	SEG	Port	Port	Port	
	1	0	0	SEG	SEG	SEG	SEG	Port	Port	Port	Port	
			1	SEG	SEG	SEG	Port	Port	Port	Port	Port	
		1	0	SEG	SEG	Port	Port	Port	Port	Port	Port	
			1	SEG	Port	Port	Port	Port	Port	Port	Port	

Item	Symbol	Applicable Pins	Values Min	Values Typ	Values Max	Unit	Test Condition	Notes
Active mode supply current	I_{OPE2}	V_{CC}	—	0.2	—	mA	Active (medium-speed) mode V_{CC} = 2.7 V, f_{OSC} = 2 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.5	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.4	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 2 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.8	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.6	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 4 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.9	—			*2 *3 *4
			—	0.9	3.0		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz, ϕ_{OSC}/128	*1 *3 *4
			—	1.2	3.0			*2 *3 *4

17.4 Output Load Circuit

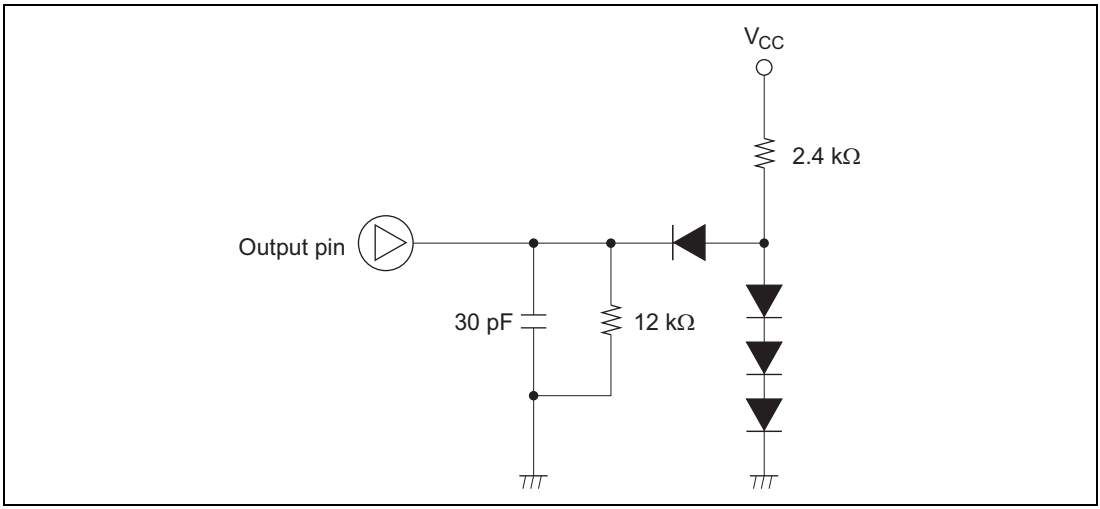
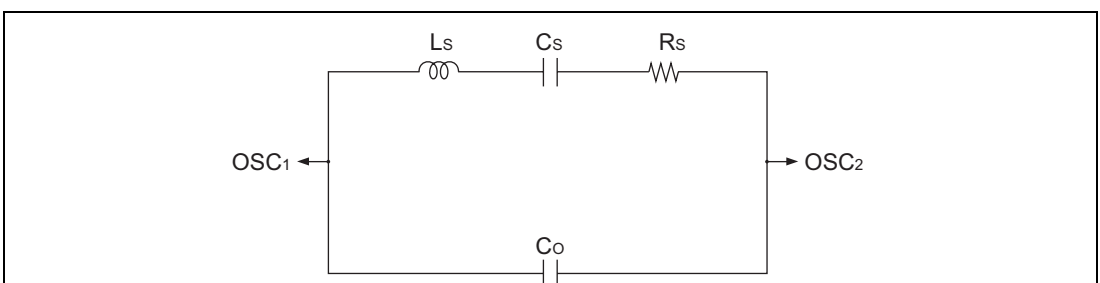


Figure 17.7 Output Load Condition

17.5 Resonator Equivalent Circuit



Crystal Resonator Parameters

Frequency (MHz)	4	4.193	10
R_S (max)	100 Ω	100 Ω	30 Ω
C_O (max)	16 pF	16 pF	16 pF

Ceramic Resonator Parameters

Frequency (MHz)	2	4	10
R_S (max)	18.3 Ω	6.8 Ω	4.6 Ω
C_O (max)	36.94 pF	36.72 pF	32.31 pF

Figure 17.8 Resonator Equivalent Circuit (1)

2. Arithmetic Instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
ADD	ADD.B #xx:8, Rd	B	2									Rd8+#xx:8 → Rd8	—	↕	↕	↕	↕	↕	2	
	ADD.B Rs, Rd	B		2								Rd8+Rs8 → Rd8	—	↕	↕	↕	↕	↕	2	
	ADD.W #xx:16, Rd	W	4									Rd16+#xx:16 → Rd16	—	(1)	↕	↕	↕	↕	4	
	ADD.W Rs, Rd	W		2								Rd16+Rs16 → Rd16	—	(1)	↕	↕	↕	↕	2	
	ADD.L #xx:32, ERd	L	6									ERd32+#xx:32 → ERd32	—	(2)	↕	↕	↕	↕	6	
	ADD.L ERs, ERd	L		2								ERd32+ERs32 → ERd32	—	(2)	↕	↕	↕	↕	2	
ADDX	ADDX.B #xx:8, Rd	B	2									Rd8+#xx:8 +C → Rd8	—	↕	↕	(3)	↕	↕	2	
	ADDX.B Rs, Rd	B		2								Rd8+Rs8 +C → Rd8	—	↕	↕	(3)	↕	↕	2	
ADDS	ADDS.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	—	—	—	—	2	
	ADDS.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	—	—	—	—	2	
	ADDS.L #4, ERd	L		2								ERd32+4 → ERd32	—	—	—	—	—	—	2	
INC	INC.B Rd	B		2								Rd8+1 → Rd8	—	—	↕	↕	↕	—	2	
	INC.W #1, Rd	W		2								Rd16+1 → Rd16	—	—	↕	↕	↕	—	2	
	INC.W #2, Rd	W		2								Rd16+2 → Rd16	—	—	↕	↕	↕	—	2	
	INC.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	↕	↕	↕	—	2	
	INC.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	↕	↕	↕	—	2	
DAA	DAA Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	—	2	
SUB	SUB.B Rs, Rd	B		2								Rd8–Rs8 → Rd8	—	↕	↕	↕	↕	↕	2	
	SUB.W #xx:16, Rd	W	4									Rd16–#xx:16 → Rd16	—	(1)	↕	↕	↕	↕	4	
	SUB.W Rs, Rd	W		2								Rd16–Rs16 → Rd16	—	(1)	↕	↕	↕	↕	2	
	SUB.L #xx:32, ERd	L	6									ERd32–#xx:32 → ERd32	—	(2)	↕	↕	↕	↕	6	
	SUB.L ERs, ERd	L		2								ERd32–ERs32 → ERd32	—	(2)	↕	↕	↕	↕	2	
SUBX	SUBX.B #xx:8, Rd	B	2									Rd8–#xx:8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
	SUBX.B Rs, Rd	B		2								Rd8–Rs8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
SUBS	SUBS.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	—	—	—	—	2	
	SUBS.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	—	—	—	—	2	
	SUBS.L #4, ERd	L		2								ERd32–4 → ERd32	—	—	—	—	—	—	2	
DEC	DEC.B Rd	B		2								Rd8–1 → Rd8	—	—	↕	↕	↕	—	2	
	DEC.W #1, Rd	W		2								Rd16–1 → Rd16	—	—	↕	↕	↕	—	2	
	DEC.W #2, Rd	W		2								Rd16–2 → Rd16	—	—	↕	↕	↕	—	2	

Table A.2 Operation Code Map (3)

Instruction code:

1st byte		2nd byte		3rd byte		4th byte	
AH	AL	BH	BL	CH	CL	DH	DL

Instruction when most significant bit of DH is 0.

Instruction when most significant bit of DH is 1.

CL / AH ALBH BLCH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01406										LDC / STC		LDC / STC		LDC / STC		LDC / STC
01C05	MULXS		MULXS													
01D05		DIVXS		DIVXS												
01F06					OR	XOR	AND									
7Cr06*1				BTST												
7Cr07*1				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD								
7Dr06*1	BSET	BNOT	BCLR					BST / BIST								
7Dr07*1	BSET	BNOT	BCLR													
7Eaa6*2				BTST												
7Eaa7*2				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD								
7Faa6*2	BSET	BNOT	BCLR					BST / BIST								
7Faa7*2	BSET	BNOT	BCLR													

Notes: 1. r is the register designation field.
2. aa is the absolute address field.

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MULXS	MULXS.B Rs, Rd	2					12
	MULXS.W Rs, ERd	2					20
MULXU	MULXU.B Rs, Rd	1					12
	MULXU.W Rs, ERd	1					20
NEG	NEG.B Rd	1					
	NEG.W Rd	1					
	NEG.L ERd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
	NOT.W Rd	1					
	NOT.L ERd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
	OR.W #xx:16, Rd	2					
	OR.W Rs, Rd	1					
	OR.L #xx:32, ERd	3					
	OR.L ERs, ERd	2					
ORC	ORC #xx:8, CCR	1					
POP	POP.W Rn	1				1	2
	POP.L ERn	2				2	2
PUSH	PUSH.W Rn	1				1	2
	PUSH.L ERn	2				2	2
ROTL	ROTL.B Rd	1					
	ROTL.W Rd	1					
	ROTL.L ERd	1					
ROTR	ROTR.B Rd	1					
	ROTR.W Rd	1					
	ROTR.L ERd	1					
ROTXL	ROTXL.B Rd	1					
	ROTXL.W Rd	1					
	ROTXL.L ERd	1					

H8/38524 Group
Hardware Manual

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