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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38524wv

1.1.2 Overview of Specifications

Table 1.1 lists the functions of H8/38524 Group products in outline.

Table 1.1 Overview of Functions

Classification	Module/ Function	Description
Memory	ROM	• ROM lineup: Flash memory version and mask Rom version • ROM capacity: 8 K, 12 K, 16 K, 24 K, and 32 Kbytes
	RAM	• RAM capacity: 512 and 1024 bytes
CPU	CPU	• H8/300H CPU (CISC type) Upward compatibility for H8/300 CPU at object level • Sixteen 16-bit general registers • Eight addressing modes • 64-Kbyte address space Program: 64 Kbytes available Data: 64 Kbytes available • 62 basic instructions, classifiable as bit arithmetic and logic instructions, multiply and divide instructions, bit manipulation instructions, and others • Minimum instruction execution time: 400 ns (for an ADD instruction while system clock ϕ = 5 MHz and V_{CC} = 2.7 to 3.6 V) • On-chip multiplier (16 × 16 → 32 bits)
	Operating mode	• Normal mode
	MCU operating mode	Mode: Single-chip mode • Low power consumption state (transition driven by the SLEEP instruction)
Interrupt (source)	Interrupt controller (INTC)	• Thirteen external interrupt pins (IRQAEC, $\overline{\text{IRQ4}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$, $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$) • Nine internal interrupt sources • Independent vector addresses

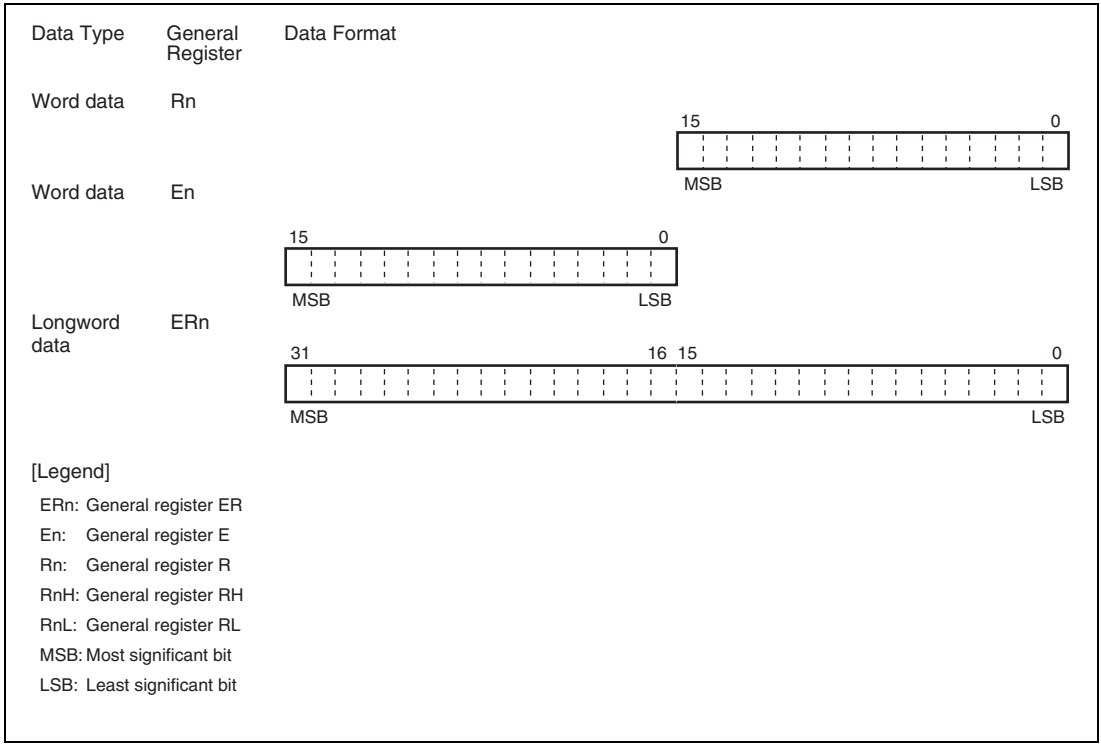
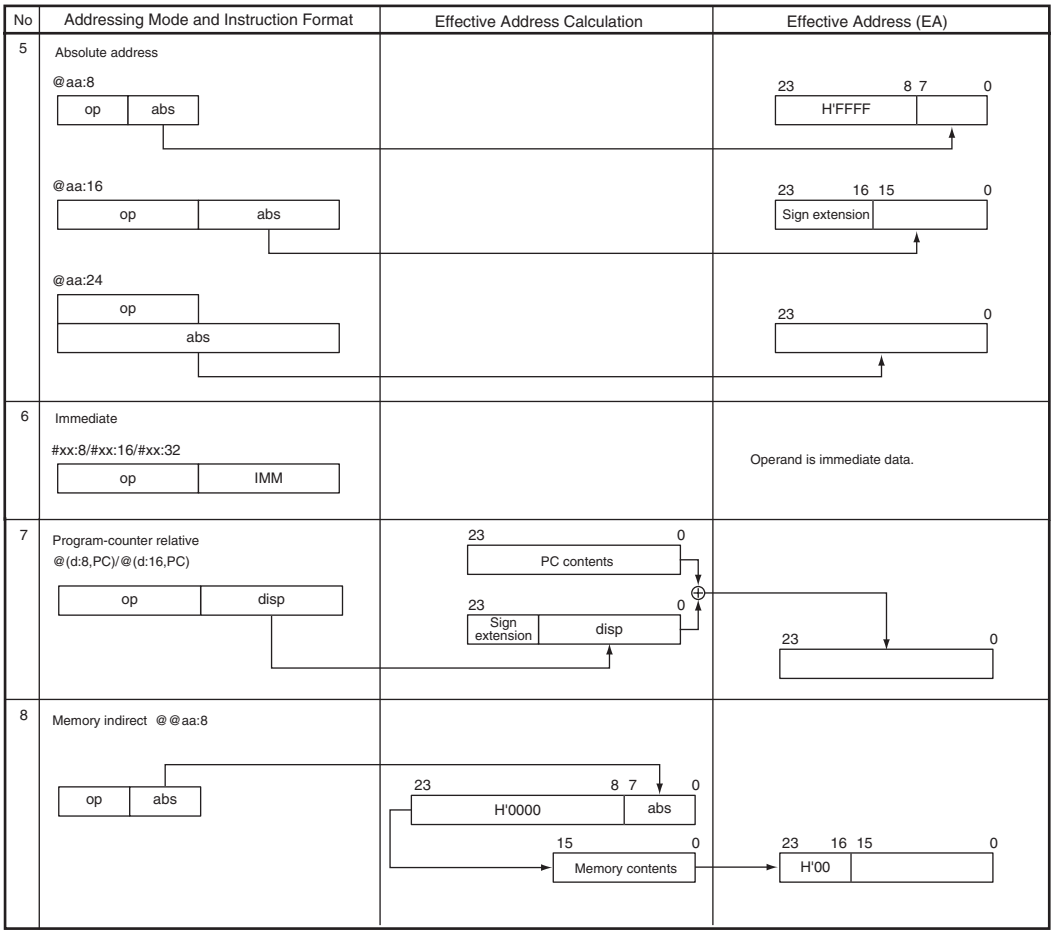


Figure 2.5 General Register Data Formats (2)

Table 2.12 Effective Address Calculation (2)



[Legend]
r, rm,rn : Register field
op : Operation field
disp : Displacement
IMM : Immediate data
abs : Absolute address

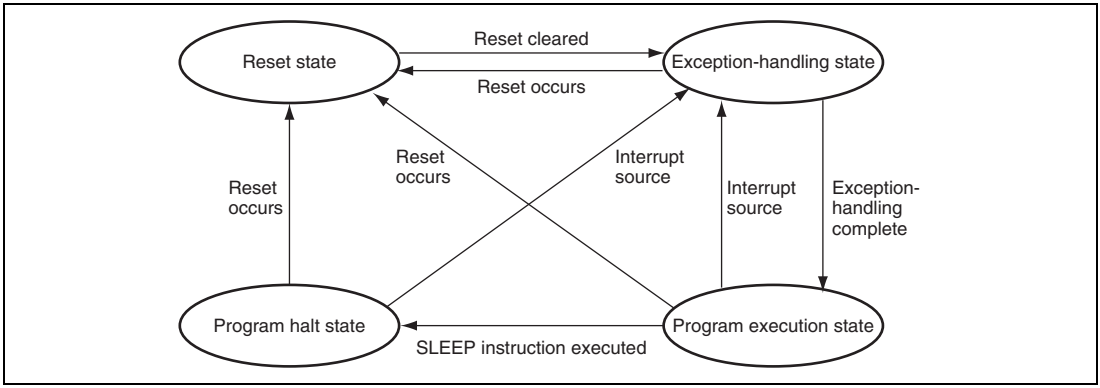


Figure 2.12 State Transitions

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).

Bit 4—$\overline{IRQ_4}$ Edge Select (IEG4)

Bit 4 selects the input sensing of the $\overline{IRQ_4}$ pin and $\overline{ADTRG}$ pin.

Bit 4 IEG4	Description	
0	Falling edge of $\overline{IRQ_4}$ and $\overline{ADTRG}$ pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_4}$ and $\overline{ADTRG}$ pin input is detected	

Bit 3—$\overline{IRQ_3}$ Edge Select (IEG3)

Bit 3 selects the input sensing of the $\overline{IRQ_3}$ pin and TMIF pin.

Bit 3 IEG3	Description	
0	Falling edge of $\overline{IRQ_3}$ and TMIF pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_3}$ and TMIF pin input is detected	

Bit 2—Reserved

Bit 2 is reserved: it can only be written with 0.

Bit 1—$\overline{IRQ_1}$ Edge Select (IEG1)

Bit 1 selects the input sensing of the $\overline{IRQ_1}$ pin and TMIC pin.

Bit 1 IEG1	Description	
0	Falling edge of $\overline{IRQ_1}$ and TMIC pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_1}$ and TMIC pin input is detected	

Bit 0—$\overline{IRQ_0}$ Edge Select (IEG0)

Bit 0 selects the input sensing of pin $\overline{IRQ_0}$.

Bit 0 IEG0	Description	
0	Falling edge of $\overline{IRQ_0}$ pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_0}$ pin input is detected	

8.2 Port 1

8.2.1 Overview

Port 1 is a 3-bit I/O port. Figure 8.1 shows its pin configuration.

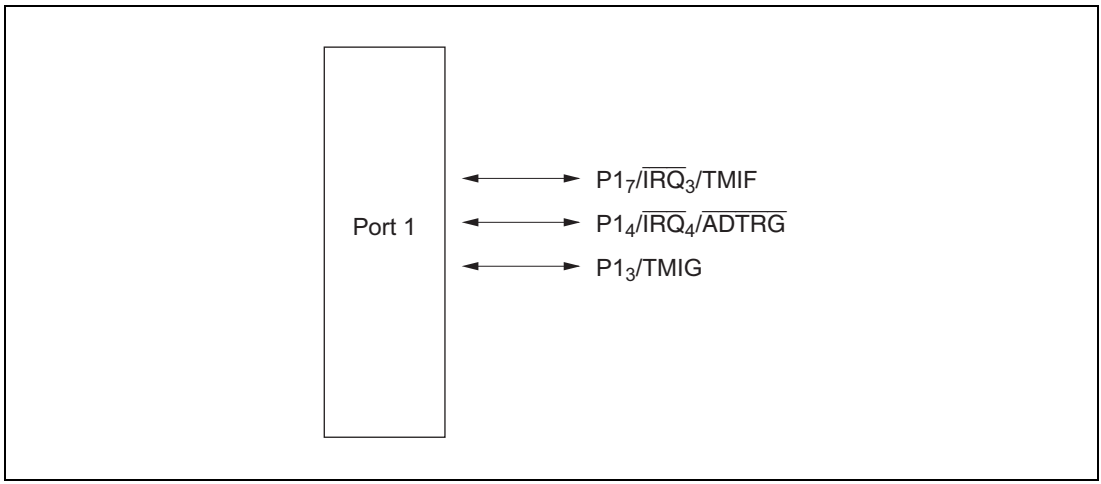


Figure 8.1 Port 1 Pin Configuration

8.2.2 Register Configuration and Description

Table 8.2 shows the port 1 register configuration.

Table 8.2 Port 1 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 1	PDR1	R/W	—	H'FFD4
Port control register 1	PCR1	W	—	H'FFE4
Port pull-up control register 1	PUCR1	R/W	—	H'FFE0
Port mode register 1	PMR1	R/W	—	H'FFC8
Port mode register 2	PMR2	R/W	H'D8	H'FFC9

Bit 3—$P1_3$/TMIG Pin Function Switch (TMIG)

This bit selects whether pin $P1_3$/TMIG is used as $P1_3$ or as TMIG.

Bit 3 TMIG	Description	
0	Functions as $P1_3$ I/O pin	(initial value)
1	Functions as TMIG input pin	

Bits 2 and 0—Reserved

These bits are reserved; they can only be written with 0.

Bit 1—Reserved

This bit is reserved; it is always read as 1 and cannot be modified.

(5) Port Mode Register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	WDCKS	NCS	IRQ0
Initial value	1	1	0	1	1	0	0	0
Read/Write	—	—	R/W	—	—	R/W	R/W	R/W

PMR2 is an 8-bit read/write register. It controls whether the PMOS transistor internal to $P3_5$ is on or off, the selection of the watchdog timer clock, the selection of TMIG noise cancellation, and switching of the $P4_3/\overline{IRQ}_0$ pin functions.

Upon reset, PMR2 is initialized to H'D8.

This section only deals with the bits related to timer G and the watchdog timer. For the functions of the bits, see the descriptions of port 3 (POF1) and port 4 (IRQ0).

8.3 Port 3

8.3.1 Overview

Port 3 is an 8-bit I/O port, configured as shown in figure 8.2.

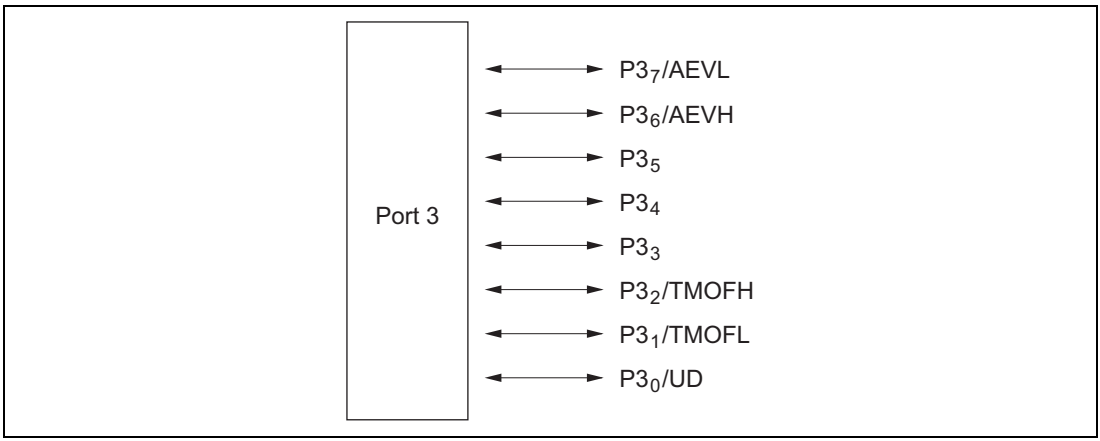


Figure 8.2 Port 3 Pin Configuration

8.3.2 Register Configuration and Description

Table 8.5 shows the port 3 register configuration.

Table 8.5 Port 3 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 3	PDR3	R/W	H'00	H'FFD6
Port control register 3	PCR3	W	H'00	H'FFE6
Port pull-up control register 3	PUCR3	R/W	H'00	H'FFE1
Port mode register 2	PMR2	R/W	H'D8	H'FFC9
Port mode register 3	PMR3	R/W	—	H'FFCA

8.5.3 Pin Functions

Table 8.12 shows the port 5 pin functions.

Table 8.12 Port 5 Pin Functions

Pin	Pin Functions and Selection Method
$P5_7/\overline{WKP_7}$/ SEG_8 to $P5_0/\overline{WKP_0}$/ SEG_1	The pin function depends on bits WKP_7 to WKP_0 in PMR5, bits $PCR5_7$ to $PCR5_0$ in PCR5, and bits SGS3 to SGS0 in LPCR.

$P5_7$ to $P5_4$ (n = 7 to 4)

SGS3 to SGS0	Other than 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001			0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001
WKP_n	0		1	*
$PCR5_n$	0	1	*	*
Pin function	$P5_n$ input pin	$P5_n$ output pin	$\overline{WKPn}$ input pin	SEGn+1 output pin

$P5_3$ to $P5_0$ (m= 3 to 0)

SGS3 to SGS0	Other than 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000			0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000
WKP_m	0		1	*
$PCR5_m$	0	1	*	*
Pin function	$P5_m$ input pin	$P5_m$ output pin	$\overline{WKPm}$ output pin	SEGm+1 output pin

*: Don't care

(1) Port Data Register 7 (PDR7)

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR7 is an 8-bit register that stores data for port 7 pins $P7_7$ to $P7_0$. If port 7 is read while PCR7 bits are set to 1, the values stored in PDR7 are read, regardless of the actual pin states. If port 7 is read while PCR7 bits are cleared to 0, the pin states are read.

Upon reset, PDR7 is initialized to H'00.

(2) Port Control Register 7 (PCR7)

Bit	7	6	5	4	3	2	1	0
	$PCR7_7$	$PCR7_6$	$PCR7_5$	$PCR7_4$	$PCR7_3$	$PCR7_2$	$PCR7_1$	$PCR7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR7 is an 8-bit register for controlling whether each of the port 7 pins $P7_7$ to $P7_0$ functions as an input pin or output pin. Setting a PCR7 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR7 and PDR7 settings are valid when the corresponding pins are designated for general-purpose input/output by bits SGS3 to SGS0 in LPCR.

Upon reset, PCR7 is initialized to H'00.

PCR7 is a write-only register, which is always read as all 1s.

8.9.3 Pin Functions

Table 8.24 shows the port 9 pin functions.

Table 8.24 Port 9 Pin Functions

Pin	Pin Functions and Selection Method		
$P9_3/V_{ref}$*			
	VREFSEL	0	1
	Pin function	$P9_3$ output pin	V_{ref} input pin
$P9_1/PWM_{n+1}$ to $P9_0/PWM_{n+1}$			(n = 1 or 0)
	$PMR9_n$	0	1
	Pin function	$P9_n$ output pin	PWM_{n+1} output pin

Note: * The V_{ref} pin is the input pin for the LVD's external reference voltage.

8.9.4 Pin States

Table 8.25 shows the port 9 pin states in each operating mode.

Table 8.25 Port 9 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P9_5$ to $P9_2$ $P9_n/PWM_{n+1}$ to $P9_n/PWM_{n+1}$	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional

(n = 1 or 0)

8.13 Application Note

8.13.1 The Management of the Un-Use Terminal

If an I/O pin not used by the user system is floating, pull it up or down.

- If an unused pin is an input pin, handle it in one of the following ways:
  - Pull it up to V_{CC} with an on-chip pull-up MOS.
  - Pull it up to V_{CC} with an external resistor of approximately 100 kΩ.
  - Pull it down to V_{SS} with an external resistor of approximately 100 kΩ.
  - For a pin also used by the A/D converter, pull it up to AV_{CC}.
- If an unused pin is an output pin, handle it in one of the following ways:
  - Set the output of the unused pin to high and pull it up to V_{CC} with an on-chip pull-up MOS.
  - Set the output of the unused pin to high and pull it up to V_{CC} with an external resistor of approximately 100 kΩ.
  - Set the output of the unused pin to low and pull it down to GND with an external resistor of approximately 100 kΩ.

(2) Timer Counter A (TCA)

Bit	7	6	5	4	3	2	1	0
	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCA is an 8-bit read-only up-counter, which is incremented by internal clock input. The clock source for input to this counter is selected by bits TMA3 to TMA0 in timer mode register A (TMA). TCA values can be read by the CPU in active mode, but cannot be read in subactive mode. When TCA overflows, the IRRTA bit in interrupt request register 1 (IRR1) is set to 1.

TCA is cleared by setting bits TMA3 and TMA2 of TMA to 11.

Upon reset, TCA is initialized to H'00.

(3) Clock Stop Register 1 (CKSTPR1)

Bit:	7	6	5	4	3	2	1	0
	—	—	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value:	1	1	1	1	1	1	1	1
Read/Write:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to timer A is described here. For details of the other bits, see the sections on the relevant modules.

Bit 0—Timer A Module Standby Mode Control (TACKSTP)

Bit 0 controls setting and clearing of module standby mode for timer A.

TACKSTP	Description	
0	Timer A is set to module standby mode	
1	Timer A module standby mode is cleared	(initial value)

9.3.4 Timer C Operation States

Table 9.6 summarizes the timer C operation states.

Table 9.6 Timer C Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCC	Interval	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
	Auto reload	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
TMC		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: * When $\phi w/4$ is selected as the TCC internal clock in active mode or sleep mode, since the system clock and internal clock are mutually asynchronous, synchronization is maintained by a synchronization circuit. This results in a maximum count cycle error of $1/\phi$ (s). When the counter is operated in subactive mode or subsleep mode, either select $\phi w/4$ as the internal clock or select an external clock. The counter will not operate on any other internal clock. If $\phi w/4$ is selected as the internal clock for the counter when $\phi w/8$ has been selected as subclock ϕ_{SUB}, the lower 2 bits of the counter operate on the same cycle, and the operation of the least significant bit is unrelated to the operation of the counter.

(2) 8-bit Event Counter Operation

When bit CH2 is set to 1 in ECCSR, ECH and ECL operate as independent 8-bit event counters.

ϕ/2, ϕ/4, ϕ/8, or AEVH pin input can be selected as the input clock source for ECH by means of bits ACKH1 and ACKH0 in ECCR, and ϕ/2, ϕ/4, ϕ/8, or AEVL pin input can be selected as the input clock source for ECL by means of bits ACKL1 and ACKL0 in ECCR.

Input sensing is selected with bits AHEGS1 and AHEGS0 when AEVH pin input is selected, and with bits ALEGS1 and ALEGS0 when AEVL pin input is selected.

The input clock is enabled only when IRQAEC is high or IECPWM is high. When IRQAEC is low or IECPWM is low, the input clock is not input to the counter, which therefore does not operate. Figure 9.21 shows an example of the software processing when ECH and ECL are used as 8-bit event counters.

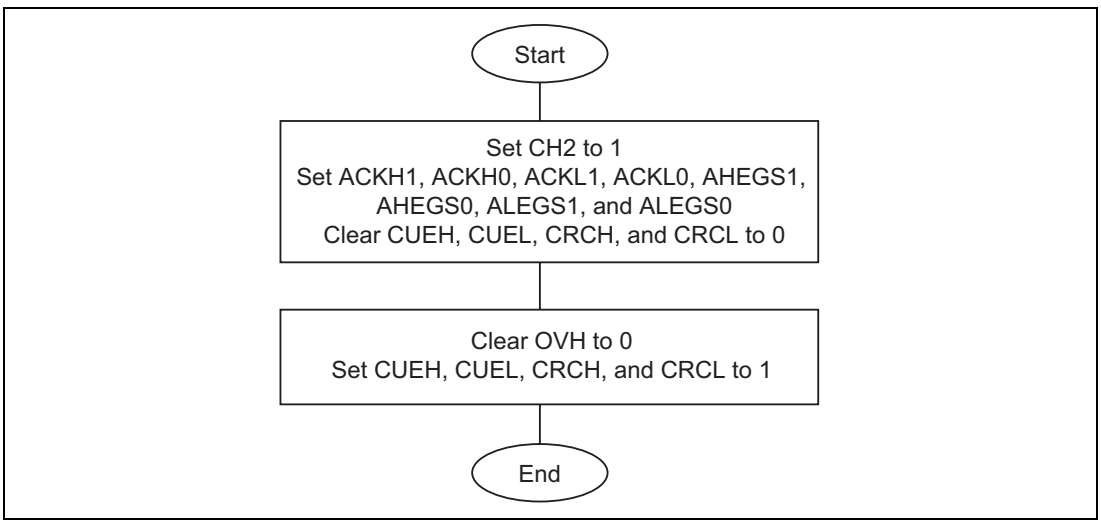


Figure 9.21 Example of Software Processing when Using ECH and ECL as 8-Bit Event Counters

ECH and ECL can be used as 8-bit event counters by carrying out the software processing shown in the example in figure 9.21. When the next clock is input after the ECH count value reaches H'FF, ECH overflows, the OVH flag is set to 1 in ECCSR, the ECH count value returns to H'00, and counting up is restarted. Similarly, when the next clock is input after the ECL count value reaches H'FF, ECL overflows, the OVL flag is set to 1 in ECCSR, the ECL count value returns to H'00, and counting up is restarted. When overflow occurs, the IRREC bit is set to 1 in IRR2. If the IENEC bit in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

Bit 7—Clock Select (CKS)

Bit 7 sets the A/D conversion speed.

Bit 7 CKS	Conversion Period	Conversion Time ϕ = 1 MHz	ϕ = 5 MHz	ϕ = 10 MHz
0	62/ϕ (initial value)	62 µs	12.4 µs	6.2 µs
1	31/ϕ	31 µs	—*	—*

Note: * The operation cannot be guaranteed if the conversion time is less than 6.2 µs. Make sure to select a setting that gives a conversion time of 6.2 µs or more.

Bit 6—External Trigger Select (TRGE)

Bit 6 enables or disables the start of A/D conversion by external trigger input.

Bit 6 TRGE	Description	
0	Disables start of A/D conversion by external trigger	(initial value)
1	Enables start of A/D conversion by rising or falling edge of external trigger at pin $\overline{\text{ADTRG}}$*	

Note: * The external trigger ($\overline{\text{ADTRG}}$) edge is selected by bit IEG4 of IEGR. See (1) IRQ Edge Select Register (IEGR) in section 3.3.2, Interrupt Control Registers, for details.

Bits 5 and 4—Reserved

Bits 5 and 4 are reserved; they are always read as 1, and cannot be modified.

Section 14 Power-On Reset and Low-Voltage Detection Circuits

14.1 Overview

This LSI can include a power-on reset circuit and low-voltage detection circuit.

The low-voltage detection circuit consists of two circuits: LVDI (interrupt by low voltage detect) and LVDR (reset by low voltage detect) circuits.

This circuit is used to prevent abnormal operation (runaway execution) from occurring due to the power supply voltage fall and to recreate the state before the power supply voltage fall when the power supply voltage rises again.

Even if the power supply voltage falls, the unstable state when the power supply voltage falls below the guaranteed operating voltage can be removed by entering standby mode* when exceeding the guaranteed operating voltage and during normal operation. Thus, system stability can be improved. If the power supply voltage falls more, the reset state is automatically entered. If the power supply voltage rises again, the reset state is held for a specified period, then active mode is automatically entered.

Figure 14.1 is a block diagram of the power-on reset circuit and the low-voltage detection circuit.

Note: * The voltage maintained in standby mode is the same as the RAM data retaining voltage (V_{RAM}). See section 17.2.2, DC Characteristics, for information on retaining voltage.

14.2.3 Low-Voltage Detection Counter (LVDCNT)

Bit	7	6	5	4	3	2	1	0
	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

LVDCNT is a read-only 8-bit up-counter. Counting begins when 1 is written to LVDE. The counter increments using $\phi/4$ as the clock source until it overflows by switching from H'FF to H'00, at which time the OVF bit in the LVDSR register is set to 1, indicating that the on-chip reference voltage generator has stabilized. If the LVD function is used, it is necessary to stand by until the counter has overflowed. The initial value of LVDCNT is H'00.

14.2.4 Clock Stop Register 2 (CKSTPR2)

Bit	7	6	5	4	3	2	1	0
	LVDCKSTP	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

CKSTPR2 is an 8-bit read/write register. It is used to control the module's module standby mode. Only the bits relevant to the LVD function are described in this section. Refer to the sections on the other modules for information about the other bits.

Bit 7—LVD Module Standby Control (LVDCKSTP)

This bit is used to control setting of the LVD function to module standby status and cancellation of that status.

Bit 7 LVDCKSTP	Description	
0	Sets LVD to module standby status	
1	Cancels LVD module standby status	(initial value)

17.2.3 AC Characteristics

Table 17.3 lists the control signal timing and table 17.4 lists the serial interface timing.

Table 17.3 Control Signal Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item	Symbol	Applicable Pins	Values			Unit	Test Condition	Reference Figure
			Min	Typ	Max			
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2.0	—	20.0	MHz		
			0.7	—	2.0		On-chip oscillator selected	*2
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	50.0	—	500	ns		Figure 17.1
			500	—	1429		On-chip oscillator selected	
System clock (ϕ) cycle time	t_{cyc}		2	—	128	t_{OSC}		
			—	—	182	µs		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.768	—	kHz		
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2	—	30.5	—	µs		Figure 17.1
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	8	t_W		*1
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	—	—	20	ms		
	t_{rc}	X_1, X_2	—	—	2.0	s		
External clock high width	t_{CPH}	OSC_1	20	—	—	ns		Figure 17.1
External clock low width	t_{CPL}	OSC_1	20	—	—	ns		Figure 17.1
External clock rise time	t_{CPr}	OSC_1	—	—	5	ns		Figure 17.1
External clock fall time	t_{CPf}	OSC_1	—	—	5	ns		Figure 17.1
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	10	—	—	t_{cyc}		Figure 17.2