Lattice Semiconductor Corporation - ISPLSI 1048E-70LT Datasheet

Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	48
Number of Macrocells	192
Number of Gates	8000
Number of I/O	96
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/isplsi-1048e-70lt

Lead-Free Package Options Available!

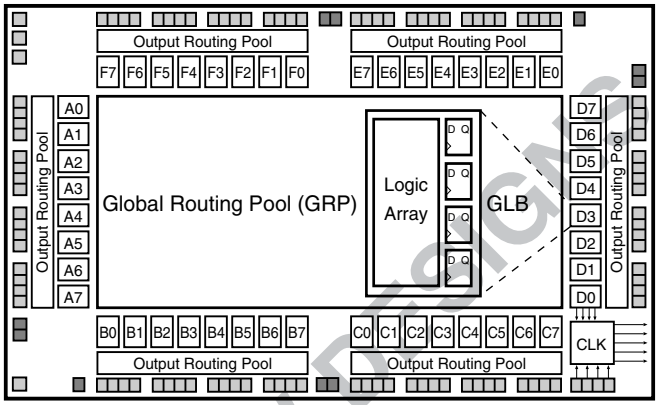
ispLSI® 1048E

In-System Programmable High Density PLD

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **8,000 PLD Gates**
  - **96 I/O Pins, Twelve Dedicated Inputs**
  - **288 Registers**
  - **High-Speed Global Interconnects**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **Functionally and Pin-out Compatible to ispLSI 1048C**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **f_{max} = 125 MHz Maximum Operating Frequency**
  - **t_{pd} = 7.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Eraseable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
- **IN-SYSTEM PROGRAMMABLE**
  - **In-System Programmable (ISP™) 5V Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Four Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
  - **Lead-Free Package Options**

Functional Block Diagram



0139G1A-isp

Description

The ispLSI 1048E is a High Density Programmable Logic Device containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, four Dedicated Clock Input pins, two dedicated Global OE input pins, and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048E offers 5V non-volatile in-system programmability of the logic, as well as the interconnect to provide truly reconfigurable systems. A functional superset of the ispLSI 1048 architecture, the ispLSI 1048E device adds two new global output enable pins and two additional dedicated inputs.

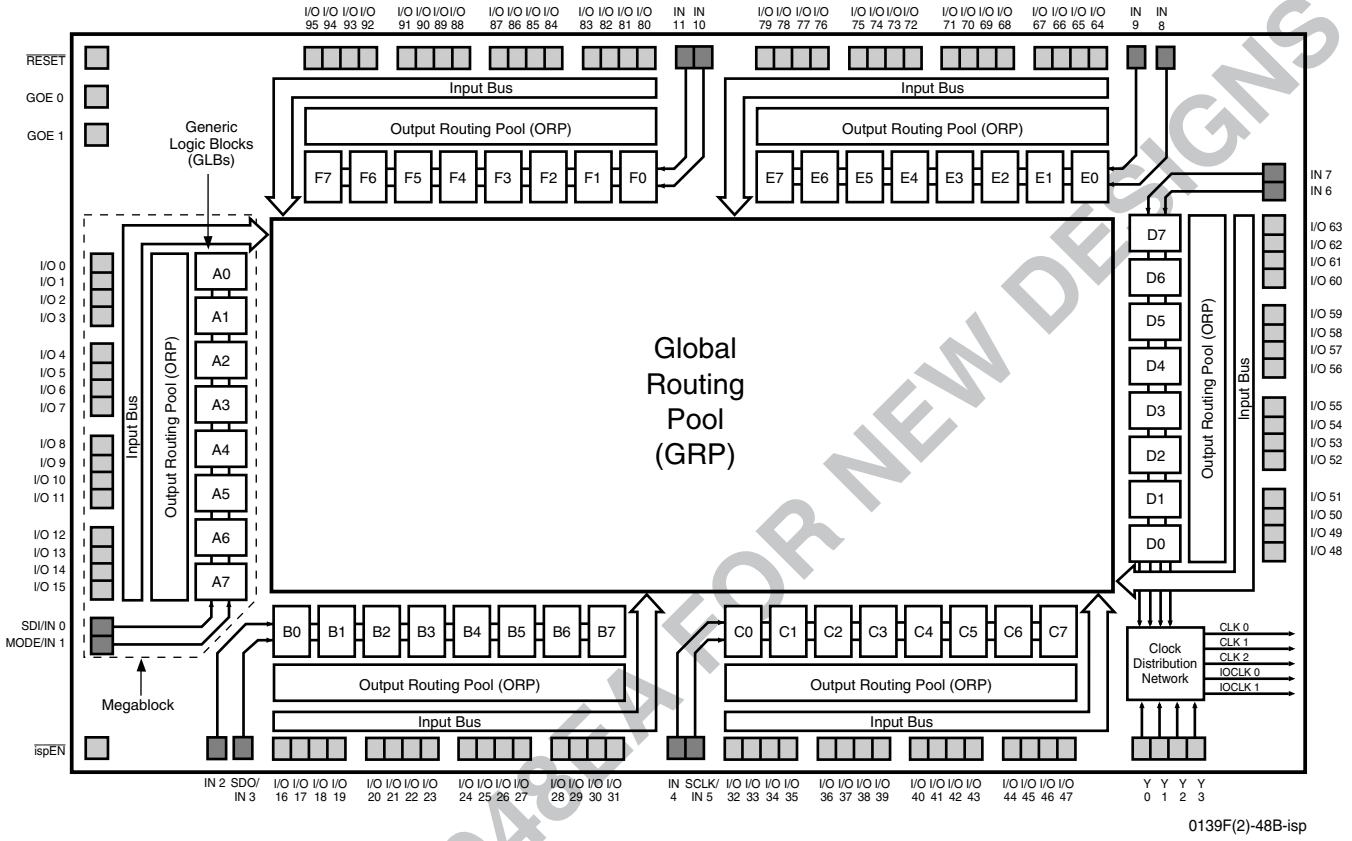
The basic unit of logic on the ispLSI 1048E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…F7 (see Figure 1). There are a total of 48 GLBs in the ispLSI 1048E device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2006

Functional Block Diagram

Figure 1. ispLSI 1048E Functional Block Diagram



The device also has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 1048E device contains six Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1048E device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC}. ..... -0.5 to +7.0V

Input Voltage Applied..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2-0005/1048E

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	15	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

Table 2-0006/1048E

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/1048E

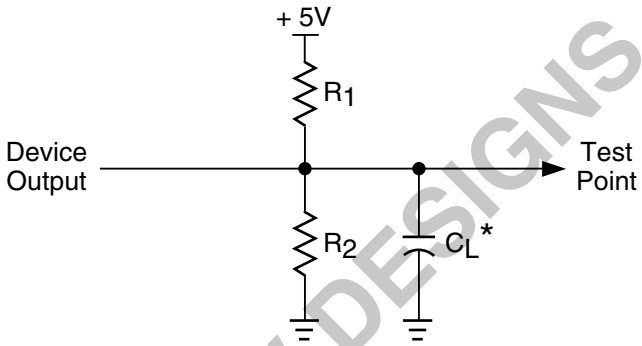
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3 ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/1048E

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{\text{ispEN}}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	175	–	mA
		f_{CLOCK} = 1 MHz	Industrial	–	175	–	mA

Table 2-0007/1048E

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		-90		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	10.0	–	12.5	–	12.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	125.0	–	100.0	–	90.9	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	91.0	–	71.0	–	71.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{wl}}\right)$	167.0	–	125.0	–	125.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	5.5	–	6.5	–	6.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	6.5	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.5	–	7.5	–	7.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.5	–	7.5	–	7.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	13.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	15.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	15.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	9.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	9.0	–	9.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	4.0	–	4.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	4.0	–	4.0	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	3.0	–	3.5	–	4.0	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	0.0	–	ns

Table 2-0030A/1048E

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	18.5	–	24.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	70.0	–	50.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	56.0	–	42.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{wl}}\right)$	100.0	–	77.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	9.0	–	12.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	7.0	–	9.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	11.0	–	14.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	9.0	–	12.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15.0	–	20.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10.0	–	13.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	18.0	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	18.0	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	12.0	–	16.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	12.0	–	16.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	6.5	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	6.5	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	4.0	–	6.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	ns

Table 2-0030B/1048E

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-125		-100		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	22	I/O Register Bypass	–	0.3	–	0.3	–	0.5	ns
t_{iolat}	23	I/O Latch Delay	–	1.9	–	2.3	–	2.5	ns
t_{iosu}	24	I/O Register Setup Time before Clock	3.0	–	3.5	–	4.0	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	0.0	–	0.0	–	-0.5	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	4.6	–	5.0	–	5.0	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	4.6	–	5.0	–	5.0	ns
t_{din}	28	Dedicated Input Delay	–	2.3	–	2.7	–	2.9	ns
GRP									
t_{grp1}	29	GRP Delay, 1 GLB Load	–	1.8	–	1.9	–	2.2	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	2.0	–	2.4	–	2.4	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	2.3	–	2.6	–	2.7	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	2.8	–	3.0	–	3.3	ns
t_{grp48}	33	GRP Delay, 48 GLB Loads	–	4.9	–	5.4	–	5.7	ns
GLB									
t_{4ptbpc}	34	4 Product Term Bypass Path Delay (Combinatorial)	–	3.9	–	5.3	–	5.4	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	–	4.0	–	5.3	–	6.3	ns
t_{1ptxor}	36	1 Product Term/XOR Path Delay	–	3.6	–	4.6	–	6.5	ns
$t_{20ptxor}$	37	20 Product Term/XOR Path Delay	–	5.0	–	5.8	–	6.5	ns
t_{xoradj}	38	XOR Adjacent Path Delay[3]	–	5.0	–	6.3	–	7.3	ns
t_{gbp}	39	GLB Register Bypass Delay	–	0.4	–	1.0	–	0.4	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.1	–	0.5	–	0.1	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	4.5	–	5.3	–	6.4	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	2.3	–	2.5	–	2.0	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	4.9	–	6.2	–	6.3	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	–	3.9	–	4.5	–	5.0	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.4	–	7.2	–	5.7	ns
t_{ptck}	46	GLB Product Term Clock Delay	2.9	4.0	3.5	4.7	4.0	5.2	ns
ORP									
t_{orp}	47	ORP Delay	–	1.0	–	1.0	–	1.0	ns
t_{orpbp}	48	ORP Bypass Delay	–	0.0	–	0.0	–	0.0	ns

Table 2-0036A/1048E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	22	I/O Register Bypass	–	0.6	–	0.7	ns
t_{iolat}	23	I/O Latch Delay	–	3.6	–	4.7	ns
t_{iosu}	24	I/O Register Setup Time before Clock	4.1	–	6.5	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	-0.6	–	-0.7	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	6.0	–	7.0	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	6.0	–	7.0	ns
t_{din}	28	Dedicated Input Delay	–	4.3	–	6.1	ns
GRP							
t_{grp1}	29	GRP Delay, 1 GLB Load	–	3.5	–	5.1	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	3.7	–	5.4	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	4.1	–	5.8	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	4.8	–	6.6	ns
t_{grp48}	33	GRP Delay, 48 GLB Loads	–	7.5	–	9.8	ns
GLB							
t_{4ptbpc}	34	4 Product Term Bypass Path Delay (Combinatorial)	–	8.5	–	10.7	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	–	7.4	–	9.2	ns
t_{1ptxor}	36	1 Product Term/XOR Path Delay	–	8.4	–	10.5	ns
$t_{20ptxor}$	37	20 Product Term/XOR Path Delay	–	8.4	–	10.5	ns
t_{xoradj}	38	XOR Adjacent Path Delay[3]	–	9.4	–	11.7	ns
t_{gbp}	39	GLB Register Bypass Delay	–	1.6	–	2.2	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.1	–	0.0	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	8.5	–	11.5	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	2.0	–	3.0	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	6.3	–	7.3	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	–	6.1	–	7.9	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	–	6.8	–	10.0	ns
t_{ptck}	46	GLB Product Term Clock Delay	5.1	6.4	6.9	8.3	ns
ORP							
t_{orp}	47	ORP Delay	–	2.0	–	2.5	ns
t_{orpbp}	48	ORP Bypass Delay	–	0.0	–	0.0	ns

Table 2-0036B/1048E

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#	DESCRIPTION	-125		-100		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	49	Output Buffer Delay	–	1.3	–	2.0	–	1.7	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	12.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	4.3	–	5.1	–	6.4	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	4.3	–	5.1	–	6.4	ns
t_{goe}	53	Global OE	–	2.7	–	3.9	–	2.6	ns
Clocks									
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	0.9	0.9	2.0	2.0	2.8	2.8	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	0.9	0.9	2.0	2.0	2.8	2.8	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.0	0.0	0.0	0.0	0.0	0.5	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
Global Reset									
t_{gr}	59	Global Reset to GLB and I/O Registers	–	2.8	–	4.3	–	4.5	ns

Table 2-0037A/1048E

1. Internal timing parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

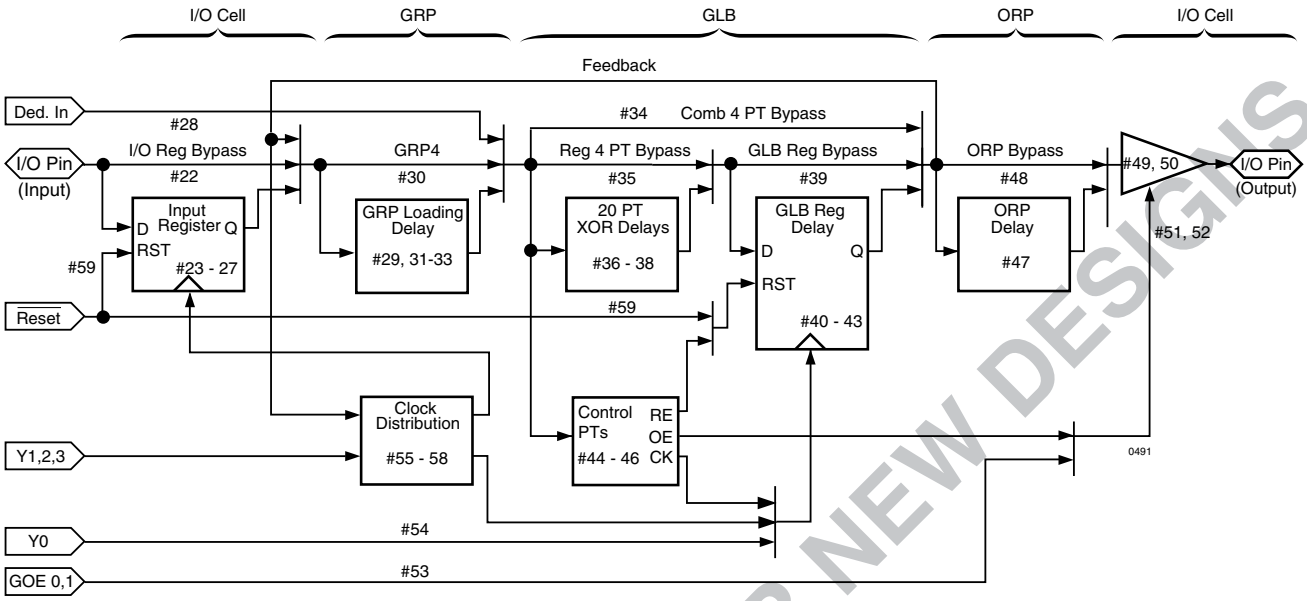
Internal Timing Parameters[1]

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	49	Output Buffer Delay	–	2.2	–	3.2	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	12.0	–	12.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	6.9	–	7.9	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	6.9	–	7.9	ns
t_{goe}	53	Global OE	–	5.1	–	8.1	ns
Clocks							
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.8	2.8	3.3	3.3	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	2.8	3.3	3.3	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.1	0.6	0.0	0.7	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	ns
Global Reset							
t_{gr}	59	Global Reset to GLB and I/O Registers	–	4.5	–	7.5	ns

Table 2-0037B/1048E

1. Internal timing parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 1048E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) – (tiobp + tgrp4 + tptck(min))
= (#22 + #30 + #37) + (#40) – (#22 + #30 + #46)
2.2 ns = (0.3 + 2.0 + 5.0) + (0.1) – (0.3 + 2.0 + 2.9)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp4 + tptck(max)) + (tgh) – (tiobp + tgrp4 + t20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
3.5 ns = (0.3 + 2.0 + 4.0) + (4.5) – (0.3 + 2.0 + 5.0)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp4 + tptck(max)) + (tgco) + (torp + tob)
= (#22 + #30 + #46) + (#42) + (#47 + #49)
10.9 ns = (0.3 + 2.0 + 4.0) + (2.3) + (1.0 + 1.3)

Derivations of tsu, th and tco from the Clock GLB[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) – (tgy0(min) + tgco + tgcp(min))
= (#22 + #30 + #37) + (#40) – (#54 + #42 + #56)
3.4 ns = (0.3 + 2.0 + 5.0) + (0.1) – (0.9 + 2.3 + 0.8)

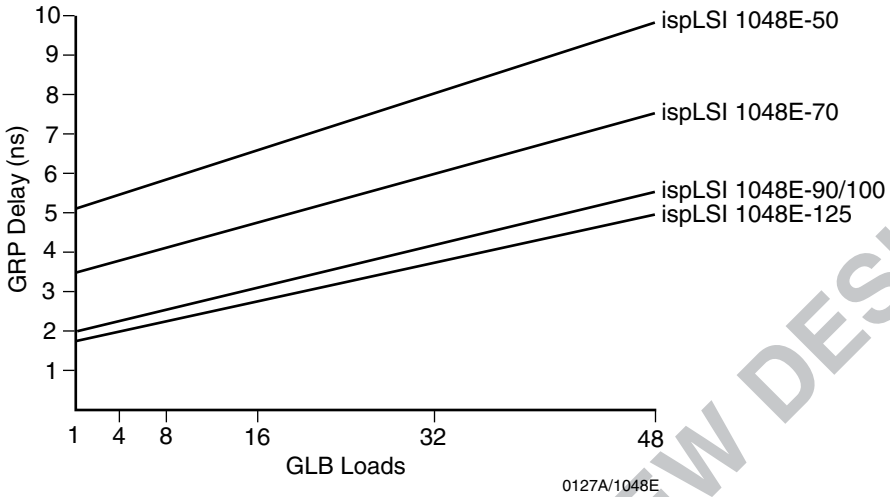
th = Clock (max) + Reg h - Logic
= (tgy0(max) + tgco + tgcp(max)) + (tgh) – (tiobp + tgrp4 + t20ptxor)
= (#54 + #42 + #56) + (#41) – (#22 + #30 + #37)
2.2 ns = (0.9 + 2.3 + 1.8) + (4.5) – (0.3 + 2.0 + 5.0)

tco = Clock (max) + Reg co + Output
= (tgy0(max) + tgco + tgcp(max)) + (tgco) + (torp + tob)
= (#54 + #42 + #56) + (#42) + (#47 + #49)
9.6 ns = (0.9 + 2.3 + 1.8) + (2.3) + (1.0 + 1.3)

1. Calculations are based upon timing specifications for the ispLSI 1048E-125.

Table 2-0042/1048E

Maximum GRP Delay vs. GLB Loads

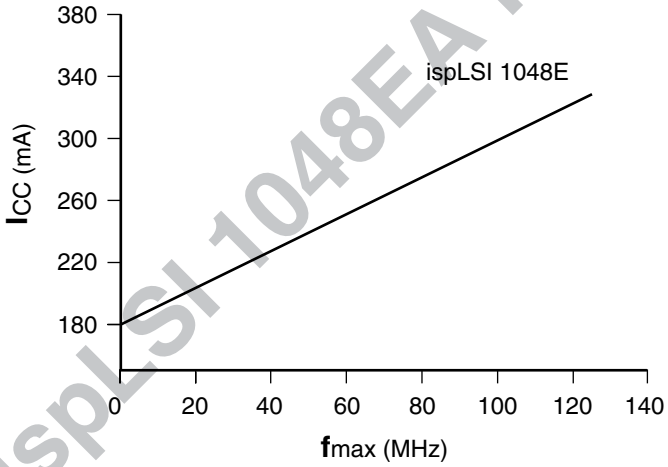


0127A/1048E

Power Consumption

Power consumption in the ispLSI 1048E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of twelve 16-bit counters,
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI 1048E using the following equation:

I_{CC} = 20 + (# of PTs * 0.42) + (# of nets * Max. freq * 0.010)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 4 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127B/1048E

Pin Description

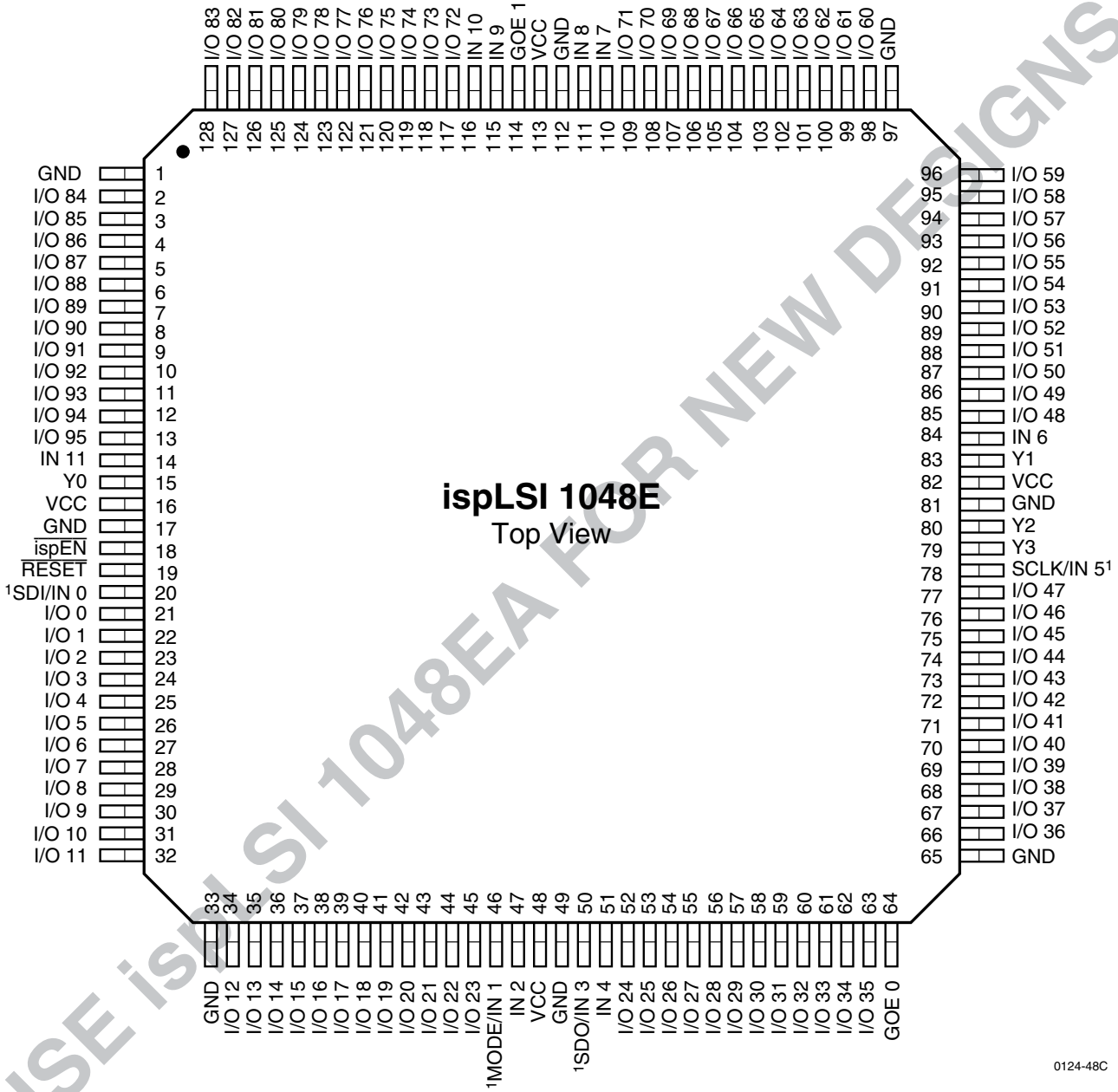
NAME	PQFP / TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	64, 114	Global Output Enable input pins.
IN 2, IN 4 IN 6 - IN 11	47, 51 84, 110, 111, 115, 116, 14	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	18	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.
SDI/IN 0[1]	20	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE/IN 1[1]	46	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO/IN 3[1]	50	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK/IN 5[1]	78	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
$\overline{\text{RESET}}$	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	15	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	83	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	80	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	79	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 17, 33, 49, 65, 81, 97, 112	Ground (GND)
VCC	16, 48, 82, 113	V_{CC}

1. Pins have dual function capability.

Table 2 - 0002C-48E

Pin Configuration

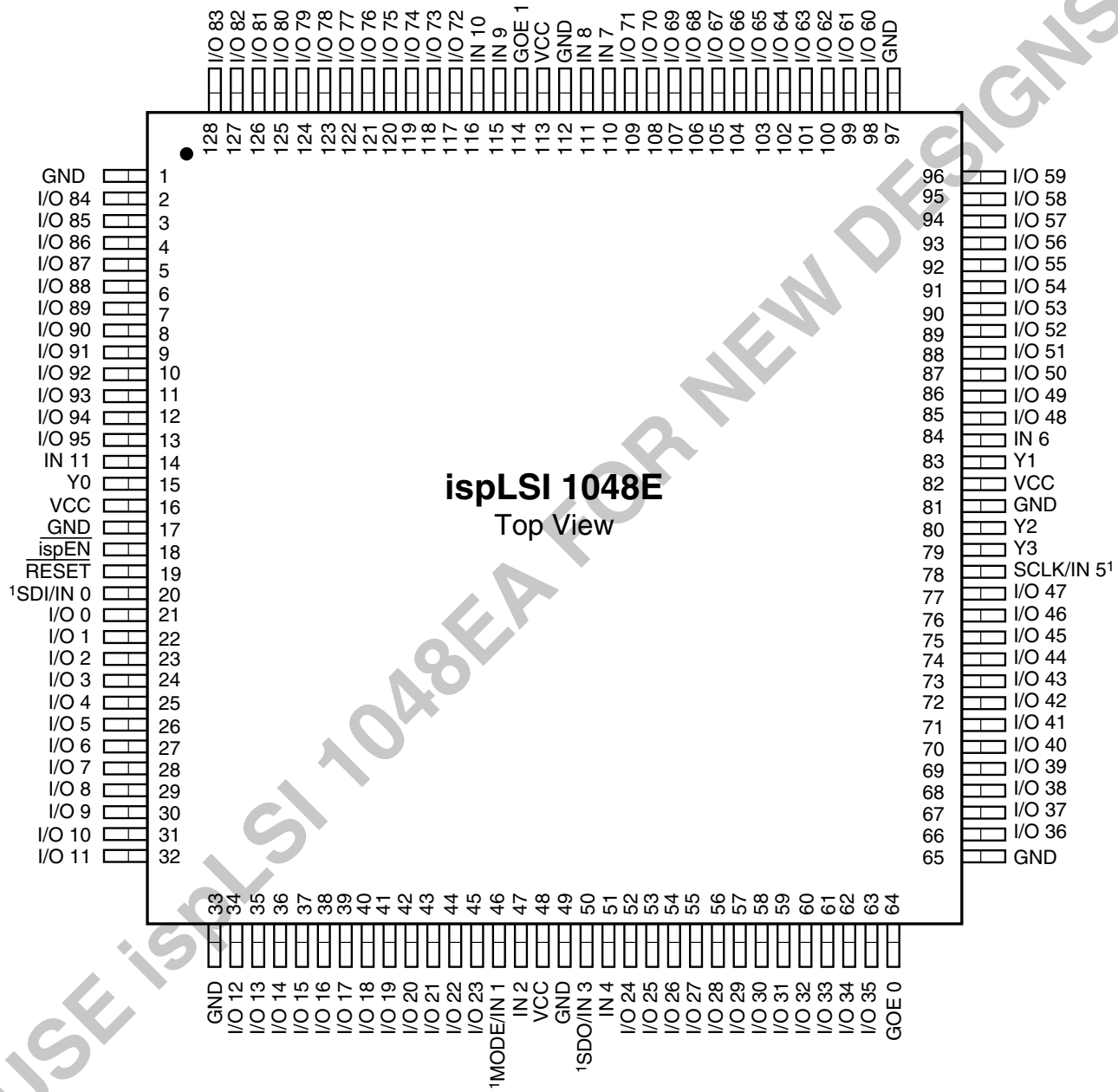
ispLSI 1048E 128-Pin PQFP Pinout Diagram



1. Pins have dual function capability.

Pin Configuration

ispLSI 1048E 128-Pin TQFP Pinout Diagram



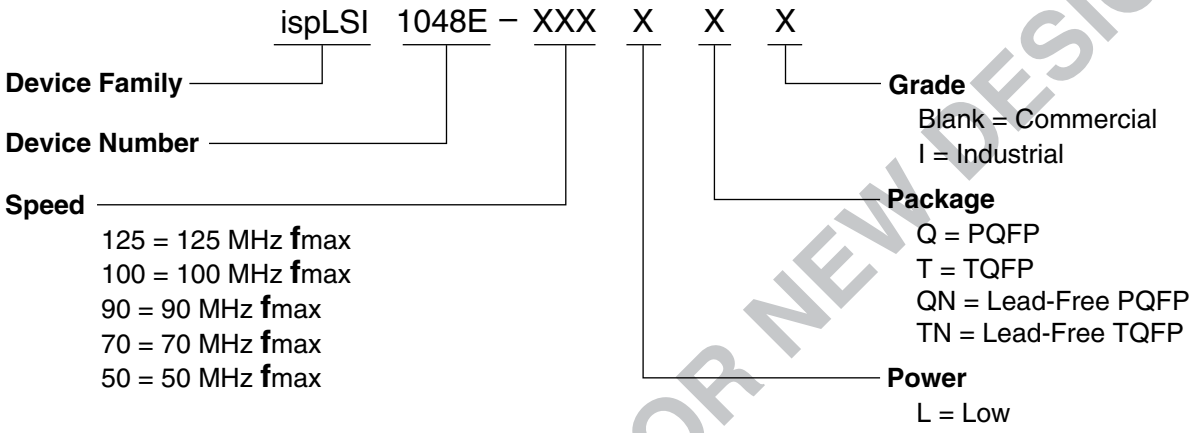
1. Pins have dual function capability.

0124-48/TQFP

Package Thermal Characteristics

For the ispLSI 1048E-125LT, it is strongly recommended that the actual Icc be verified to ensure that the maximum junction temperature (T_J) with power supplied is not exceeded. Depending on the specific logic design and clock speed, airflow may be required to satisfy the maximum allowable junction temperature (T_J) specification. Please refer to the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM for additional information on calculating T_J.

Part Number Description



ispLSI 1048E Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 1048E-125LQ	128-Pin PQFP
	125	7.5	ispLSI 1048E-125LT	128-Pin TQFP
	100	10	ispLSI 1048E-100LQ	128-Pin PQFP
	100	10	ispLSI 1048E-100LT	128-Pin TQFP
	90	10	ispLSI 1048E-90LQ	128-Pin PQFP
	90	10	ispLSI 1048E-90LT	128-Pin TQFP
	70	15	ispLSI 1048E-70LQ	128-Pin PQFP
	70	15	ispLSI 1048E-70LT	128-Pin TQFP
	50	20	ispLSI 1048E-50LQ	128-Pin PQFP
	50	20	ispLSI 1048E-50LT	128-Pin TQFP

Table 2-0041A/1048E

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	70	15	ispLSI 1048E-70LQI*	128-Pin PQFP
	50	20	ispLSI 1048E-50LQI*	128-Pin PQFP

*Use 1048E-70 for new 1048E-50 designs.

Table 2-0041B/1048E

ispLSI 1048E Ordering Information (Cont.)

Lead-Free Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 1048E-125LQN	Lead-Free 128-Pin PQFP
	125	7.5	ispLSI 1048E-125LTN	Lead-Free 128-Pin TQFP
	100	10	ispLSI 1048E-100LQN	Lead-Free 128-Pin PQFP
	100	10	ispLSI 1048E-100LTN	Lead-Free 128-Pin TQFP
	90	10	ispLSI 1048E-90LQN	Lead-Free 128-Pin PQFP
	90	10	ispLSI 1048E-90LTN	Lead-Free 128-Pin TQFP
	70	15	ispLSI 1048E-70LQN	Lead-Free 128-Pin PQFP
	70	15	ispLSI 1048E-70LTN	Lead-Free 128-Pin TQFP
	50	20	ispLSI 1048E-50LQN	Lead-Free 128-Pin PQFP
	50	20	ispLSI 1048E-50LTN	Lead-Free 128-Pin TQFP

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	70	15	ispLSI 1048E-70LQNI	Lead-Free 128-Pin PQFP

Revision History

Date	Version	Change Summary
—	11	Previous Lattice release.
August 2006	12	Updated for lead-free package options.