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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	CPU16
Core Size	16-Bit
Speed	16MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-BQFP Bumpered
Supplier Device Package	132-PQFP (24.13x24.13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc16z1ceh16

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Mnemonic	Operation	Description	Address		Instruction				Con	ditior	n Co	des		_
			Mode	Opcode	Operand	Cycles	s	ΜV	н	EV	Ν	z	v	C
LDAB	Load B	$(M) \Rightarrow B$	IND8, X	C5	ff	6	_	<u> </u>	-		Δ	Δ	0	Δ
			IND8, Y	D5	ff	6								
			IND8, Z	E5	ff	6								
			IMM8	F5	ii	2								
			IND16, X	17C5	gggg	6								
			IND16, Y	17D5	gggg	6								
			IND16, Z	17E5	9999	6								
			EXT	17F5	hh ll	6								
			E, X	27C5	_	6								
			E, Y	27D5	_	6								
			E, Z	27E5	_	6								
LDD	Load D	$(M:M+1) \Rightarrow D$	IND8, X	85	ff	6	—	_	_	_	Δ	Δ	0	-
		, ,	IND8, Y	95	ff	6								
			IND8, Z	A5	ff	6								
			IMM16	37B5	jj kk	4								
			IND16, X	37C5	gggg	6								
			IND16, Y	37D5	9999	6								
			IND16, Z	37E5	gggg	6								
			EXT	37F5	hh ll	6								
			E, X	2785	_	6								
			E, Y	2795	_	6								
			E, Z	27A5	_	6								
LDE	Load E	$(M:M+1) \Rightarrow E$	IMM16	3735	jj kk	4					Δ	Δ	0	_
LDL	LUdu L	$(M : M + 1) \rightarrow L$	IND16, X	3745		6						Δ	0	
			IND16, Y	3755	9999	6								
			IND16, Z	3765	9999	6								
			EXT	3775	gggg hh ll	6								
LDED	Lood Constant	$(M:M+1) \Rightarrow E$				8								_
LDED	Load Concatenated E and D	$(M : M + 1) \Rightarrow E$ $(M + 2 : M + 3) \Rightarrow D$	EXT	2771	hh ll	o	_	_	_	_	_	_	_	
L DI II				0700		0								
LDHI	Initialize H and I	$(M:M+1)_X\RightarrowH\:R$	INH	27B0	-	8	_	_	_	_		_	_	
		$(M:M+1)_Y \Rightarrow I\;R$												
LDS	Load SP	$(M:M+1) \Rightarrow SP$	IND8, X	CF	ff	6	—	_	_	_	Δ	Δ	0	-
			IND8, Y	DF	ff	6								
			IND8, Z	EF	ff	6								
			IND16, X	17CF	gggg	6								
			IND16, Y	17DF	gggg	6								
			IND16, Z	17EF	gggg	6								
			EXT	17FF	hh ll	6								
			IMM16	37BF	jj kk	4								
LDX	Load IX	$(M : M + 1) \Rightarrow IX$	IND8, X	CC	ff	6	—	_	_		Δ	Δ	0	
			IND8, Y	DC	ff	6								
			IND8, Z	EC	ff	6								
			IMM16	37BC	jj kk	4								
			IND16, X	17CC	gggg	6								
			IND16, Y	17DC	gggg	6								
			IND16, Z	17EC	gggg	6								
			EXT	17FC	hh ll	6								
LDY	Load IY	$(M:M+1) \Rightarrow IY$	IND8, X	CD	ff	6	—	_	_	_	Δ	Δ	0	7
			IND8, Y	DD	ff	6								
			IND8, Z	ED	ff	6								
			IMM16	37BD	jj kk	4								
			IND16, X	17CD	gggg	6								
			IND16, Y	17DD	9999	6								
			IND16, Z	17ED	gggg	6								
			EXT	17FD	hh ll	6								
LDZ	Load IZ	$(M:M+1) \Rightarrow IZ$	IND8, X	CE	ff	6	—	_	_	_	Δ	Δ	0	-
		. ,	IND8, Y	DE	ff	6								
			IND8, Z	EE	ff	6								
			IMM16	37BE	jj kk	4								
			IND16, X	17CE	9999	6								
			IND16, Y	17DE	9999	6								
			IND16, Z	17EE	9999	6								
1														

Table 4-2 Instruction Set Summary (Continued)



NOTE

The external bus interface does not latch data when an external bus cycle is terminated by a bus error. When this occurs during an instruction prefetch, the IMB precharge state (bus pulled high, or \$FF) is latched into the CPU16 instruction register, with indeterminate results.

5.6.5.2 Double Bus Faults

Exception processing for bus error exceptions follows the standard exception processing sequence. Refer to **4.13 Exceptions** for more information. However, two special cases of bus error, called double bus faults, can abort exception processing.

BERR assertion is not detected until an instruction is complete. The BERR latch is cleared by the first instruction of the BERR exception handler. Double bus fault occurs in two ways:

- 1. When bus error exception processing begins, and a second BERR is detected before the first instruction of the exception handler is executed.
- 2. When one or more bus errors occur before the first instruction after a RESET exception is executed.

Multiple bus errors within a single instruction that can generate multiple bus cycles cause a single bus error exception after the instruction has been executed.

Immediately after assertion of a second BERR, the MCU halts and drives the HALT line low. Only a reset can restart a halted MCU. However, bus arbitration can still occur. Refer to **5.6.6 External Bus Arbitration** for more information. A bus error or address error that occurs after exception processing has been completed (during the execution of the exception handler routine, or later) does not cause a double bus fault. The MCU continues to retry the same bus cycle as long as the external hardware requests it.

5.6.5.3 Halt Operation

When HALT is asserted while BERR is not asserted, the MCU halts external bus activity after negation of DSACK. The MCU may complete the current word transfer in progress. For a long-word to byte transfer, this could be after S2 or S4. For a word to byte transfer, activity ceases after S2.

Negating and reasserting HALT according to timing requirements provides single-step (bus cycle to bus cycle) operation. The HALT signal affects external bus cycles only, so that a program that does not use external bus can continue executing. During dy-namically-sized 8-bit transfers, external bus activity may not stop at the next cycle boundary. Occurrence of a bus error while HALT is asserted causes the CPU16 to process a bus error exception.

When the MCU completes a bus cycle while the HALT signal is asserted, the data bus goes into a high-impedance state and the AS and DS signals are driven to their inactive states. Address, function code, size, and read/write signals remain in the same state.

M68HC16 Z SERIES USER'S MANUAL

SYSTEM INTEGRATION MODULE



The SIM clock synthesizer provides clock signals to the other MCU modules. After the clock is running and MSTRST is asserted for at least four clock cycles, these modules reset. V_{DD} ramp time and VCO frequency ramp time determine how long the four cycles take. Worst case is approximately 15 milliseconds. During this period, module port pins may be in an indeterminate state. While input-only pins can be put in a known state by external pull-up resistors, external logic on input/output or output-only pins during this time must condition the lines. Active drivers require high-impedance buffers or isolation resistors to prevent conflict.

Figure 5-20 is a timing diagram for power-on reset. It shows the relationships between RESET, V_{DD} , and bus signals.

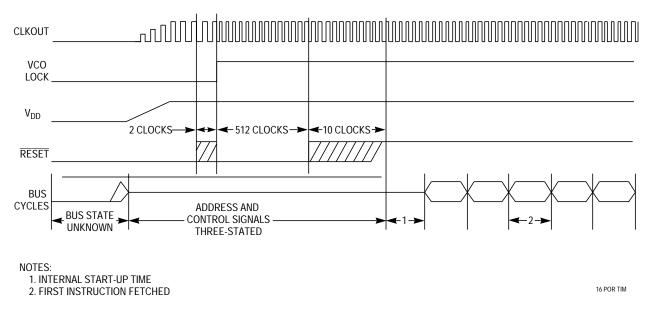


Figure 5-20 Power-On Reset

5.7.8 Use of the Three-State Control Pin

Asserting the three-state control (TSC) input causes the MCU to put all output drivers in a disabled, high-impedance state. The signal must remain asserted for approximately ten clock cycles in order for drivers to change state.

When the internal clock synthesizer is used (MODCLK held high during reset), synthesizer ramp-up time affects how long the ten cycles take. Worst case is approximately 20 milliseconds from TSC assertion.

When an external clock signal is applied (MODCLK held low during reset), pins go to high-impedance state as soon after TSC assertion as approximately ten clock pulses have been applied to the EXTAL pin.

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STANDBY RAM MODULE

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To ensure that the MCCI stops in a known state, assert the STOP bit before executing the CPU LPSTOP instruction. Before asserting the STOP bit, disable the SPI (clear the SPE bit) and disable the SCI receivers and transmitters (clear the RE and TE bits). Complete transfers in progress before disabling the SPI and SCI interfaces.

Once the STOP bit is asserted, it can be cleared by system software or by reset.

10.2.1.2 Privilege Levels

The supervisor bit (SUPV) in the MMCR has no effect since the CPU16 operates only in the supervisor mode.

10.2.1.3 MCCI Interrupts

The interrupt request level of each of the three MCCI interfaces can be programmed to a value of zero (interrupts disabled) through seven (highest priority). These levels are selected by the ILSCIA and ILSCIB fields in the SCI interrupt level register (ILSCI) and the ILSPI field in the SPI interrupt level register (ILSPI). In case two or more MCCI submodules request an interrupt simultaneously and are assigned the same interrupt request level, the SPI submodule is given the highest priority and SCIB is given the lowest.

When an interrupt is requested which is at a higher level than the interrupt mask in the CPU status register, the CPU initiates an interrupt acknowledge cycle. During this cycle, the MCCI compares its interrupt request level to the level recognized by the CPU. If a match occurs, arbitration with other modules begins.

Interrupting modules present their arbitration number on the IMB, and the module with the highest number wins. The arbitration number for the MCCI is programmed into the interrupt arbitration (IARB) field of the MMCR. Each module should be assigned a unique arbitration number. The reset value of the IARB field is \$0, which prevents the MCCI from arbitrating during an interrupt acknowledge cycle. The IARB field should be initialized by system software to a value from \$F (highest priority) through \$1 (lowest priority). Otherwise, the CPU identifies any interrupts generated as spurious and takes a spurious-interrupt exception.

If the MCCI wins the arbitration, it generates an interrupt vector that uniquely identifies the interrupting serial interface. The six MSBs are read from the interrupt vector (INTV) field in the MCCI interrupt vector register (MIVR). The two LSBs are assigned by the MCCI according to the interrupting serial interface, as indicated in Table 10-1.

Table 10-1 MCCI Interrupt Vectors

Interface	INTV[1:0]
SCIA	00
SCIB	01
SPI	10

MULTICHANNEL COMMUNICATION INTERFACE



10.5 MCCI Initialization

After reset, the MCCI remains in an idle state. Several registers must be initialized before serial operations begin. A general sequence guide for initialization follows.

- A. Global
 - 1. Configure MMCR
 - a. Write an interrupt arbitration number greater than zero into the IARB field. b. Clear the STOP bit if it is not already cleared.
 - 2. Interrupt vector and interrupt level registers (MIVR, ILSPI, and ILSCI) a. Write the SPI/SCI interrupt vector into MIVR.
 - b. Write the SPI interrupt request level into the ILSPI and the interrupt request levels for the two SCI interfaces into the ILSCI.
 - 3. Port data register
 - a. Write a data word to PORTMC.
 - b. Read a port pin state from PORTMCP.
 - 4. Pin control registers
 - a. Establish the direction of MCCI pins by writing to the MDDR.
 - b. Assign pin functions by writing to the MPAR.
- B. Serial Peripheral Interface
 - 1. Configure SPCR
 - a. Write a transfer rate value into the BAUD field.
 - b. Determine clock phase (CPHA) and clock polarity (CPOL).
 - c. Specify an 8- or 16-bit transfer (SIZE) and MSB- or LSB-first transfer mode (LSBF).
 - d. Select master or slave operating mode (MSTR).
 - e. Enable or disable wired-OR operation (WOMP).
 - f. Enable or disable SPI interrupts (SPIE).
 - g. Enable the SPI by setting the SPE bit.
- C. Serial Communication Interface (SCIA/SCIB)
 - 1. To transmit, read the SCSR, and then write transmit data to the SCDR. This clears the TDRE and TC indicators in the SCSR.
 - a. SCI control register 0 (SCCR0)
 - b. Write a baud rate value into the BR field.
 - 2. Configure SCCR1
 - a. Select 8- or 9-bit frame format (M).
 - b. Determine use (PE) and type (PT) of parity generation or detection.
 - c. To receive, set the RE and RIE bits in SCCR1. Select use (RWU) and type (WAKE) of receiver wakeup. Select idle-line detection type (ILT) and enable or disable idle-line interrupt (ILIE).
 - d. To transmit, set TE and TIE bits in SCCR1, and enable or disable WOMC and TCIE bits. Disable break transmission (SBK) for normal operation.



GENERAL-PURPOSE TIMER For More Information On This Product, Go to: www.freescale.com



Table A-7 Low Voltage Clock Control Timing

(V_{DD} and V_{DDSYN} = 2.7 to 3.6 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range ¹ MC68CM16Z1	f _{ref}	3.2	4.2	MHz
2	PLL Reference Frequency Range ¹ MC68CK16Z1 MC68CK16Z4	f _{ref}	20 20	50 50	kHz kHz
3	System Frequency ² On-Chip PLL System Frequency Slow On-Chip PLL System Frequency Fast On-Chip PLL System Frequency External Clock Operation	f _{sys}	dc 4 (f _{ref}) 4 (f _{ref}) /128 dc	16.78 16.78 16.78 16.78 16.78	MHz
4	PLL Lock Time ^{1, 7, 8, 9} Changing W or Y in SYNCR or exiting from LPSTOP ³ Warm Start-Up ⁴ Cold Start-Up (fast reference option only) ⁵	t _{ipii}	_	20 50 75	ms
5	VCO Frequency ⁶	f _{VCO}	—	2 (f _{sys} max)	ms
6	Limp Mode Clock Frequency SYNCR X bit = 0 SYNCR X bit = 1	f _{limp}	_	f _{sys} max /2 f _{sys} max	MHz
7	CLKOUT Jitter ^{1, 7, 8, 9, 10} Short term (5 μs interval) Long term (500 μs interval)	J _{clk}	-0.5 -0.05	0.5 0.05	%

NOTES:

1. Refer to notes in Table A-10.



Table A-11 Low Voltage 16.78-MHz DC Characteristics

(V_{DD} and V_{DDSYN} = 2.7 to 3.6Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	V _{IH}	0.7 (V _{DD})	V _{DD} + 0.3	V
2	Input Low Voltage	V _{IL}	$V_{SS} - 0.3$	0.2 (V _{DD})	V
3	Input Hysteresis ¹	V _{HYS}	0.5	—	V
4	Input Leakage Current ² $V_{in} = V_{DD}$ or V_{SS} Input-only pins	I _{in}	-2.5	2.5	μΑ
5	High Impedance (Off-State) Leakage Current ² $V_{in} = V_{DD}$ or V_{SS} All input/output and output pins	I _{OZ}	-2.5	2.5	μΑ
6	CMOS Output High Voltage ^{2, 3} $I_{OH} = -10.0 \ \mu A$ Group 1, 2, 4 input/output and output pins	V _{OH}	V _{DD} –0.2		V
7	CMOS Output Low Voltage ² $I_{OL} = 10.0 \mu A$ Group 1, 2, 4 input/output and output pins	V _{OL}	_	0.2	V
8	Output High Voltage ^{2, 3} $I_{OH} = -0.4 \text{ mA}$ Group 1, 2, 4 input/output and output pins	V _{OH}	V _{DD} –0.5		V
9	Output Low Voltage ² $I_{OL} = 0.8 \text{ mA Group 1 I/O pins, CLKOUT, FREEZE/QUOT, IPIPE0}$ $I_{OL} = 2.6 \text{ mA Group 2 and group 4 I/O pins, CSBOOT, BG/CS}$ $I_{OL} = 6 \text{ mA Group 3}$	V _{OL}	 	0.4 0.4 0.4	V
10	Three State Control Input High Voltage	VIHTSC	7.2	9.1	V
11	Data Bus Mode Select Pull-up Current ⁴ $V_{in} = V_{IL}$ $V_{in} = V_{IH}$	I _{MSP}	— —8	-95 	μA
12	V_{DD} Supply Current ⁵ Run ⁶ LPSTOP, 4.194 MHz crystal, VCO Off (STSIM = 0) ⁷ LPSTOP, 32.768 kHz crystal, VCO Off (STSIM = 0) ⁷ LPSTOP, external clock input frequency = max f _{sys} WAIT ⁸	I _{DD} S _{IDD} S _{IDD} S _{IDD} W _{IDD}	 	50 2 260 3.0 23	mA mA μA mA mA
13	Clock Synthesizer Operating Voltage	V _{DDSYN}	2.7	3.6	V
14	$\begin{array}{l} \text{MC68CM16Z1V}_{\text{DDSYN}} \text{ Supply Current}^{4} \\ \text{VCO on, crystal reference, maximum } {f_{\text{sys}}}^{7} \\ \text{External clock, maximum } {f_{\text{sys}}} \\ \text{LPSTOP, 4.194 MHz crystal reference, VCO off (STSIM = 0)}^{7} \\ \text{V}_{\text{DD}} \text{ powered down} \end{array}$	I _{DDSYN}	 	2 2.5 2 2	mA mA mA mA
14A	$\begin{array}{l} MC68CK16Z1/Z4 \ V_{DDSYN} \ Supply \ Current^4 \\ VCO \ on, \ crystal \ reference, \ maximum \ f_{\mathsf{sys}^7 \\ External \ clock, \ maximum \ f_{\mathsf{sys}} \\ LPSTOP, \ 32.768 \ kHz \ crystal \ reference, \ \mathsf{VCO \ off \ (STSIM = 0)^7 \\ 32.768 \ kHz, \ V_{\mathsf{DD} \ powered \ down \end{array}$	I _{DDSYN}	 	655 2.5 150 70	μA mA μA μA
15	RAM Standby Voltage ⁹ Specified V _{DD} applied V _{DD} = V _{SS}	V _{SB}	0.0 2.7	V _{DD} 3.6	V
16	$\label{eq:constraint} \begin{array}{ll} \text{MC68CK16Z1/Z4 RAM Standby Current}^{4, \ 9, \ 10} \\ \text{Normal RAM operation} & V_{\text{DD}} > V_{\text{SB}} - 0.5 \ \text{V} \\ \text{Transient condition} & V_{\text{SB}} - 0.5 \ \text{V} \geq V_{\text{DD}} \geq V_{\text{SS}} + 0.5 \ \text{V} \\ \text{Standby operation} & V_{\text{DD}} < V_{\text{SS}} + 0.5 \ \text{V} \end{array}$	I _{SB}	 	10 3 50	μA mA μA

ELECTRICAL CHARACTERISTICS



Table A-16 16.78-MHz AC Timing

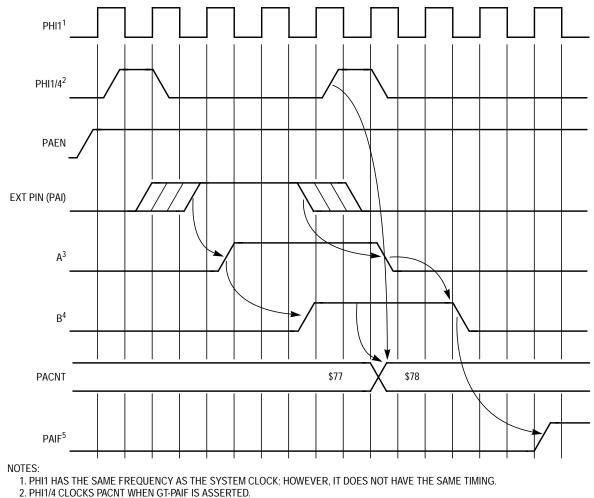
 $(V_{DD} \text{ and } V_{DDSYN} = 5.0 \text{ Vdc} \pm 10 \text{ \%}, V_{SS} = 0 \text{ Vdc}, T_A = T_L \text{ to } T_H)^1$

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation	f		16.78	MHz
1	Clock Period	t _{cyc}	59.6	—	ns
1A	ECLK Period	t _{Ecyc}	476	—	ns
1B	External Clock Input Period ²	t _{Xcyc}	59.6	—	ns
2, 3	Clock Pulse Width ³	t _{CW}	24	—	ns
2A, 3A	ECLK Pulse Width	t _{ECW}	236	—	ns
2B, 3B	External Clock Input High/Low Time ²	t _{XCHL}	29.8	—	ns
4, 5	CLKOUT Rise and Fall Time	t _{Crf}	_	5	ns
4A, 5A	Rise and Fall Time (All Outputs except CLKOUT)	t _{rf}	_	8	ns
4B, 5B	External Clock Input Rise and Fall Time ³	t _{XCrf}	_	5	ns
6	Clock High to ADDR, FC, SIZE Valid ⁴	t _{CHAV}	0	29	ns
7	Clock High to ADDR, Data, FC, SIZE, High Impedance	t _{CHAZx}	0	59	ns
8	Clock High to ADDR, FC, SIZE, Invalid	t _{CHAZn}	0	—	ns
9	Clock Low to \overline{AS} , \overline{DS} , \overline{CS} Asserted ⁴	t _{CLSA}	2	24	ns
9A	$\overline{\text{AS}}$ to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ Asserted (Read) ⁵	t _{STSA}	-15	15	ns
11	ADDR, FC, SIZE Valid to \overline{AS} , \overline{CS} , (and \overline{DS} Read) Asserted	t _{AVSA}	15	—	ns
12	Clock Low to AS, DS, CS Negated	t _{CLSN}	2	29	ns
13	AS, DS, CS Negated to ADDR, FC SIZE Invalid (Address Hold)	t _{SNAI}	15	—	ns
14	$\overline{\text{AS}}$, $\overline{\text{CS}}$ (and $\overline{\text{DS}}$ Read) Width Asserted	t _{SWA}	100	—	ns
14A	DS, CS Width Asserted (Write)	t _{SWAW}	45	—	ns
14B	$\overline{\text{AS}}$, $\overline{\text{CS}}$ (and $\overline{\text{DS}}$ Read) Width Asserted (Fast Cycle)	t _{SWDW}	40	—	ns
15	AS, DS, CS Width Negated ⁶	t _{SN}	40	—	ns
16	Clock High to AS, DS, R/W High Impedance	t _{CHSZ}	_	59	ns
17	AS, DS, CS Negated to R/W High	t _{SNRN}	15	—	ns
18	Clock High to R/W High	t _{CHRH}	0	29	ns
20	Clock High to R/W Low	t _{CHRL}	0	29	ns
21	R/\overline{W} High to \overline{AS} , \overline{CS} Asserted	t _{RAAA}	15	—	ns
22	R/\overline{W} Low to \overline{DS} , \overline{CS} Asserted (Write)	t _{RASA}	70	-	ns
23	Clock High to Data Out Valid	t _{CHDO}	_	29	ns
24	Data Out Valid to Negating Edge of AS, CS (Fast Write Cycle)	t _{DVASN}	15	—	ns
25	DS, CS Negated to Data Out Invalid (Data Out Hold)	t _{SNDOI}	15	—	ns
26	Data Out Valid to $\overline{\text{DS}}$, $\overline{\text{CS}}$ Asserted (Write)	t _{DVSA}	15	-	ns
27	Data In Valid to Clock Low (Data Setup) ⁴	t _{DICL}	5	—	ns
27A	Late BERR, HALT Asserted to Clock Low (Setup Time)	t _{BELCL}	20	-	ns
28	AS, DS Negated to DSACK[1:0], BERR, HALT, AVEC Negated	t _{SNDN}	0	80	ns
29	$\overline{\text{DS}}$, $\overline{\text{CS}}$ Negated to Data In Invalid (Data In Hold) ⁷	t _{SNDI}	0	-	ns
29A	DS, CS Negated to Data In High Impedance ^{7, 8}	t _{SHDI}		55	ns

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3. A = PAI SIGNAL AFTER THE SYNCHRONIZER.

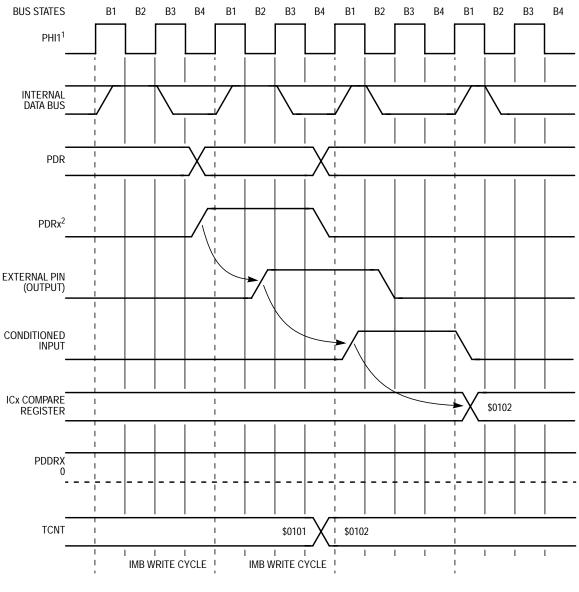
4. B = "A" AFTER THE DIGITAL FILTER.

5. PAIF IS ASSERTED WHEN PAI IS NEGATED.

PULSE ACCUM GATED MODE

Figure A-26 Pulse Accumulator — Gated Mode (Count While Pin High)





NOTES:

1. PHI1 IS THE SAME FREQUENCY AS THE SYSTEM CLOCK; HOWEVER, IT DOES NOT HAVE THE SAME TIMING.

2. WHEN THE BIT VALUE IS DRIVEN ON THE PIN, THE INPUT CIRCUIT SEES THE SIGNAL. AFTER IT IS CONDITIONED,

IT CAUSES THE CONTENTS OF THE TCNT TO BE LATCHED INTO THE ICX COMPARE REGISTER.

GENERAL PURPOSE OUTPUT

Figure A-32 General-Purpose Output (Causes Input Capture)



Device	Crystal Input	Operating Voltage	Package Type	Temperature	Frequency (MHz)	Package Order Quantity	Order Number
MC68HC16Z4	32 kHz	5 V	144-Pin	–40 to +85°C	16 MHz	2	SPMCK16Z4CPV16
			TQFP			60	MCK68HC16Z4CPV16
						300	MCK16Z4CPV16B1
					20 MHz	2	SPMCK16Z4CPV20
						60	MCK68HC16Z4CPV20
						300	MCK16Z4CPV20B1
					25 MHz	2	SPMCK16Z4CPV25
						60	MCK68HC16Z4CPV25
						300	MCK16Z4CPV25B1
				-40 to +105°C	16 MHz	2	SPMCK16Z4VPV16
						60	MCK68HC16Z4VPV16
						300	MCK16Z4VPV16B1
					20 MHz	2	SPMCK16Z4VPV20
						60	MCK68HC16Z4VPV20
						300	MCK16Z4VPV20B1
					25 MHz	2	SPMCK16Z4VPV25
						60	MCK68HC16Z4VPV25
						300	MCK16Z4VPV25B1
				-40 to +125°C	16 MHz	2	SPMCK16Z4MPV16
						60	MCK68HC16Z4MPV16
						300	MCK16Z4MPV16B1
					20 MHz	2	SPMCK16Z4MPV20
						60	MCK68HC16Z4MPV20
						300	MCK16Z4MPV20B1
		2.7 V	132-Pin	_40 to +85°C	16 MHz	2	SPMCCK16Z4CFC16
			PQFP			36	MC68CK16Z4CFC16
						180	MCCK16Z4CFC16B1
			144-Pin	–40 to +85°C	16 MHz	2	SPMCCK16Z4CPV16
			TQFP			60	MC68CK16Z4CPV16
						300	MCCK16Z4CPV16B1

 Table B-1 M68HC16 Z-Series Ordering Information (Continued)

 (Shaded cells indicate preliminary part numbers)



ROM	BS0 -	– RO	М Во	otstra	p Wo	rd 0								\$YFF	-830
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NOT	USED			ZK[3:0]			SK[[3:0]			PK	[3:0]	
ROM	BS1 -	– RO	М Во	otstra	p Wo	rd 1								\$YFF	832
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							PC[15:0]							
ROM	BS2 -	– RO	М Во	otstra	p Wo	rd 2								\$YFF	834
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							SP[15:0]							
ROM	BS3 -	– RO	M Bo	otstra	p Wo	rd 3								\$YFF	-836
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							IZ[1	5:0]							

Typically, CPU16 reset vectors reside in non-volatile memory and are fetched when the CPU16 comes out of reset. These four words can be used as reset vectors with the contents specified at mask time. The content of these words cannot be changed. On generic (blank ROM) MC68HC16Z2 and MC68HC16Z3 devices, ROMBS[0:3] are masked to \$0000. When the ROM on the MC68HC16Z2 and MC68HC16Z3 is masked with customer specific code, ROMBS[0:3] respond to system addresses \$00000 to \$00006 during the reset vector fetch if $\overline{BOOT} = 0$.

D.4.4 ROM Bootstrap Words

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	JSR AIX BRA	SEND_CH #\$01 SEND_STRING	;go send out the byte ;increment IX to point to the next byte ;loop back and do next byte in string
STRING_	JSR	DELAY	; wait for a moment
	RTS		;go back to whence we came
SEND_CH	:		;subroutine to send out one byte to SCI
	LDAA	SCSR	;read SCI status reg to check/clear TDRE bit
	ANDA	#\$01	check only the TDRE flag bit
	BEQ	SEND_CH	;if TDR is not empty, go back to check it ;again
	LDAA	#\$00	;clear A to send a full word to SCDR (\$FFCOE)
	STD	SCDR	itransmit one ASCII character to the screen
L00P5:	LDAB	SCSR+1	
	ANDB	#\$80	;test the TC bit (transfer complete)
	BEQ	LOOP5	;continue to wait until TC is set
	RTS		return to send_string subroutine;
* * * * *	The STRI	INGs ****	
STRING	DC	'The System Clo	ock is now running at 16.777 MHz',0a,0d,00
SEC_STR	-	'check this out	-
STRING2			ock is now running at 4.194 MHz',0a,0d,00
* * * * *	Interrup	pts/Exceptions *	****
BDM:	BGND		;exception vectors point here
BDM:	BGND		<pre>;exception vectors point here ;and put the user into background debug mode</pre>
		e 4 - Software Wat	;and put the user into background debug mode
	Example		; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo
E.2.1.4	Example	ption : This prog	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog,
E.2.1.4	Example	ption : This prog the perio	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector.
E.2.1.4 *	Example	ption : This prog the perio The perio	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog,
E.2.1.4 * * *	Example	otion : This prog the perio The perio on the du	;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated
E.2.1.4 * * *	Example	ption : This prog the perio The perio on the du will forc is pulled	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will
E.2.1.4 * * * * *	Example	ption : This prog the perio The perio on the du will forc is pulled "feed" th	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will he watchdog with \$55 and \$AA, and the
E.2.1.4 * * * * * *	Example	ption : This prog the perio The perio on the du will forc is pulled "feed" th	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will
E.2.1.4 * * * * * * * * * *	Example Descrip	ption : This prog the perio The perio on the du will ford is pulled "feed" th clock wil	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will he watchdog with \$55 and \$AA, and the
E.2.1.4 * * * * * * * * * *	Example Descrip	ption : This prog the perio The perio on the du will forc is pulled "feed" th clock wil	; and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will ne watchdog with \$55 and \$AA, and the .1 run without being reset on the dummy terminal.
E.2.1.4 * * * * * * * * * *	Example Descrig	etion : This prog the perio The perio on the du will forc is pulled "feed" th clock wil	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will ne watchdog with \$55 and \$AA, and the .1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip	ption : This prog the perio The perio on the du will ford "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the .1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip ******** INCLUDE INCLUDE	ption : This prog the perio The perio on the du will ford "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated mmy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the .1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrig ******** INCLUDE INCLUDE INCLUDE	etion : This prog the perio The perio on the du will ford is pulled "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo pram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the 1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip ******** INCLUDE INCLUDE	ption : This prog the perio The perio on the du will ford "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the 1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip ******** INCLUDE INCLUDE INCLUDE	ption : This prog the perio The perio on the du will ford "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo pram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the 1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip ******** INCLUDE INCLUDE INCLUDE	ption : This prog the perio The perio on the du will ford "feed" th clock wil ************************************	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo gram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 I low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the 1 run without being reset on the dummy terminal. ************************************</pre>
E.2.1.4 * * * * * * * * * *	Example Descrip ******** INCLUDE INCLUDE INCLUDE ORG DC.W	<pre>ption : This prog the perio The perio on the du will ford is pulled "feed" th clock wil ************************************</pre>	<pre>;and put the user into background debug mode tchdog, Periodic Interrupt, and Autovector Demo pram demonstrates the software watchdog, odic interrupt, and an autovector. odic interrupt runs a clock which is updated ummy terminal. Every eight seconds the COP se a reset unless IRQ6 is grounded. When IRQ6 1 low, an autovectored interrupt routine will be watchdog with \$55 and \$AA, and the .1 run without being reset on the dummy terminal. ************************************</pre>
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INITIALIZATION AND PROGRAMMING EXAMPLES



E.2.3 QSM/SCI Programming Example

The following programming example involves using a port of the serial communication interface (SCI), one of the serial interfaces of the queued serial module (QSM), to display a message on a dummy terminal.

Refer to **SECTION 9 QUEUED SERIAL MODULE** for more information on the QSM or the SCI.

E.2.3.1 Example 6 - Using an SCI Port

```
*
    Description : This program uses the SCI port to display
                  a shameless message on a dummy terminal. It includes
*
                  a subroutine to print a single character to the SCI
*
                  and a subroutine that uses the single character
*
                  subroutine to print an entire string.
INCLUDE 'EQUATES.ASM'
                                 ;table of EQUates for common register
addresses
       INCLUDE 'ORG00000.ASM'
                                 ; initialize reset vector
       INCLUDE 'ORG00008.ASM'
                                 ; initialize interrupt vectors
        ORG $0200
                                 ;start program after exception vector table
***** Initialize *****
INIT:
       INCLUDE 'INITSYS.ASM'
                                 ; initially set EK=F, XK=0, YK=0, ZK=0
                                 ;set sys clock at 16.78 MHz, disable COP
       INCLUDE 'INITRAM.ASM'
                                 ;turn on internal SRAM at $10000
                                 ;set stack (SK=1, SP=03FE)
       INCLUDE 'INITSCI.ASM'
                                 ;set the SCI baud rate to 9600 baud
                                 ;enable the SCI receiver and transmitter
       LDAB #$00
       TBXK
                                 ;set XK to bank 0 for STRING access
       LDAB #$01
       TBZK
                                 ;set ZK to bank 1 for delay counter access
       LDZ #$0000
                                 ;clear IZ for later use with delay counter
***** Main Program
                    * * * * *
MAIN
       LDX #STRING
                                 ; point to the beginning of ASCII string
       JSR SEND STRING
                                 ; go output the ASCII string
       BRA MAIN
                                 ; branch back to main
***** Subroutines *****
SEND STRING:
                           ; subroutine to send out the entire ASCII string
       LDAB 0,X
                          ;get next byte in string as pointed to by IX
       BEQ STRING_DONE
                          ; if B=00, then goto delay between messages
       JSR SEND CH
                          ;go send out the byte
```

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