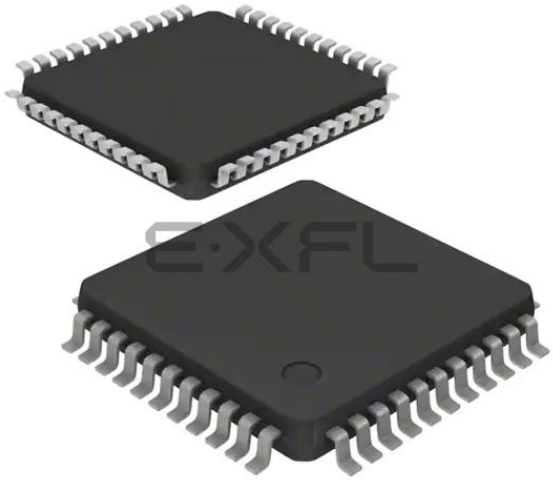


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | - |
| Number of I/O | 24 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 236 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86c9320fsc |

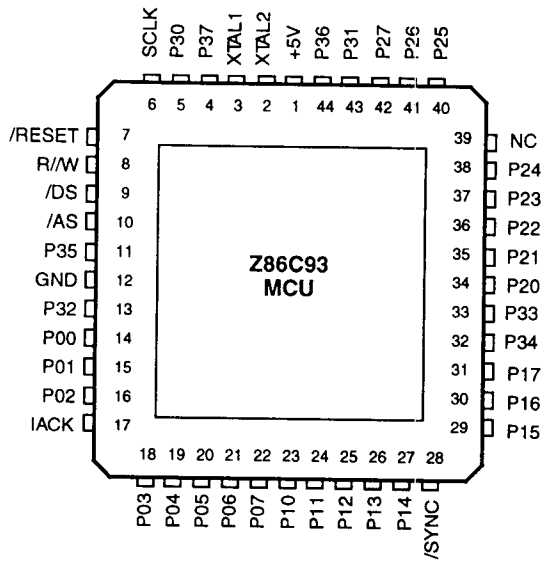



**Figure 4. 44-Pin PLCC**

**Table 2. 44-Pin PLCC Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | Input |
| 2 | XTAL2 | Crystal, Osc. Clock | Output |
| 3 | XTAL1 | Crystal, Osc. Clock | Input |
| 4 | P37 | Port 3 pin 7 | Output |
| 5 | P30 | Port 3 pin 0 | Input |
| 6 | SCLK | System Clock | Output |
| 7 | /RESET | Reset | Input |
| 8 | R/W | Read/Write | Output |
| 9 | /DS | Data Strobe | Output |
| 10 | /AS | Address Strobe | Output |
| 11 | P35 | Port 3 pin 5 | Output |
| 12 | GND | Ground GND | Input |
| 13 | P32 | Port 3 pin 2 | Input |

| No | Symbol | Function | Direction |
|---|---|---|---|
| 14-16 | P00-P02 | Port 0 pin 0,1,2 | In/Output |
| 17 | IACK | Int. Acknowledge | Output |
| 18-22 | P03-P07 | Port 0 pin 3,4,5,6,7 | In/Output |
| 23-27 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output |
| 28 | /SYNC | Synchronize Pin | Output |
| 29-31 | P15-P17 | Port 1 pin 5,6,7 | In/Output |
| 32 | P34 | Port 3 pin 4 | Output |
| 33 | P33 | Port 3 pin 3 | Input |
| 34-38 | P20-P24 | Port 2 pin 0,1,2,3,4 | In/Output |
| 39 | N/C | Not Connected (20 MHz) | Input |
| | /WAIT | WAIT (25 or 33 MHz) | Input |
| 40-42 | P25-P27 | Port 2 pin 5,6,7 | In/Output |
| 43 | P31 | Port 3 pin 1 | Input |
| 44 | P36 | Port 3 pin 6 | Output |

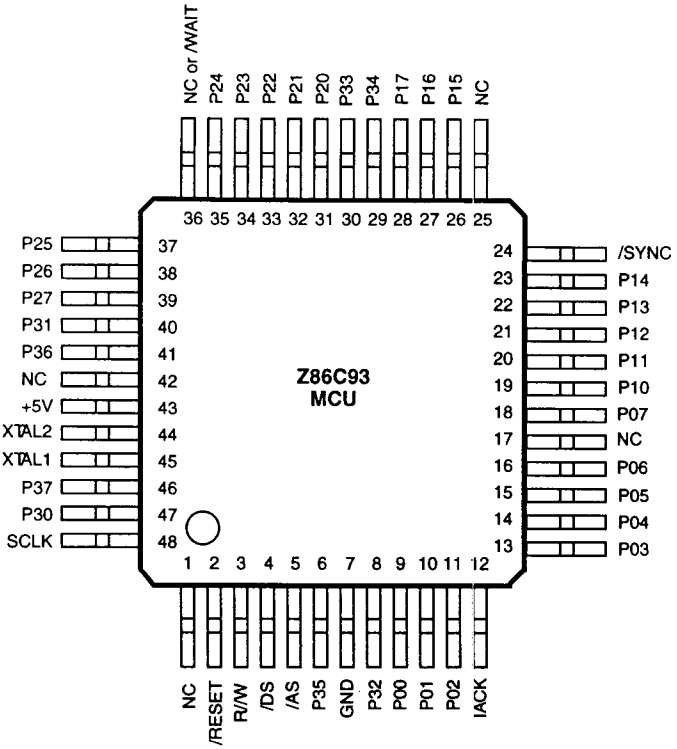



**Figure 6. 48-Pin VQFP Package**

**Table 4. 48-Pin VQFP Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | N/C | Not Connected | Input |
| 2 | /RESET | Reset | Input |
| 3 | R/W | Read/Write | Output |
| 4 | /DS | Data Strobe | Output |
| 5 | /AS | Address Strobe | Output |
| 6 | P35 | Port 3 pin 5 | Input |
| 7 | GND | Ground GND | Input |
| 8 | P32 | Port 3 pin 2 | Input |
| 9-11 | P00-P02 | Port 0 pin 3,4,5,6 | In/Output |
| 12 | IACK | Int. Acknowledge | Output |
| 13-16 | P03-P06 | Port 0 pin 3,4,5,6 | In/Output |
| 17 | N/C | Not Connected | Input |
| 18 | P07 | Port 0 pin 7 | In/Output |
| 19-23 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output |
| 24 | /SYNC | Synchronize Pin | Output |

| No | Symbol | Function | Direction |
|---|---|---|---|
| 25 | N/C | Not Connected | Input |
| 26-28 | P15-P17 | Port 1 pin 5,6,7 | In/Output |
| 29 | P34 | Port 3 pin 4 | Output |
| 30 | P33 | Port 3 pin 33 | Input |
| 31-35 | P20-P24 | Port 2 pin 0,1,2,3,4 | In/Output |
| 36 | N/C | Not Connected (20 MHz) | Input |
| | /WAIT | WAIT (25 or 33 MHz) | Input |
| 37-39 | P25-P27 | Port 2 pin 5,6,7 | In/Output |
| 40 | P31 | Port 3 pin 1 | Input |
| 41 | P36 | Port 3 pin 6 | Output |
| 42 | N/C | Not Connected | Input |
| 43 | $V_{cc}$ | Power Supply | Input |
| 44 | XTAL2 | Crystal, Osc. Clock | Output |
| 45 | XTAL1 | Crystal, Osc. Clock | Input |
| 46 | P37 | Port 3 pin 7 | Output |
| 47 | P30 | Port 3 pin 0 | Input |
| 48 | SCLK | System Clock | Output |

## PIN FUNCTIONS

**/DS.** (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

**/AS.** (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is via Port 1 for all external programs. When /RESET is asserted, /AS toggles. Memory address transfers are valid at the trailing edge of /AS.

**XTAL1, XTAL2.** *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

**R/W.** (output, read High/write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory. It is High when the MCU is reading from the external program or data memory.

**/RESET.** (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C93 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the 5th clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of 2TpC. When /RESET is deactivated, program execution begins at location 000CH. Reset time must be held Low for 50 ms or until $V_{CC}$ is stable, whichever is longer.

**SCLK.** *System Clock* (output). The internal system clock is available at this pin. Available in the PLCC, QFP and VQFP packages only.

**IACK.** *Interrupt Acknowledge* (output, active High). This output, when High, indicates that the Z86C93 is in an interrupt cycle. Available in the PLCC, QFP and VQFP packages only.

**/SYNC.** (output, active Low). This signal indicates the last clock cycle of the currently executing instruction. Available in the PLCC, QFP and VQFP packages only.

**/WAIT.** (input, active Low). Introduces asynchronous wait states into the external memory fetch cycle. When this inut goes Low during an external memory access, the Z86C93 freezes the fetch cycle until tis pin goes High. This pin is sampled after /DS goes Low; should be pulled up if not used. Available in the 25 MHz and 33 MHz dev ices only.

**Port 0 P00-P07.** Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble to be under handshake control. Port 0 comes up as A15-A8 Address lines after /RESET.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 7). The /OEN (Output Enable) signal in Figure 7 is an internal signal.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

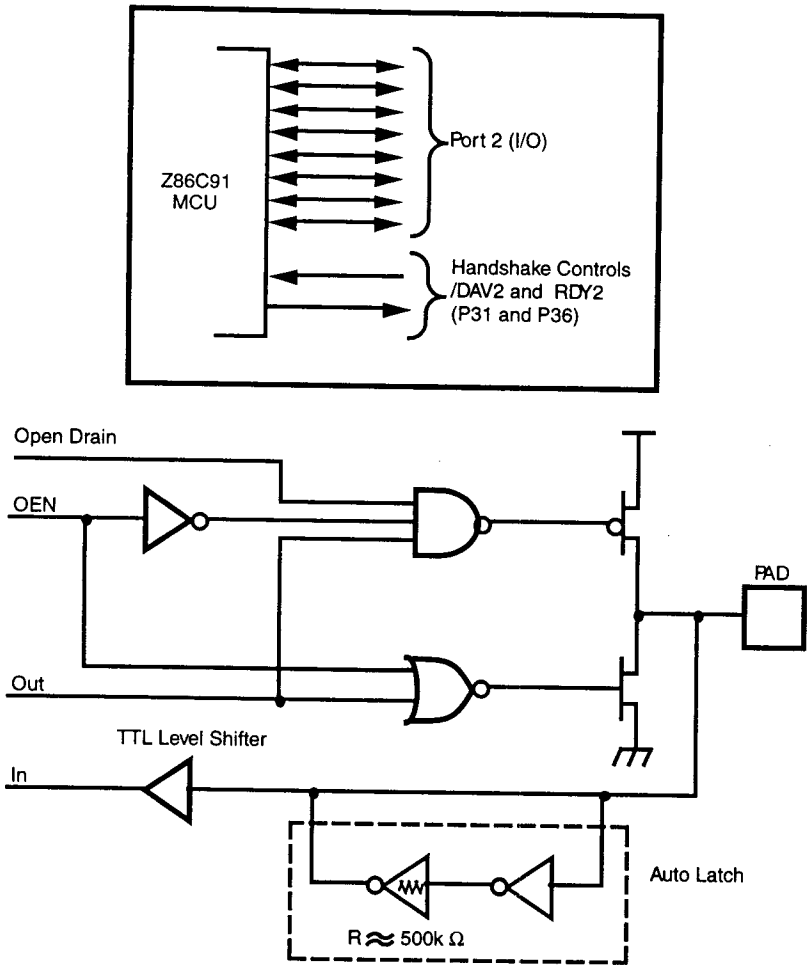



**Figure 9. Port 2 Configuration**

**Port 3 P30-P37.** Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

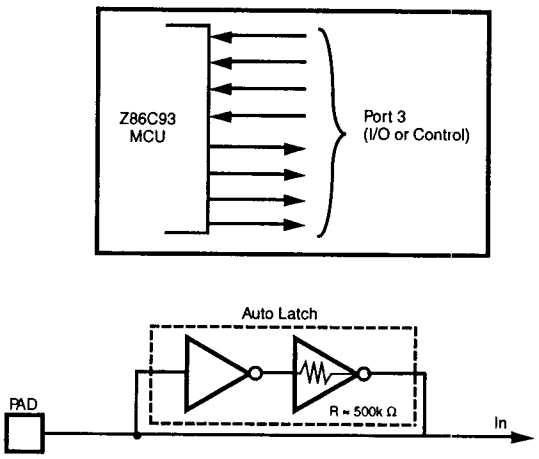



**Figure 10. Port 3 Configuration**

**Table 5. Port 3 Pin Assignments**

| Pin # | I/O | CTC1 | Int. | P0HS | P2HS | UART | Ext. |
|---|---|---|---|---|---|---|---|
| P30 | In | | IRQ3 | | | Serial In | |
| P31 | In | $T_{IN}$ | IRQ2 | | D/R | | |
| P32 | In | | IRQ0 | D/R | | | |
| P33 | In | | IRQ1 | | | | |
| P34 | Out | | | | | | DM |
| P35 | Out | | | R/D | | | |
| P36 | Out | $T_{OUT}$ | | | R/D | | |
| P37 | Out | | | | | Serial Out | |

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals ($T_{IN}$ and $T_{OUT}$), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

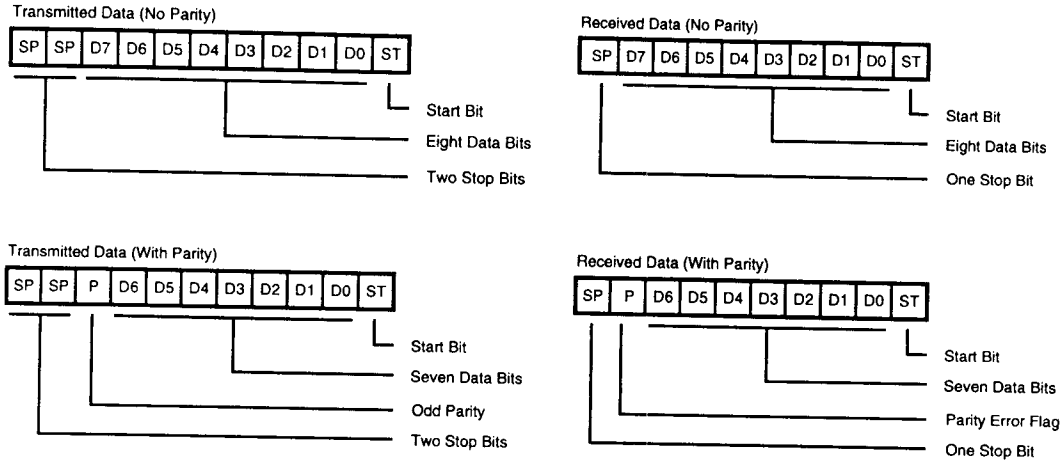



**Figure 11. Serial Data Formats**

## ADDRESS SPACE

Program Memory. The Z86C93 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory. The Z96C93 can address up to 64 Kbytes of external data memory. External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34 is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

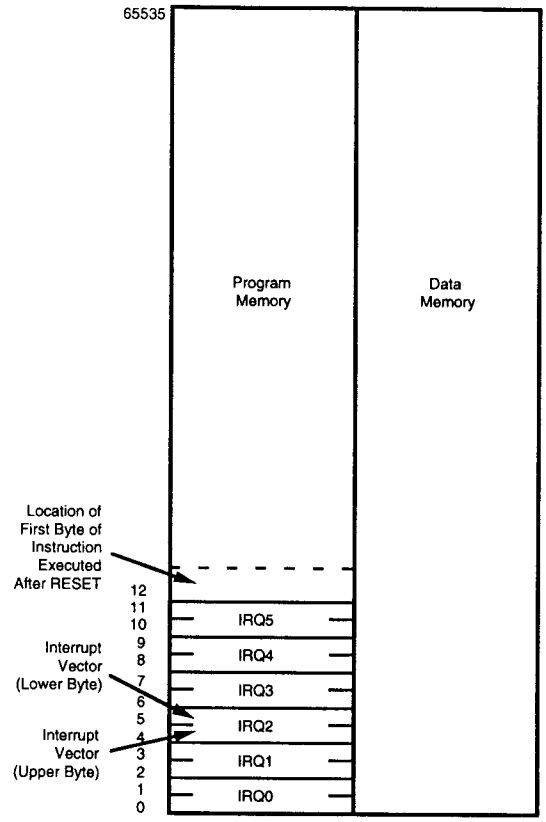



**Figure 12. Program and Data Memory Configuration**

**Expanded Register File.** The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area (Figure 13). The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14). The registers that are used in the multiply/divide unit reside in the Expanded Register File at Bank E and those for the additional timer control words reside in Bank D. The rest of the Expanded Register is not physically implemented and is open for future expansion.

**Register File.** The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers. The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C93 also allows short 4-bit register addressing using the Register Pointer (Figure 15). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

**Note:** Register Group E0-EF can only be accessed through working registers and indirect addressing modes.

**Stack.** The Z86C93 has a 16-bit Stack Pointer (R254-R255), used for external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH, Bits 8-15) can be used as a general-purpose register when using internal stack only.

## FUNCTIONAL DESCRIPTION

This section breaks down the Z86C93 into its main functional parts.

### Multiply/Divide Unit

The Multiply/Divide unit describes the basic features, implementation details of the interface between the Z8 and the multiply/divide unit.

Basic features:

- 16-bit by 16-bit multiply with 32-bit product
- 32-bit by 16-bit divide with 16-bit quotient and 16-bit remainder
- Unsigned integer data format
- Simple interface to Z8

**Interface to Z8.** The following is a brief description of the register mapping in the multiply/divide unit and its interface to the Z8 (Figure 16).

The multiply/divide unit is interfaced like a peripheral. The only addressing mode available with the peripheral interface is register addressing. In other words, all of the operands are in the respective registers before a multiplication/division can start.

**Register mapping.** The registers used in the multiply/divide unit are mapped onto the expanded register file in Bank E. The exact register locations used are shown below.

| REGISTER | ADDRESS |
|---|---|
| MREG0 | (E) 00 |
| MREG1 | (E) 01 |
| MREG2 | (E) 02 |
| MREG3 | (E) 03 |
| MREG4 | (E) 04 |
| MREG5 | (E) 05 |
| MDCON | (E) 06 |
| GPR | (E) 14 |
| GPR | (E) 15 |

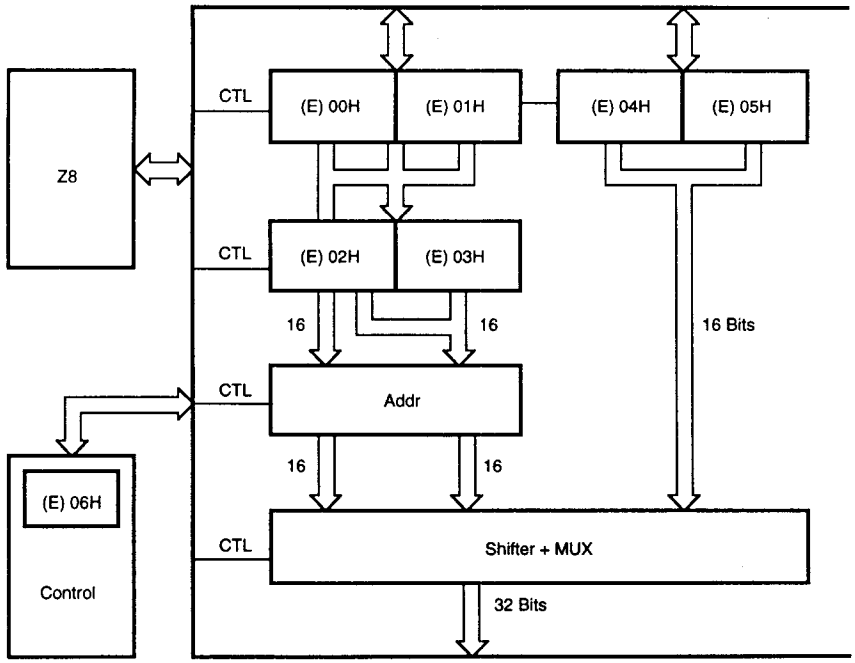



**Figure 16. Multiply/Divide Unit Block Diagram**

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. Either T0 or T1 can be outputted via P36.

The following are the enhancements made to the counter/timer block on the Z86C93 (Figure 18):

- T0 counter length is extended to 16 bits. For example, T0 now has a 6-bit prescaler and 16-bit down counter.
- T1 counter length is extended to 16 bits. For example, T1 now has a 6-bit prescaler and 16-bit down counter.
- A new counter/timer T2 is added. T2 has a 4-bit prescaler and a 16-bit down counter with capture register.

These three counters are cascadable as shown in Table 6. The result is that T2 may be extendable to 32 bits and T1 extendable to 24 bits. Bits 1 and 0 (CAS1 AND CAS0) of the T2 Prescaler Register (PRE2) determine the counter length.

**Table 6. Counter Length Configurations**

| CAS 1 | CAS0 | T0 | T1 | T2 |
|---|---|---|---|---|
| 0 | 0 | 8 | 8 | 32 |
| 0 | 1 | 16 | 16 | 16 |
| 1 | 0 | 8 | 24 | 16 |
| 1 | 1 | 8 | 16 | 24 |

The controlling clock input to T2 is programmed to XTAL/2 or XTAL/8 (only when T2 counter length is 16 bits), which results in a resolution of 100 ns at an external XTAL clock speed of 20 MHz.

Capture Register. T2 has a 16-bit capture register associated with T2 HIGH BYTE and T2 LOW BYTE registers. The negative going transition on pin P33 enables the latching of the current T2 value (16 bits) into the capture register. The register mapping of the capture register is in Bank D (Figure 13). Note that the negative transition on P33 is capable of generating an interrupt. Also, the negative transition on P33 always latches the current T2 value into the capture register. There is no need for a control bit to enable/disable the latching; the capture register is read only.

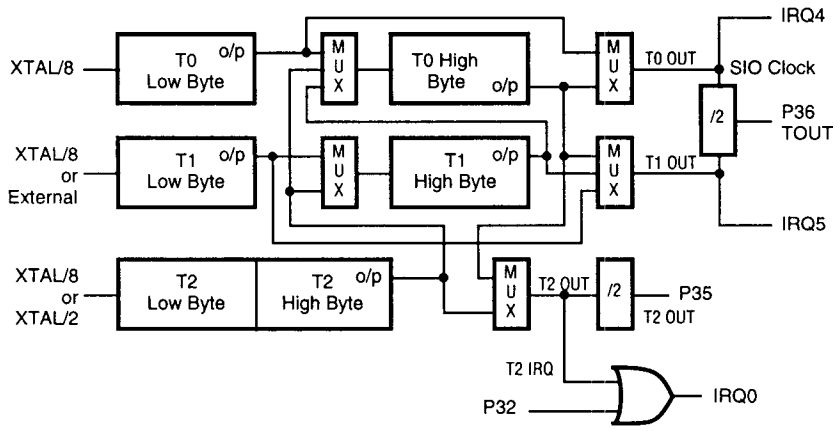



**Figure 18. Counter/Timer Block Diagram**

**Table 7. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ 0 | /DAV 0, P32, T2 | 0, 1 | External (P32), Programmable Rise or Fall Edge Triggered |
| IRQ 1, | P33 | 2, 3 | External (P33), Fall Edge Triggered |
| IRQ 2 | /DAV 2, P31, $T_{IN}$ | 4, 5 | External (P31), Programmable Rise or Fall Edge Triggered |
| IRQ 3 | P30, Serial In | 6, 7 | External (P30), Fall Edge Triggered |
| IRQ 4 | T0, Serial Out | 8, 9 | Internal |
| IRQ 5 | TI | 10, 11 | Internal |

## Clock

The Z86C93 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The external clock levels are not TTL. The crystal should be AT cut, 1 MHz to 25 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF<CL<100 pF) from each pin to ground (Figure 20).

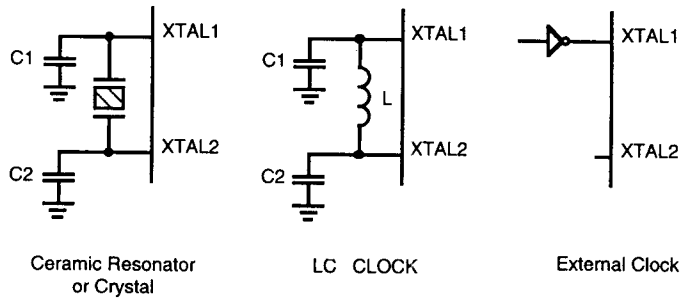



**Figure 22. Oscillator Configuration**

## Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
          or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage* | -0.3 | +7.0 | V |
| $T_{STG}$ | Storage Temp | -65 | +150 | C |
| $T_A$ | Oper Ambient Temp | † | † | C |

* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

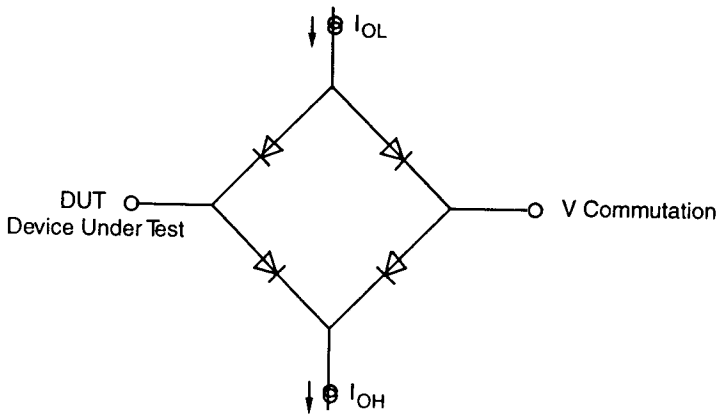



**Figure 23. Test Load Diagram**

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 3.3V ± 10%

| Sym | Parameter | $T_A$ = 0°C to +70°C Min | Max | Typical at 25°C | Units | Conditions |
|---|---|---|---|---|---|---|
| | Max Input Voltage | | 7 | | V | $I_{IN}$ 250 µA |
| $V_{CH}$ | Clock Input High Voltage | 0.8 $V_{CC}$ | $V_{CC}$ | | V | Driven by External Clock Generator |
| $V_{CL}$ | Clock Input Low Voltage | -0.03 | 0.1x$V_{CC}$ | | V | Driven by External Clock Generator |
| $V_{IH}$ | Input High Voltage | 0.7x$V_{CC}$ | $V_{CC}$ | | V | |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.1x$V_{CC}$ | | V | |
| $V_{OH}$ | Output High Voltge | 1.8 | | | V | $I_{OH}$ = -1.0 mA |
| $V_{OH}$ | Output High Voltge | $V_{CC}$ - 100mV | | | V | $I_{OH}$ = -100 µA |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | V | $I_{OL}$ = +1.0 mA |
| $V_{RH}$ | Reset Input High Voltage | 0.8x$V_{CC}$ | $V_{CC}$ | | V | |
| $V_{RI}$ | Reset Input Low Voltage | -0.03 | 0.1x$V_{CC}$ | | V | |
| $I_{IL}$ | Input Leakage | -2 | 2 | | µA | Test at 0V, $V_{CC}$ |
| $I_{OL}$ | Output Leakage | -2 | 2 | | µA | Test at 0V, $V_{CC}$ |
| $I_{IR}$ | Reset Input Current | | -80 | | µA | $V_{RL}$ = 0V |
| $I_{CC}$ | Supply Current | | 30 | 20 | mA | @ 25 MHz [1] |
| $I_{CC1}$ | Stand By Current (HALT Mode) | | 12 | 8 | mA | HALT Mode $V_{IN}$=0V, $V_{CC}$ @ 25 MHz [1] |
| $I_{CC2}$ | Stand By Current (HALT Mode) | | 8 | 1 | µA | STOP Mode $V_{IN}$=0V, $V_{CC}$ [1] |
| $I_{ALL}$ | Auto Latch Low Current | -10 | 10 | 5 | µA | |

**Note:**

[1] All inputs driven to 0V, $V_{CC}$ and outputs floating.

## AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

| | | | $T_A$ = 0°C to +70°C | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 25 MHz | | 20 MHz | | Typical | |
| No | Sym | Parameter | Min | Max | Min | Max | Min | Max | $V_{cc}$=5.0V @ 25°C | Units |
| 1 | TdA(AS) | Address Valid To /AS Rise Delay | 13 | | 22 | | 26 | | | ns |
| 2 | TdAS(A) | /AS Rise To Address Hold Time | 20 | | 25 | | 28 | | | ns |
| 3 | TdAS(DI) | /AS Rise Data In Req'd Valid Delay | | 90 | | 130 | | 160 | | ns |
| 4 | TwAS | /AS Low Width | 20 | | 28 | | 36 | | | ns |
| 5 | TdAZ(DSR) | Address Float To /DS (Read) | 0 | | 0 | | 0 | | | ns |
| 6 | TwDSR | /DS (Read) Low Width | 65 | | 100 | | 130 | | | ns |
| 7 | TwDSW | /DS (Write) Low Width | 40 | | 65 | | 75 | | | ns |
| 8 | TdDSR(DI) | /DS (Read) To Data in Req'd Valid Delay | | 30 | | 78 | | 100 | | ns |
| 9 | ThDSR(DI) | /DS Rise (Read) to Data In Hold Time | 0 | | 0 | | 0 | | | ns |
| 10 | TdDS(A) | /DS Rise To Address Active Delay | 25 | | 34 | | 40 | | | ns |
| 11 | TdDS(AS) | /DS Rise To /AS Delay | 16 | | 30 | | 36 | | | ns |
| 12 | TdR/W(AS) | R/W To /AS Rise Delay | 12 | | 26 | | 32 | | | ns |
| 13 | TdDS(R/W) | /DS Rise To R/W Valid Delay | 12 | | 30 | | 36 | | | ns |
| 14 | TdDO(DSW) | Data Out To /DS (Write) Delay | 12 | | 34 | | 40 | | | ns |
| 15 | ThDSW(DO) | /DS Rise (Write) To Data Out Hold Time | 12 | | 34 | | 40 | | | ns |
| 16 | TdA(DI) | Address To Data In Req'd Valid Delay | | 110 | | 160 | | 200 | | ns |
| 17 | TdAS(DSR) | /AS Rise To /DS (Read) Delay | 20 | | 40 | | 48 | | | ns |
| 18 | TaDI(DSR) | Data In Set-up Time To /DS Rise Read | 16 | | 30 | | 36 | | | ns |
| 19 | TdDM(AS) | /DM To /AS Rise Delay | 10 | | 22 | | 26 | | | ns |
| 20 | TdDS(DM) | /DS Rise To /DM Valid Delay | | | | | | | 34* | ns |
| 21 | ThDS(A) | /DS Rise To Address Valid Hold Time | | | | | | | 34* | ns |
| 22 | TdXT(SCR) | XTAL Falling to SCLK Rising | | | | | | | 20* | ns |
| 23 | TdXT(SCF) | XTAL Falling to SCLK Falling | | | | | | | 23* | ns |
| 24 | TdXT(DSRF) | XTAL Falling to/DS Read Falling | | | | | | | 29* | ns |
| 25 | TdXT(DSRR) | XTAL Falling to /DS Read Rising | | | | | | | 29* | ns |
| 26 | TdXT(DSWF) | XTAL Falling to /DS Write Falling | | | | | | | 29* | ns |
| 27 | TdXT(DSWF) | XTAL Falling to /DS Write Rising | | | | | | | 29* | ns |
| 28 | TsW(XT) | Wait Set-up Time | | | | | | | 10* | ns |
| 29 | ThW(XT) | Wait Hold Time | | | | | | | 15* | ns |
| 30 | TwW | Wait Width (One Wait Time) | | | | | | | 25* | ns |

**Notes:**
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
* Preliminary value to be characterized.

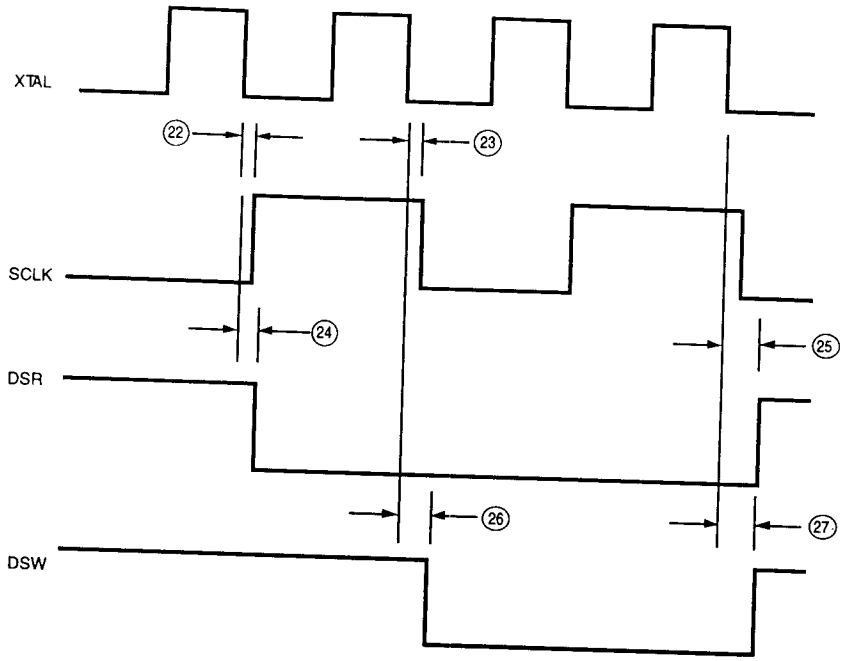



**Figure 25. XTAL/SCLK To DSR and DSW Timing**

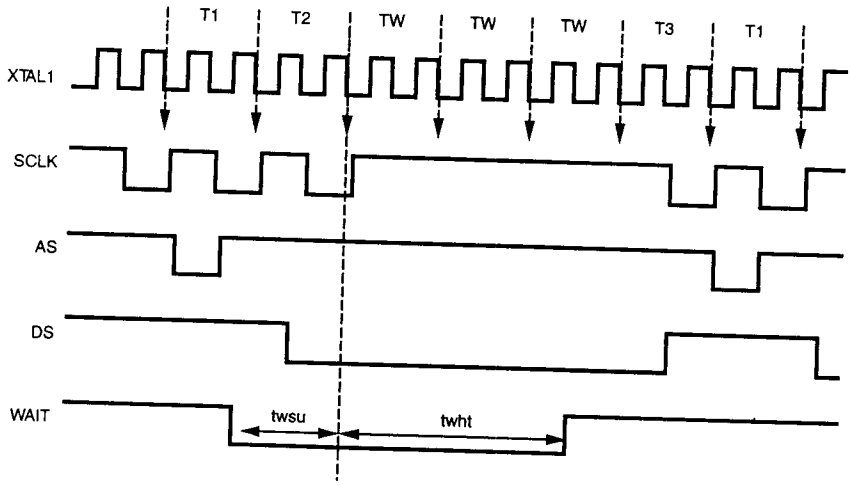



**Figure 26. XTAL/SCLK To WAIT Timing (25 MHz Device Only)**

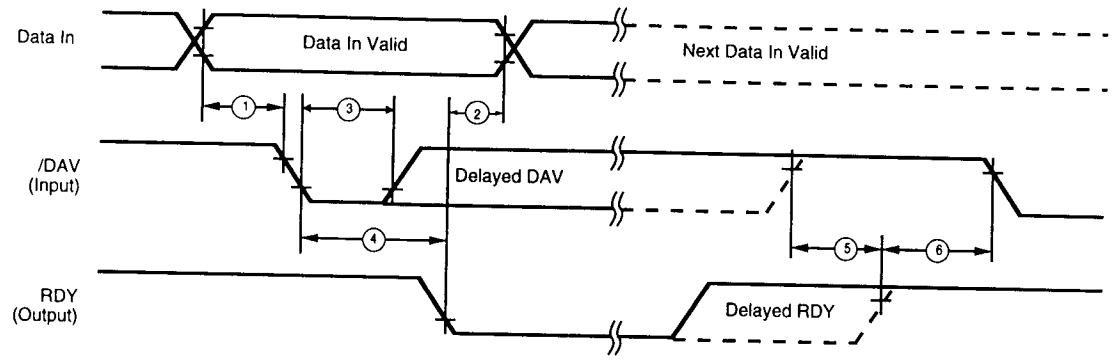



**Figure 28. Input Handshake Timing**

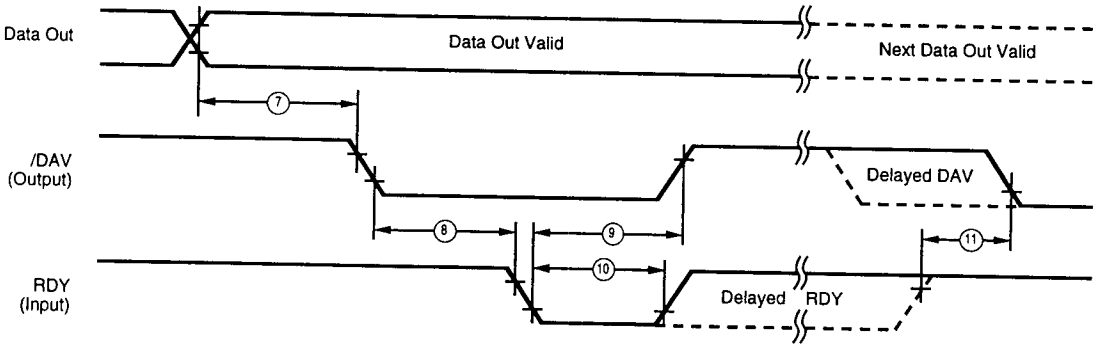


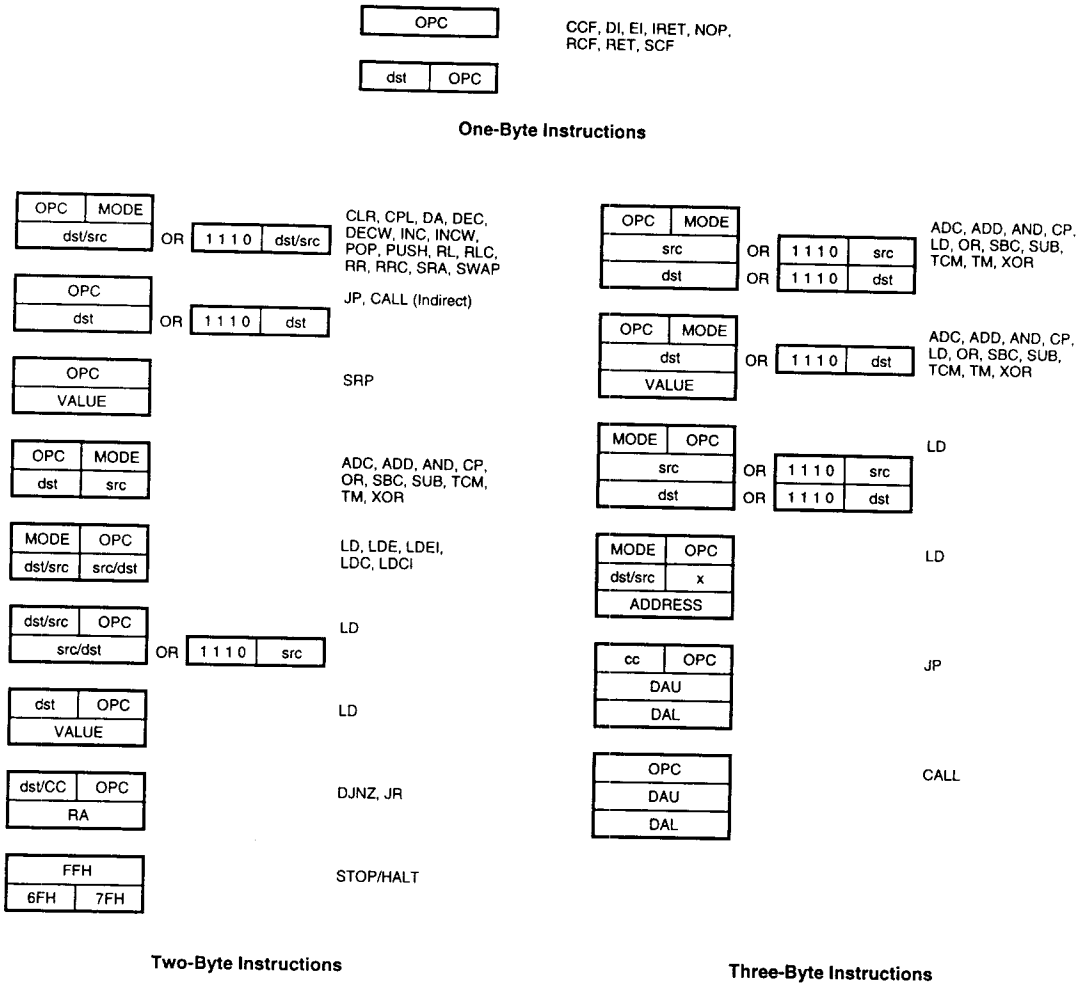

**Figure 29. Output Handshake Timing**

## AC CHARACTERISTICS

Handshake Timing Table

| No | Symbol | Parameter | $T_A$ = 0°C to +70°C Min | Max | Units | Data Direction |
|---|---|---|---|---|---|---|
| 1 | TsDI(DAV) | Data In Setup Time to /DAV | 0 | | ns | In |
| 2 | ThDI(DAV) | RDY to Data In Hold Time | 0 | | ns | In |
| 3 | TwDAV | /DAV Width | 40 | | ns | In |
| 4 | TdDAVIf(RDYf) | /DAV to RDY Delay | | 70 | ns | In |
| 5 | TdDAVIr(RDYr) | DAV Rise to RDY Wait Time | | 40 | ns | In |
| 6 | TdRDYOr(DAVIf) | RDY Rise to DAV Delay | 0 | | ns | In |
| 7 | TdDO(DAV) | Data Out to DAV Delay | | TpC | ns | Out |
| 8 | TdDAVOf(RDYIf) | /DAV to RDY Delay | 0 | | ns | Out |
| 9 | TdRDYIf(DAVOr) | RDY to /DAV Rise Delay | | 70 | ns | Out |
| 10 | TwRDY | RDY Width | 40 | | ns | Out |
| 11 | TdRDYIr(DAVOf) | RDY Rise to DAV Wait Time | | 40 | ns | Out |

## INSTRUCTION FORMATS




## INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

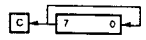
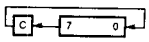
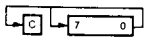
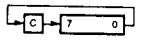
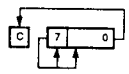
dst ← dst + src

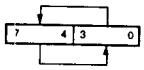
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

## INSTRUCTION SUMMARY (Continued)

| Instruction and Operation | Address Mode dst | Address Mode src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **NOP** | | | FF | - | - | - | - | - | - |
| **OR** dst, src<br>dst←dst OR src | † | | 4[ ] | - | * | * | 0 | - | - |
| **POP** dst<br>dst←@SP;<br>SP←SP + 1 | R<br>IR | | 50<br>51 | - | - | - | - | - | - |
| **PUSH** src<br>SP←SP - 1;<br>@SP←src | | R<br>IR | 70<br>71 | - | - | - | - | - | - |
| **RCF**<br>C←0 | | | CF | 0 | - | - | - | - | - |
| **RET**<br>PC←@SP;<br>SP←SP + 2 | | | AF | - | - | - | - | - | - |
| **RL** dst<br>  | R<br>IR | | 90<br>91 | * | * | * | * | - | - |
| **RLC** dst<br>  | R<br>IR | | 10<br>11 | * | * | * | * | - | - |
| **RR** dst<br>  | R<br>IR | | E0<br>E1 | * | * | * | * | - | - |
| **RRC** dst<br>  | R<br>IR | | C0<br>C1 | * | * | * | * | - | - |
| **SBC** dst, src<br>dst←dst←src←C | † | | 3[ ] | * | * | * | * | 1 | * |
| **SCF**<br>C←1 | | | DF | 1 | - | - | - | - | - |
| **SRA** dst<br>  | R<br>IR | | D0<br>D1 | * | * | * | 0 | - | - |
| **SRP** src<br>RP←src | | Im | 31 | - | - | - | - | - | - |

| Instruction and Operation | Address Mode dst | Address Mode src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **STOP** | | | 6F | - | - | - | - | - | - |
| **SUB** dst, src<br>dst←dst←src | † | | 2[ ] | * | * | * | * | 1 | * |
| **SWAP** dst<br>  | R<br>IR | | F0<br>F1 | X | * | * | X | - | - |
| **TCM** dst, src<br>(NOT dst)<br>AND src | † | | 6[ ] | - | * | * | 0 | - | - |
| **TM** dst, src<br>dst AND src | † | | 7[ ] | - | * | * | 0 | - | - |
| **XOR** dst, src<br>dst←dst<br>XOR src | † | | B[ ] | - | * | * | 0 | - | - |

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

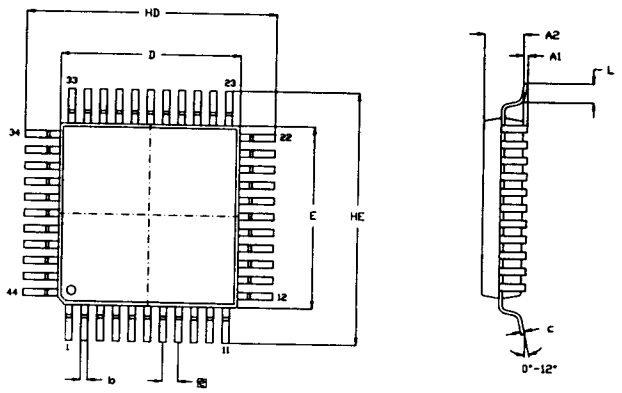
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

| Address Mode dst | Address Mode src | Lower Opcode Nibble |
|---|---|---|
| r | r | [2] |
| r | Ir | [3] |
| R | R | [4] |
| R | IR | [5] |
| R | IM | [6] |
| IR | IM | [7] |

## PACKAGE INFORMATION (Continued)

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

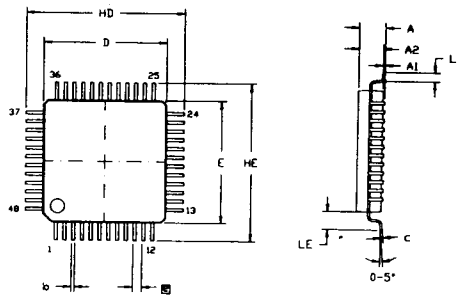
| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.05 | 0.25 | .002 | .010 |
| A2 | 2.05 | 2.25 | .081 | .089 |
| b | 0.25 | 0.45 | .010 | .018 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 13.70 | 14.30 | .539 | .563 |
| D | 9.90 | 10.10 | .390 | .398 |
| HE | 13.70 | 14.30 | .539 | .563 |
| E | 9.90 | 10.10 | .390 | .398 |
| e | 0.80 TYP | | .031 TYP | |
| L | 0.60 | 1.20 | .024 | .047 |




**44-Pin QFP Package Diagram**

| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.60 | .053 | .063 |
| A1 | 0.05 | 0.20 | .002 | .008 |
| A2 | 1.30 | 1.50 | .051 | .059 |
| b | 0.15 | 0.26 | .006 | .010 |
| c | 0.10 | 0.18 | .004 | .007 |
| HD | 8.60 | 9.40 | .339 | .370 |
| D | 6.90 | 7.10 | .272 | .280 |
| HE | 8.60 | 9.40 | .339 | .370 |
| E | 6.90 | 7.10 | .272 | .280 |
| e | 0.50 TYP | | .020 TYP | |
| L | 0.30 | 0.70 | .012 | .028 |
| LE | 0.90 | 1.10 | .035 | .043 |

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"




**48-Pin VQFP Package Diagram**

## ZILOG DOMESTIC SALES OFFICES AND TECHNICAL CENTERS

CALIFORNIA
Agoura ..... 818-707-2160
Campbell ..... 408-370-8120
Irvine ..... 714-453-9701

COLORADO
Boulder ..... 303-494-2905

FLORIDA
Largo ..... 813-585-2533

GEORGIA
Norcross ..... 404-448-9370

ILLINOIS
Schaumburg ..... 708-517-8080

MINNESOTA
Minneapolis ..... 612-944-0737

NEW HAMPSHIRE
Nashua ..... 603-888-8590

OHIO
Independence ..... 216-447-1480

OREGON
Portland ..... 503-274-6250

PENNSYLVANIA
Ambler ..... 215-653-0230

TEXAS
Dallas ..... 214-987-9987

WASHINGTON
Seattle ..... 206-523-3591

## INTERNATIONAL SALES OFFICES

CANADA
Toronto ..... 416-673-0634

GERMANY
Munich ..... 49-8967-2045
Sömmerda ..... 49-3634-23906

JAPAN
Tokyo ..... 81-3-3587-0528

HONG KONG
Kowloon ..... 852-7238979

KOREA
Seoul ..... 82-2-577-3272

SINGAPORE
Singapore ..... 65-2357155

TAIWAN
Taipei ..... 886-2-741-3125

UNITED KINGDOM
Maidenhead ..... 44-628-392-00



**Zilog, Inc. 210 East Hacienda Ave.**
**Campbell, CA 95008-6600**
**Telephone (408) 370-8000**
**Telex 910-338-7621**
**FAX 408 370-8056**