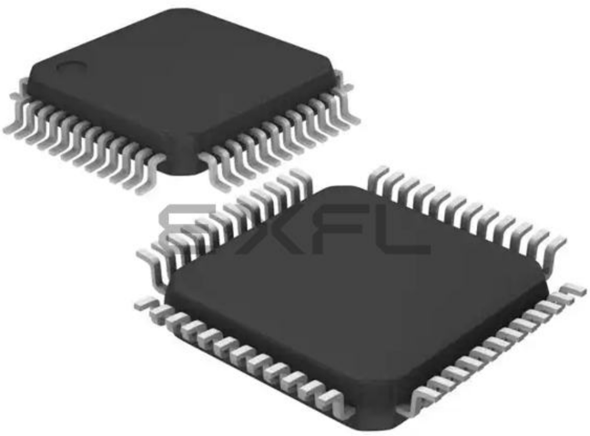


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9325asc

PRODUCT SPECIFICATION

Z86C93

CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.
- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.
- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.
- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.
- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Two 16-bit counter timers with 6-bit prescalers.
- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.
- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.
- Additional emulation signals SCLK, IACK, and /SYNC are made available.
- Two low power standby modes, STOP and HALT
- Full-duplex UART
- 3.3 ± 10% volt operation at 25 MHz
- 5.0 ± 10% volt operation at 20, 25 and 33 MHz

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and Counter/Timer blocks.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

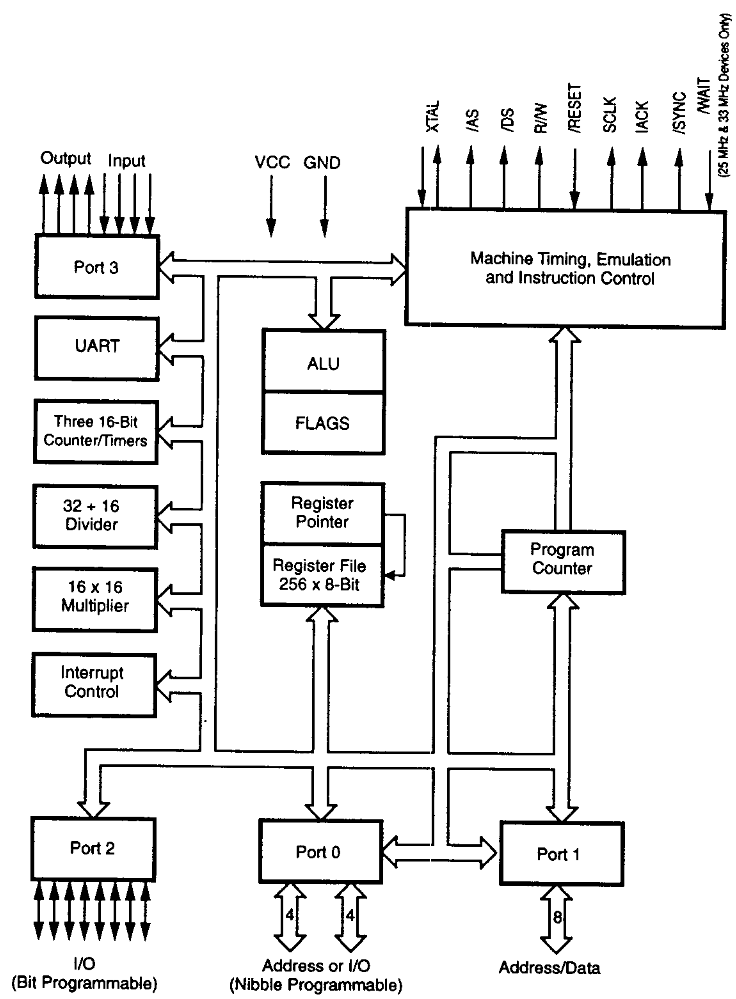


Figure 1. Functional Block Diagram

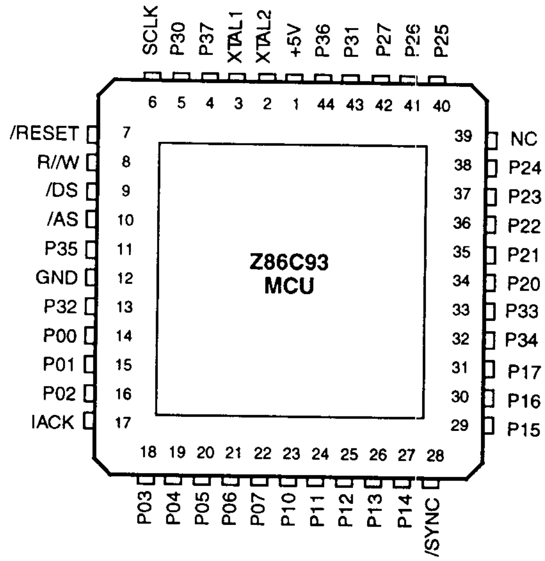


Figure 4. 44-Pin PLCC

Table 2. 44-Pin PLCC Pin Identification

No	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Osc. Clock	Output
3	XTAL1	Crystal, Osc. Clock	Input
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	SCLK	System Clock	Output
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3 pin 5	Output
12	GND	Ground GND	Input
13	P32	Port 3 pin 2	Input

No	Symbol	Function	Direction
14-16	P00-P02	Port 0 pin 0,1,2	In/Output
17	IACK	Int. Acknowledge	Output
18-22	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
23-27	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
28	/SYNC	Synchronize Pin	Output
29-31	P15-P17	Port 1 pin 5,6,7	In/Output
32	P34	Port 3 pin 4	Output
33	P33	Port 3 pin 3	Input
34-38	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
39	N/C	Not Connected (20 MHz)	Input
	/WAIT	WAIT (25 or 33 MHz)	Input
40-42	P25-P27	Port 2 pin 5,6,7	In/Output
43	P31	Port 3 pin 1	Input
44	P36	Port 3 pin 6	Output

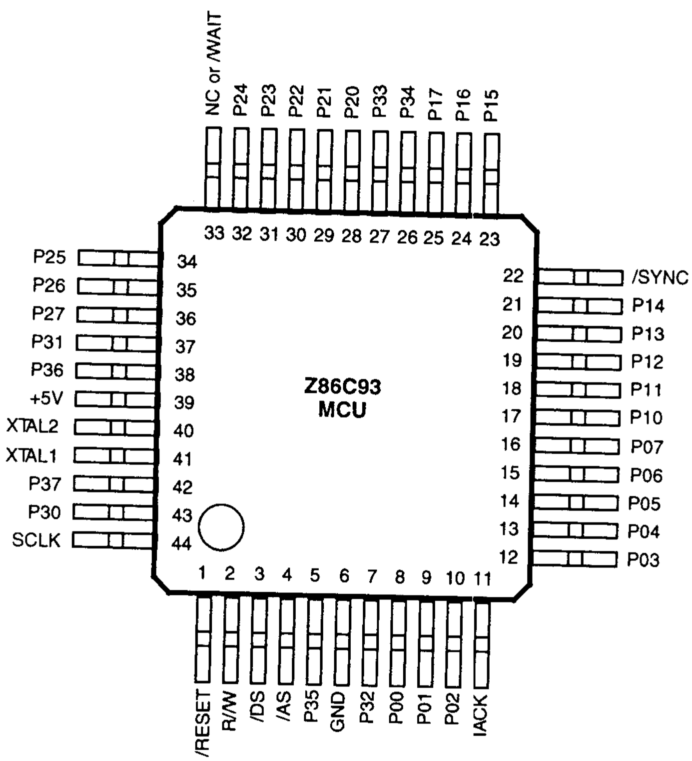


Figure 5. 44-Pin QFP

Table 3. 44-Pin QFP Pin Identification

No	Symbol	Function	Direction
1	/RESET	Reset	Input
2	R/W	Read/Write	Output
3	/DS	Data Strobe	Output
4	/AS	Address Strobe	Output
5	P35	Port 3 pin 5	Input
6	GND	Ground GND	Input
7	P32	Port 3 pin 2	Input
8-10	P00-P02	Port 0 pin 0,1,2	In/Output
11	IACK	Int. Acknowledge	Output
12-16	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
17-21	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
22	/SYNC	Synchronize Pin	Output
23-25	P15-P17	Port 1 pin 5,6,7	In/Output

No	Symbol	Function	Direction
26	P34	Port 3 pin 4	Output
27	P33	Port 3 pin 3	Input
28-32	P2C-P24	Port 2 pin 0,1,2,3,4	In/Output
33	N/C	Not Connected (20 MHz)	Input
	/WAIT	WAIT (25 or 33 MHz)	Input
34-36	P25-P27	Port 2 pin 5,6,7	In/Output
37	P31	Port 3 pin 1	Input
38	P36	Port 3 pin 6	Output
39	V_{CC}	Power Supply	Input
40	XTAL2	Crystal, Osc. Clock	Output
41	XTAL1	Crystal, Osc. Clock	Input
42	P37	Port 3 pin 7	Output
43	P30	Port 3 pin 0	Input
44	SCLK	System Clock	Output

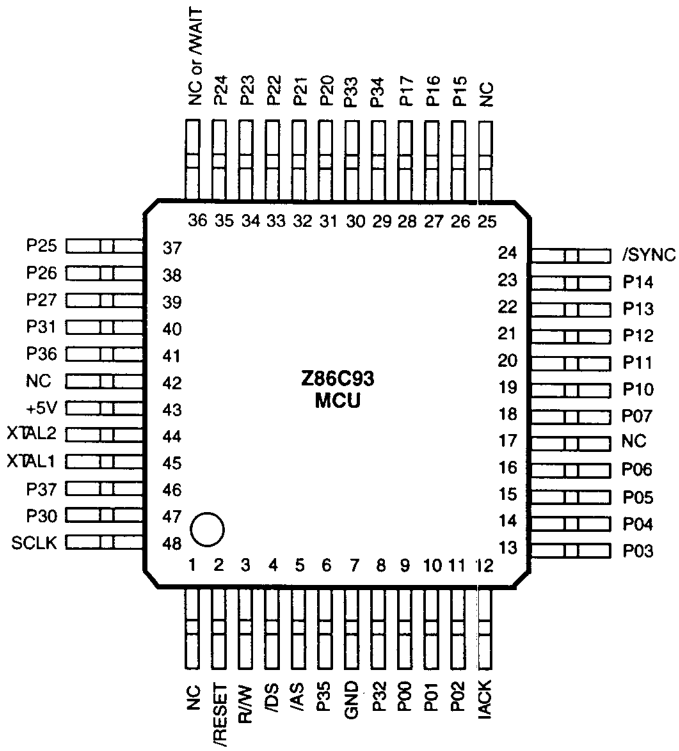


Figure 6. 48-Pin VQFP Package

Table 4. 48-Pin VQFP Pin Identification

No	Symbol	Function	Direction
1	N/C	Not Connected	Input
2	/RESET	Reset	Input
3	R/W	Read/Write	Output
4	/DS	Data Strobe	Output
5	/AS	Address Strobe	Output
6	P35	Port 3 pin 5	Input
7	GND	Ground GND	Input
8	P32	Port 3 pin 2	Input
9-11	P00-P02	Port 0 pin 3,4,5,6	In/Output
12	IACK	Int. Acknowledge	Output
13-16	P03-P06	Port 0 pin 3,4,5,6	In/Output
17	N/C	Not Connected	Input
18	P07	Port 0 pin 7	In/Output
19-23	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
24	/SYNC	Synchronize Pin	Output

No	Symbol	Function	Direction
25	N/C	Not Connected	Input
26-28	P15-P17	Port 1 pin 5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 33	Input
31-35	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
36	N/C	Not Connected (20 MHz)	Input
	/WAIT	WAIT (25 or 33 MHz)	Input
37-39	P25-P27	Port 2 pin 5,6,7	In/Output
40	P31	Port 3 pin 1	Input
41	P36	Port 3 pin 6	Output
42	N/C	Not Connected	Input
43	V_{CC}	Power Supply	Input
44	XTAL2	Crystal, Osc. Clock	Output
45	XTAL1	Crystal, Osc. Clock	Input
46	P37	Port 3 pin 7	Output
47	P30	Port 3 pin 0	Input
48	SCLK	System Clock	Output

PIN FUNCTIONS

/DS. (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS. (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is via Port 1 for all external programs. When /RESET is asserted, /AS toggles. Memory address transfers are valid at the trailing edge of /AS.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W. (output, read High/write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory. It is High when the MCU is reading from the external program or data memory.

/RESET. (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C93 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the 5th clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of 2TpC. When /RESET is deactivated, program execution begins at location 000CH. Reset time must be held Low for 50 ms or until V_{CC} is stable, whichever is longer.

SCLK. *System Clock* (output). The internal system clock is available at this pin. Available in the PLCC, QFP and VQFP packages only.

IACK. *Interrupt Acknowledge* (output, active High). This output, when High, indicates that the Z86C93 is in an interrupt cycle. Available in the PLCC, QFP and VQFP packages only.

/SYNC. (output, active Low). This signal indicates the last clock cycle of the currently executing instruction. Available in the PLCC, QFP and VQFP packages only.

/WAIT. (input, active Low). Introduces asynchronous wait states into the external memory fetch cycle. When this inut goes Low during an external memory access, the Z86C93 freezes the fetch cycle until tis pin goes High. This pin is sampled after /DS goes Low; should be pulled up if not used. Available in the 25 MHz and 33 MHz dev ices only.

Port 0 P00-P07. Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble to be under handshake control. Port 0 comes up as A15-A8 Address lines after /RESET.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 7). The /OEN (Output Enable) signal in Figure 7 is an internal signal.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

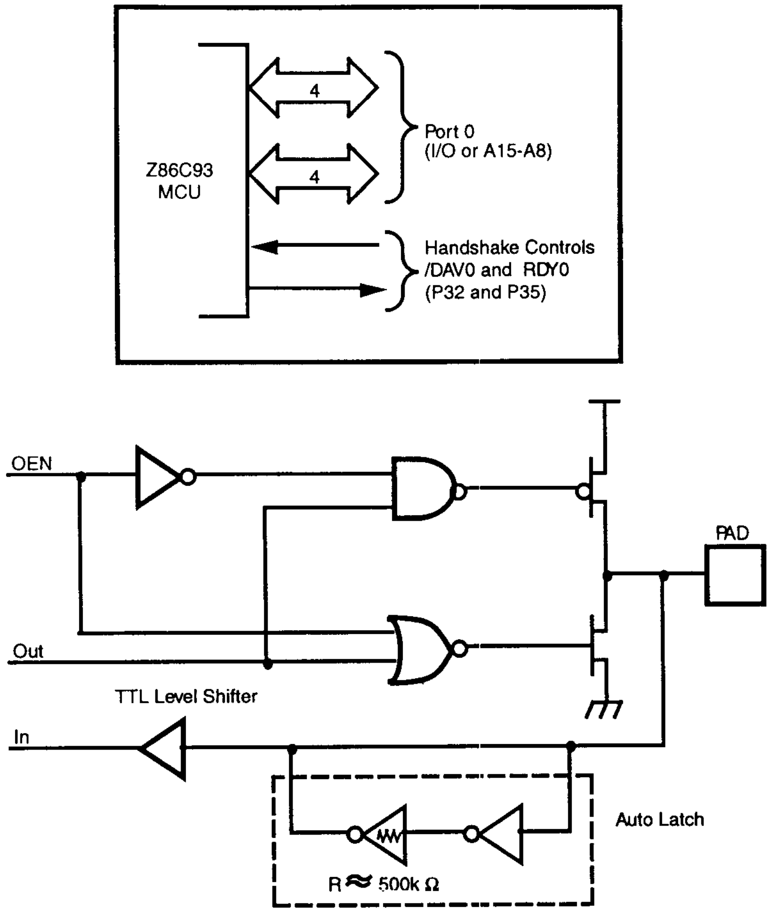


Figure 7. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1. (P10-P17). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory (Figure 8).

If more than 256 external locations are required, Port 0 must output the additional lines.

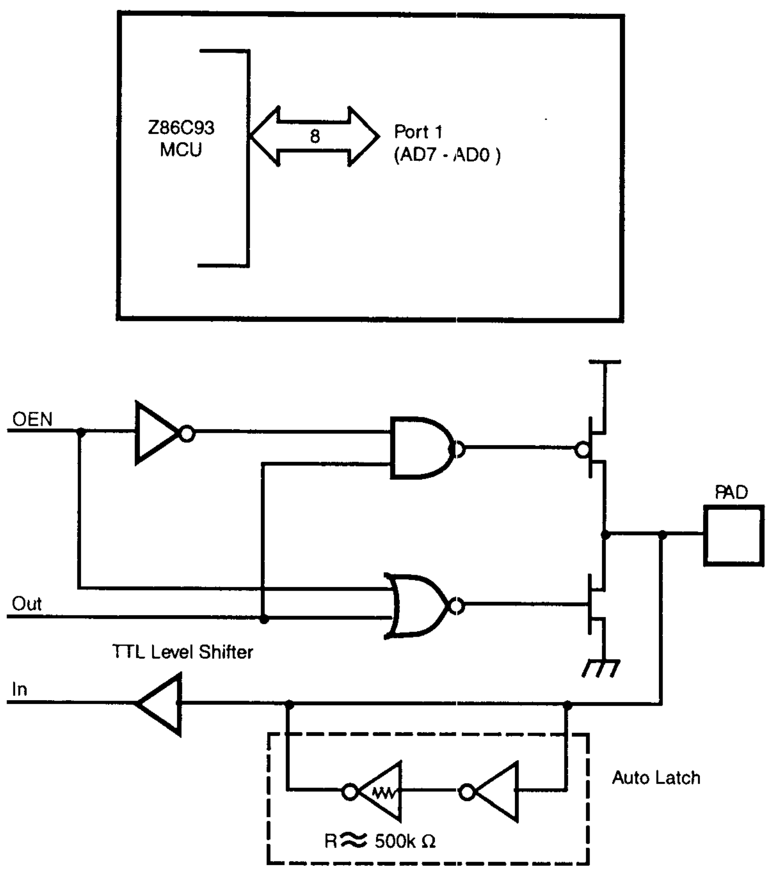


Figure 8. Port 1 Configuration

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

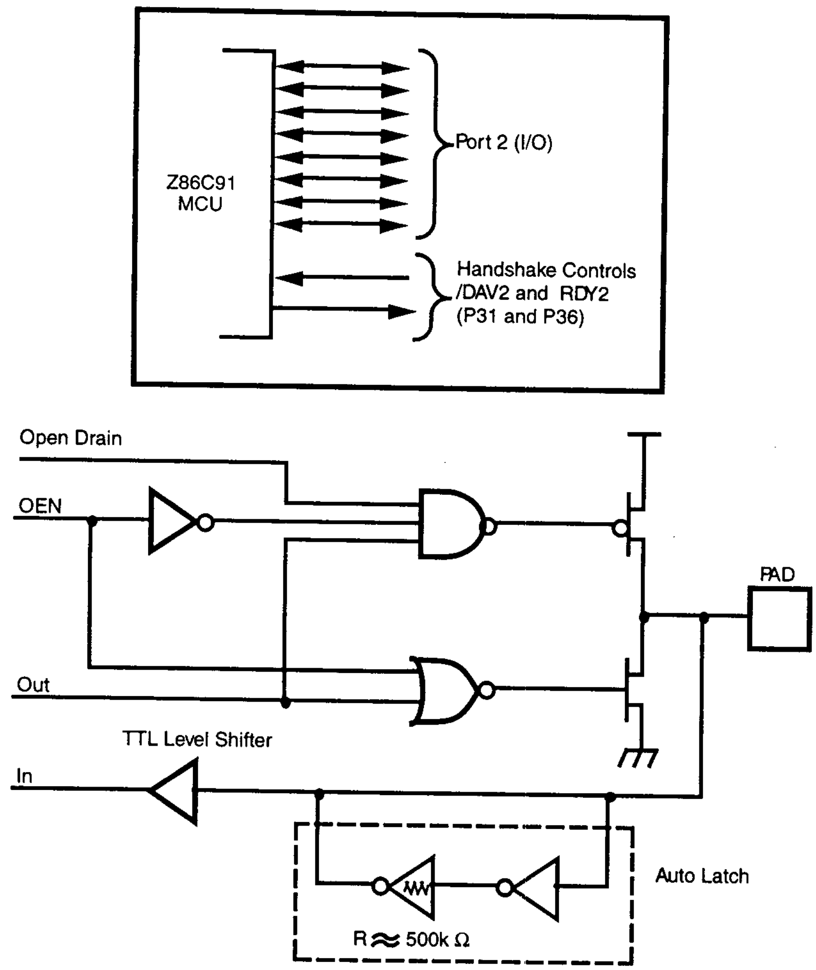


Figure 9. Port 2 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

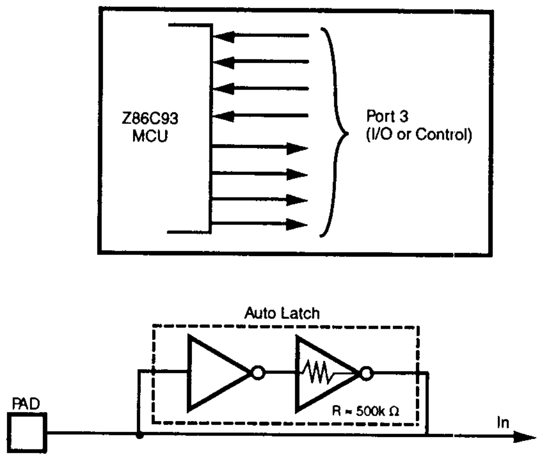


Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In		IRQ3			Serial In	
P31	In	T_{IN}	IRQ2		D/R		
P32	In		IRQ0	D/R			
P33	In		IRQ1				
P34	Out						DM
P35	Out			R/D			
P36	Out	T_{OUT}			R/D		
P37	Out					Serial Out	

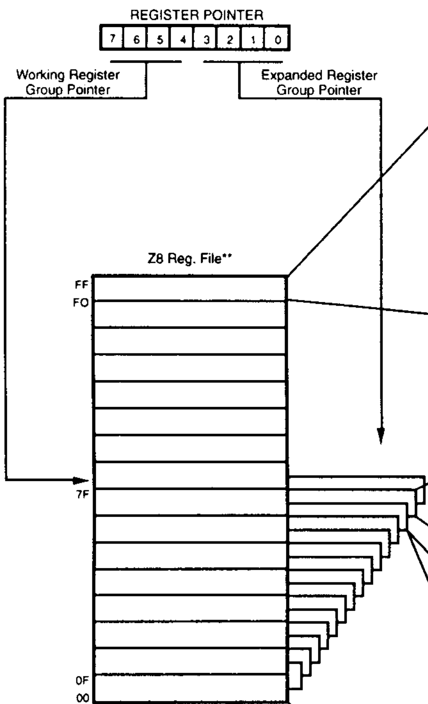
Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.



Z8 STANDARD CONTROL REGISTERS

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
FF	SPL	U	U	U	U	U	U	U	U
FE	SPH	U	U	U	U	U	U	U	U
FD	RP	U	U	U	U	U	U	U	U
FC	FLAGS	U	U	U	U	U	U	U	U
FB	IMR	0	U	U	U	U	U	U	U
FA	IRQ	0	0	0	0	0	0	0	0
F9	IPR	U	U	U	U	U	U	U	U
F8	P01M	1	1	1	1	0	1	1	1
F7	P3M	0	0	0	0	0	0	0	0
* F6	P2M	1	1	1	1	1	1	1	1
* F5	PRE0	U	U	U	U	U	U	U	0
F4	T0	U	U	U	U	U	U	U	U
F3	PRE1	U	U	U	U	U	U	0	0
F2	T1	U	U	U	U	U	U	U	U
F1	TMR	0	0	0	0	0	0	0	0
F0	SIO	U	U	U	U	U	U	U	U

EXPANDED REG. BANK (E)

REGISTER		RESET CONDITION							
(E) 15	GPR	U	U	U	U	U	U	U	U
(E) 14	GPR	U	U	U	U	U	U	U	U
(E) 13-7	Reserved								
(E) 6	MDCON	1	0	0	U	U	U	0	0
(E) 5	MREG5	U	U	U	U	U	U	U	U
(E) 4	MREG4	U	U	U	U	U	U	U	U
(E) 3	MREG3	U	U	U	U	U	U	U	U
(E) 2	MREG2	U	U	U	U	U	U	U	U
(E) 1	MREG1	U	U	U	U	U	U	U	U
(E) 0	MREG0	U	U	U	U	U	U	U	U

EXPANDED REG. BANK (D)

REGISTER		RESET CONDITION							
(D) 9	T2CAPL	U	U	U	U	U	U	U	U
(D) 8	T2CAPH	U	U	U	U	U	U	U	U
(D) 7	T2L	U	U	U	U	U	U	U	U
(D) 6	T2H	U	U	U	U	U	U	U	U
(D) 5	Reserved								
(D) 4	T0H	U	U	U	U	U	U	U	U
(D) 3	T2PRE	U	U	U	U	0	U	0	0
(D) 2	T1H	U	U	U	U	U	U	U	U
(D) 1	T2TMR	U	0	U	0	0	0	0	0
(D) 0	Reserved								

EXPANDED REG. BANK (0)

REGISTER		RESET CONDITION							
(0) 03	P3	1	1	1	1	U	U	U	U
(0) 02	P2	U	U	U	U	U	U	U	U
(0) 01	Reserved	U	U	U	U	U	U	U	U
(0) 00	P0	U	U	U	U	U	U	U	U

U = Unknown
* = Will not be reset with a STOP Mode Recovery
GPR = General Purpose Register
** = All addresses are in hexadecimal

Figure 13. Register File

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. Either T0 or T1 can be outputted via P36.

The following are the enhancements made to the counter/timer block on the Z86C93 (Figure 18):

- T0 counter length is extended to 16 bits. For example, T0 now has a 6-bit prescaler and 16-bit down counter.
- T1 counter length is extended to 16 bits. For example, T1 now has a 6-bit prescaler and 16-bit down counter.
- A new counter/timer T2 is added. T2 has a 4-bit prescaler and a 16-bit down counter with capture register.

These three counters are cascadable as shown in Table 6. The result is that T2 may be extendable to 32 bits and T1 extendable to 24 bits. Bits 1 and 0 (CAS1 AND CAS0) of the T2 Prescaler Register (PRE2) determine the counter length.

Table 6. Counter Length Configurations

CAS 1	CAS0	T0	T1	T2
0	0	8	8	32
0	1	16	16	16
1	0	8	24	16
1	1	8	16	24

The controlling clock input to T2 is programmed to XTAL/2 or XTAL/8 (only when T2 counter length is 16 bits), which results in a resolution of 100 ns at an external XTAL clock speed of 20 MHz.

Capture Register. T2 has a 16-bit capture register associated with T2 HIGH BYTE and T2 LOW BYTE registers. The negative going transition on pin P33 enables the latching of the current T2 value (16 bits) into the capture register. The register mapping of the capture register is in Bank D (Figure 13). Note that the negative transition on P33 is capable of generating an interrupt. Also, the negative transition on P33 always latches the current T2 value into the capture register. There is no need for a control bit to enable/disable the latching; the capture register is read only.

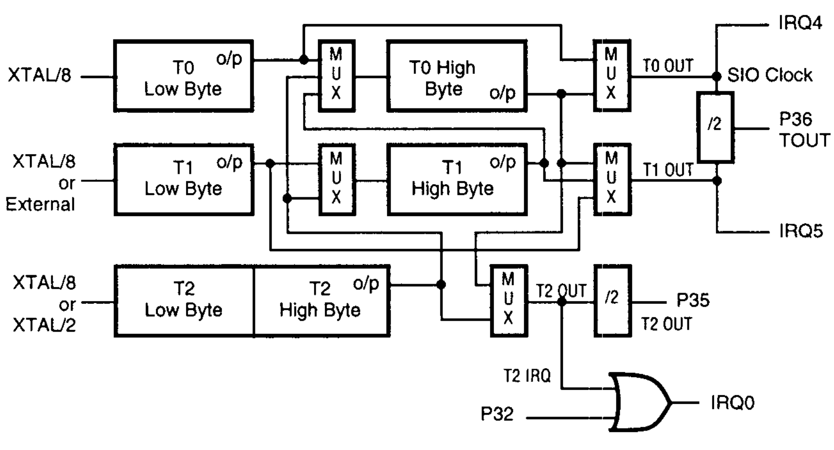


Figure 18. Counter/Timer Block Diagram

Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	C

* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

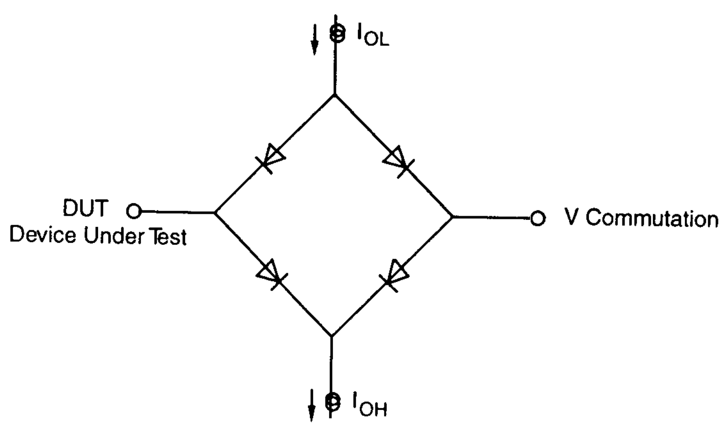


Figure 23. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS
V_{CC} = 3.3V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	0.8 V_{CC}	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.1xV_{CC}		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7xV_{CC}	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.1xV_{CC}		V	
V_{OH}	Output High Voltge	1.8			V	I_{OH} = -1.0 mA
V_{OH}	Output High Voltge	V_{CC} - 100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +1.0 mA
V_{RH}	Reset Input High Voltage	0.8xV_{CC}	V_{CC}		V	
V_{Rl}	Reset Input Low Voltage	-0.03	0.1xV_{CC}		V	
I_{IL}	Input Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		µA	V_{RL} = 0V
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Stand By Current (HALT Mode)		12	8	mA	HALT Mode V_{IN}=0V, V_{CC} @ 25 MHz [1]
I_{CC2}	Stand By Current (HALT Mode)		8	1	µA	STOP Mode V_{IN}=0V, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	-10	10	5	µA	

Note:
[1] All inputs driven to 0V, V_{CC} and outputs floating.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltge	2.4			V	I_{OH}=-2.0 mA
V_{OH}	Output High Voltage	V_{CC} -100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +5 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.8		V	
I_{IL}	Input Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		µA	V_{RL} = 0V
I_{CC}	Supply Current		55	35	mA	@ 33 MHz [1]
			40	25	mA	@ 25 MHz [1]
			30	20	mA	@ 20 MHz [1]
I_{CC1}	Standby Current (HALT Mode)		15	9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 25 MHz [1]
			20	15		HALT Mode V_{IN} = 0V, V_{CC} @ 33 MHz [1]
			12	7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 20 MHz [1]
I_{CC2}	Standby Current (STOP Mode)		10	1	µA	STOP Mode V_{IN} = 0V, V_{CC} [1]
I_{AL}	Auto Latch Current	-16	16	5	µA	

Note:
[1] All inputs driven to 0V, or V_{cc} and outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

No	Sym	Parameter	T_A = 0°C to +70°C 33 MHz Min	33 MHz Max	25 MHz Min	25 MHz Max	20 MHz Min	20 MHz Max	Typical V_{CC}=5.0V @ 25°C	Units
1	TdA(AS)	Address Valid To /AS Rise Delay	13		22		26			ns
2	TdAS(A)	/AS Rise To Address Hold Time	20		25		28			ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		90		130		160		ns
4	TwAS	/AS Low Width	20		28		36			ns
5	TdAZ(DSR)	Address Float To /DS (Read)	0		0		0			ns
6	TwDSR	/DS (Read) Low Width	65		100		130			ns
7	TwDSW	/DS (Write) Low Width	40		65		75			ns
8	TdDSR(DI)	/DS (Read) To Data in Req'd Valid Delay		30		78		100		ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0			ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		34		40			ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36			ns
12	TdR/W(AS)	R/W To /AS Rise Delay	12		26		32			ns
13	TdDS(R/W)	/DS Rise To R/W Valid Delay	12		30		36			ns
14	TdDO(DSW)	Data Out To /DS (Write) Delay	12		34		40			ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40			ns
16	TdA(DI)	Address To Data In Req'd Valid Delay		110		160		200		ns
17	TdAS(DSR)	/AS Rise To /DS (Read) Delay	20		40		48			ns
18	TaDI(DSR)	Data In Set-up Time To /DS Rise Read	16		30		36			ns
19	TdDM(AS)	/DM To /AS Rise Delay	10		22		26			ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay							34*	ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time							34*	ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising							20*	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling							23*	ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling							29*	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising							29*	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling							29*	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising							29*	ns
28	TsW(XT)	Wait Set-up Time							10*	ns
29	ThW(XT)	Wait Hold Time							15*	ns
30	TwW	Wait Width (One Wait Time)							25*	ns

Notes:
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
* Preliminary value to be characterized.

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

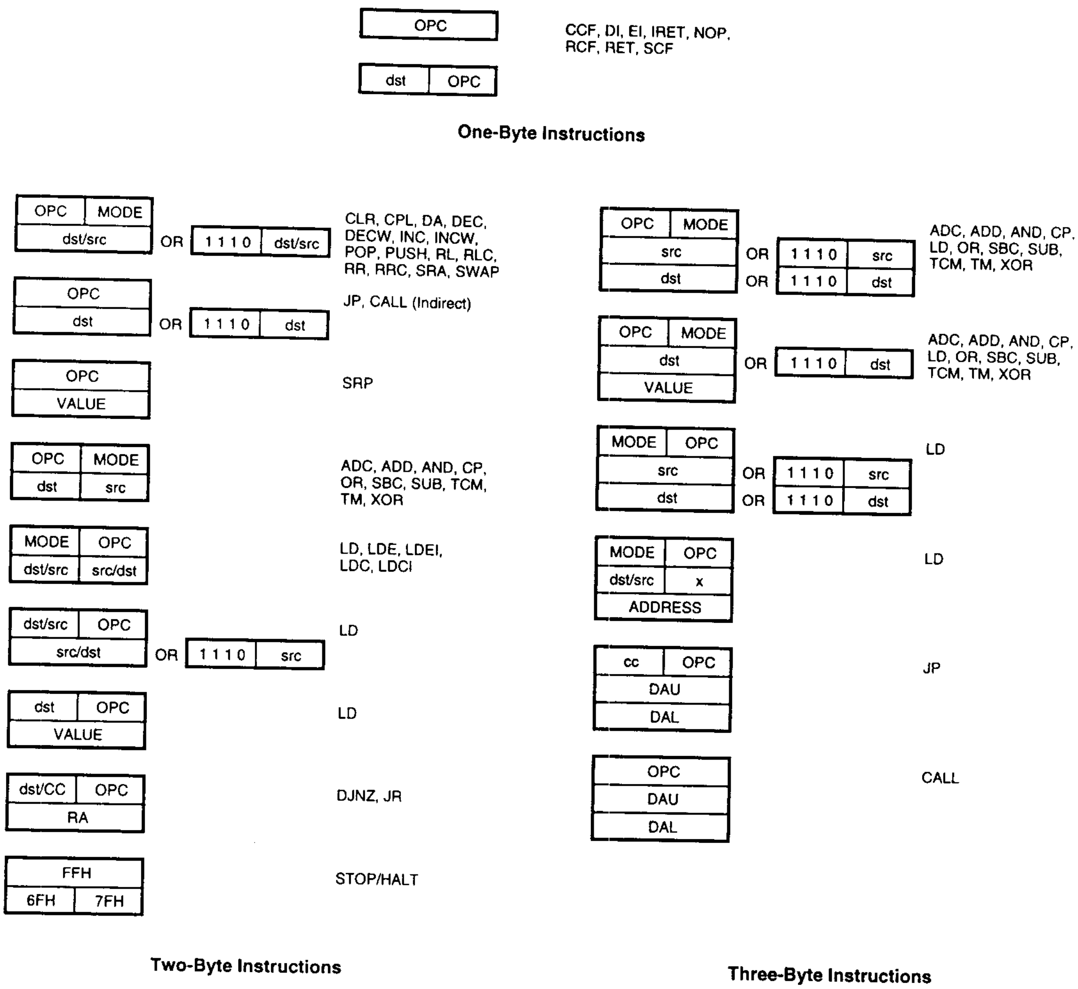
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

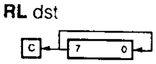
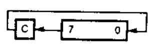
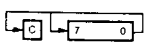
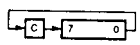
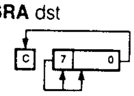
dst ← dst + src

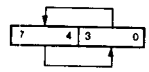
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP - 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP src RP←src	Im	31	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
STOP		6F	- - - - - -
SUB dst, src dst←dst←src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]