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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9325fsc00tr



Z86C93

CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.
- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.
- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.
- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.
- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Two 16-bit counter timers with 6-bit prescalers.
- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.
- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.
- Additional emulation signals SCLK, IACK, and /SYNC are made available.
- Two low power standby modes, STOP and HALT
- Full-duplex UART
- $3.3 \pm 10\%$ volt operation at 25 MHz
- $5.0 \pm 10\%$ volt operation at 20, 25 and 33 MHz

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

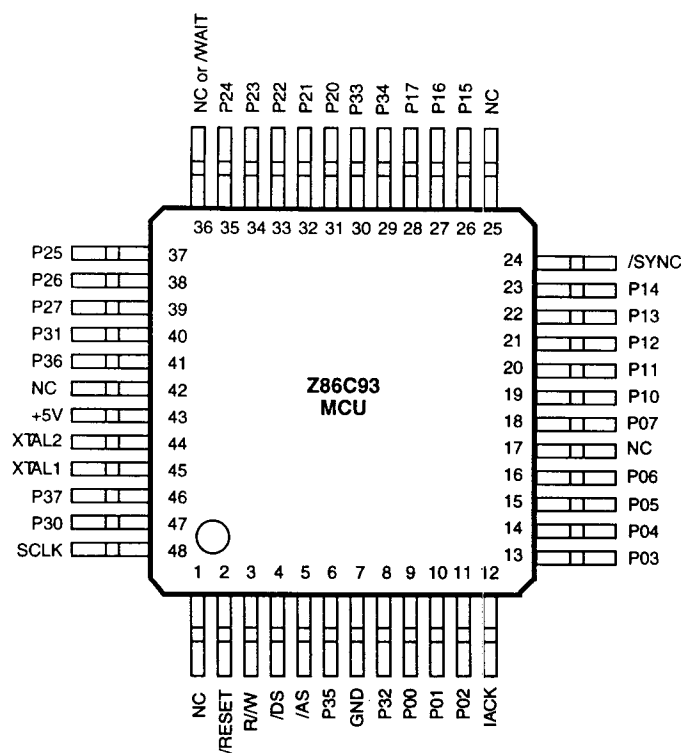


Figure 6. 48-Pin VQFP Package

Table 4. 48-Pin VQFP Pin Identification

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	N/C	Not Connected	Input	25	N/C	Not Connected	Input
2	/RESET	Reset	Input	26-28	P15-P17	Port 1 pin 5,6,7	In/Output
3	R/W	Read/Write	Output	29	F34	Port 3 pin 4	Output
4	/DS	Data Strobe	Output	30	F33	Port 3 pin 33	Input
5	/AS	Address Strobe	Output	31-35	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
6	P35	Port 3 pin 5	Input	36	N/C	Not Connected (20 MHz)	Input
7	GND	Ground GND	Input		/WAIT	WAIT (25 or 33 MHz)	Input
8	P32	Port 3 pin 2	Input	37-39	P25-P27	Port 2 pin 5,6,7	In/Output
9-11	P00-P02	Port 0 pin 3,4,5,6	In/Output	40	F31	Port 3 pin 1	Input
12	IACK	Int. Acknowledge	Output	41	P36	Port 3 pin 6	Output
13-16	P03-P06	Port 0 pin 3,4,5,6	In/Output	42	N/C	Not Connected	Input
17	N/C	Not Connected	Input	43	V _{cc}	Power Supply	Input
18	P07	Port 0 pin 7	In/Output	44	XTAL2	Crystal, Osc. Clock	Output
19-23	P10-P14	Port 1 pin 0,1,2,3,4	In/Output	45	XTAL1	Crystal, Osc. Clock	Input
24	/SYNC	Synchronize Pin	Output	46	P37	Port 3 pin 7	Output
				47	P30	Port 3 pin 0	Input
				48	SCLK	System Clock	Output

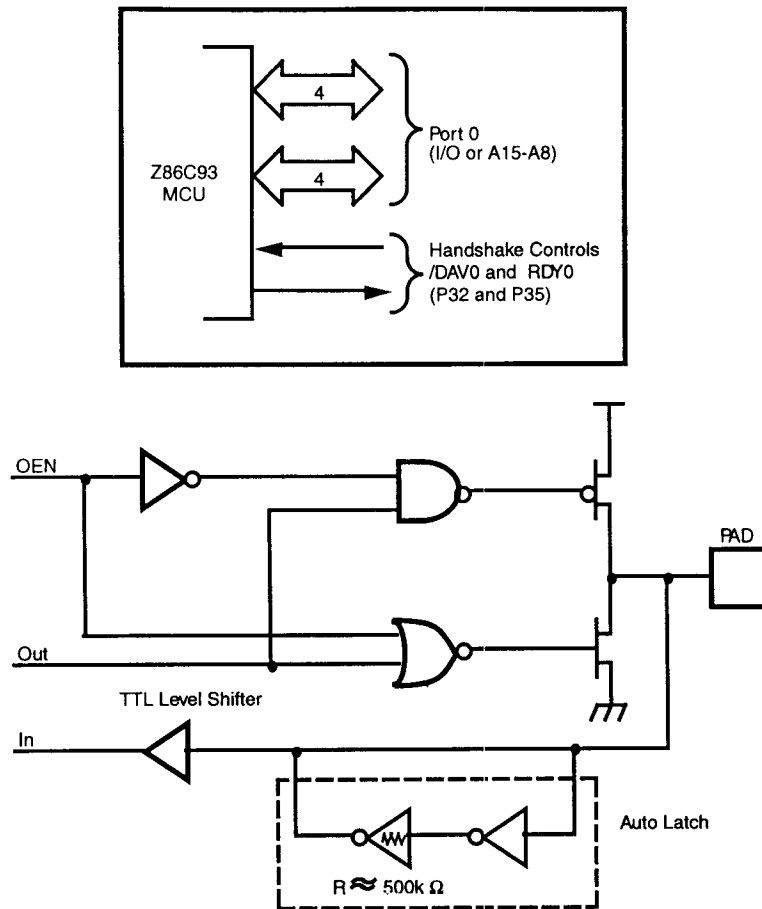


Figure 7. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1. (P10-P17). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory (Figure 8).

If more than 256 external locations are required, Port 0 must output the additional lines.

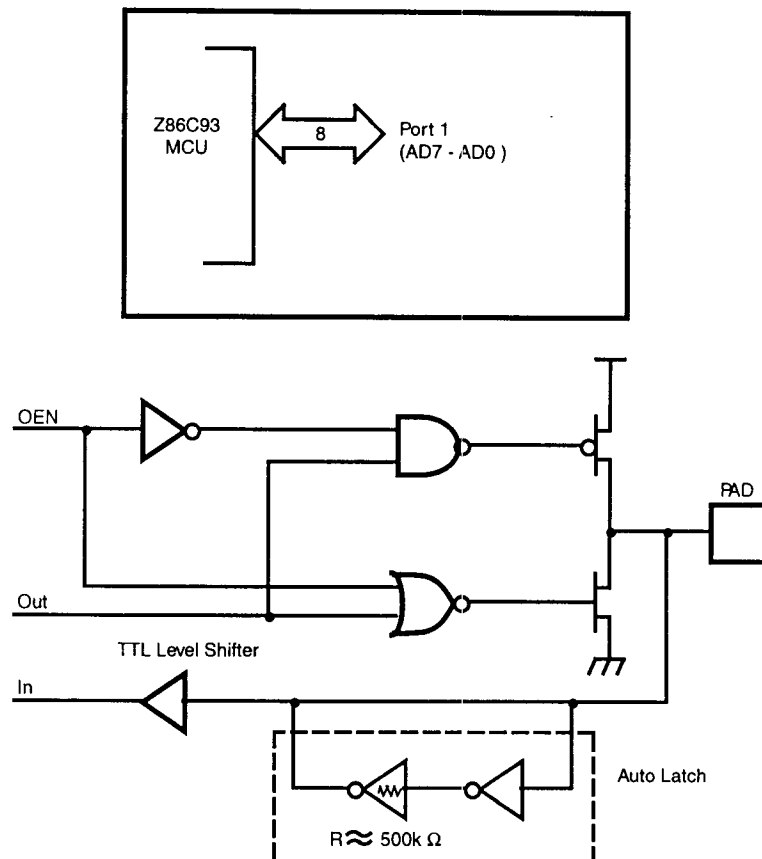


Figure 8. Port 1 Configuration

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal

assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

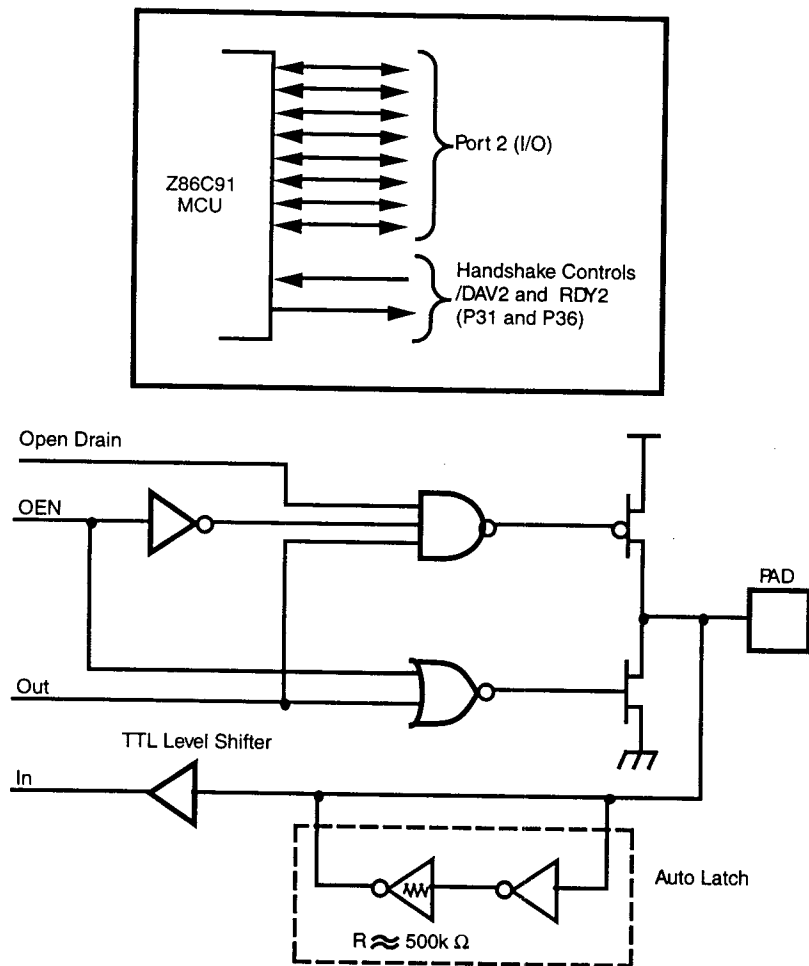


Figure 9. Port 2 Configuration

PIN FUNCTIONS (Continued)

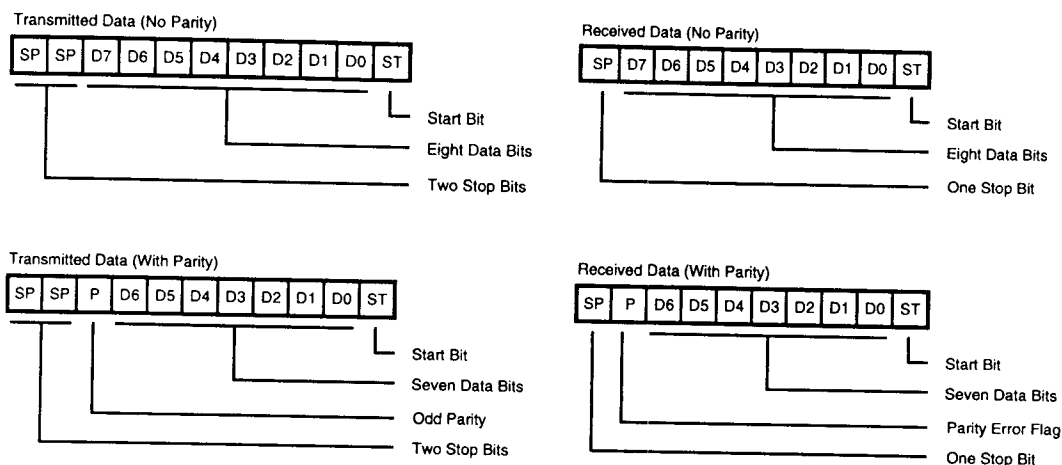


Figure 11. Serial Data Formats

ADDRESS SPACE

Program Memory. The Z86C93 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory. The Z96C93 can address up to 64 Kbytes of external data memory. External data memory is included with, or separated from, the external program memory

space. /DM, an optional I/O function that can be programmed to appear on pin P34 is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

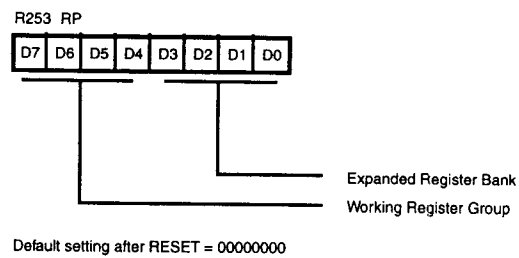


Figure 14. Register Pointer Register

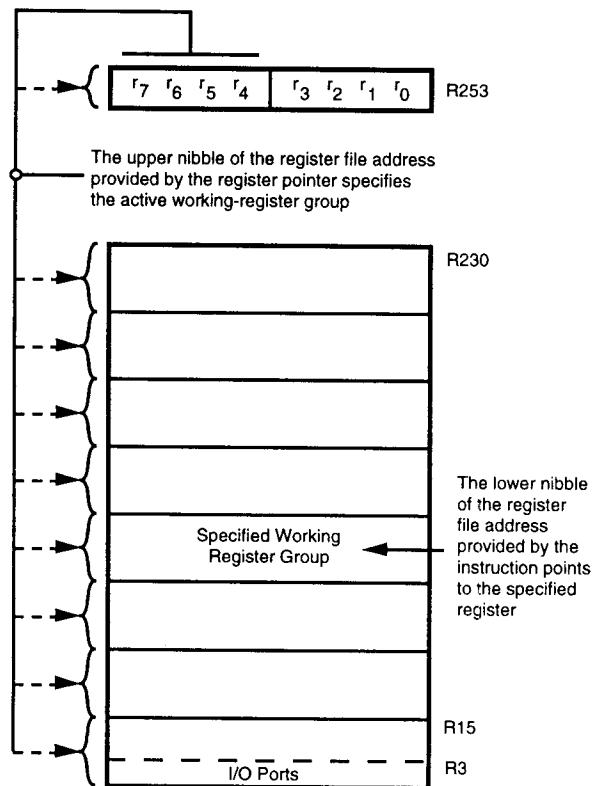


Figure 15. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

DIVZR. Division by Zero (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined
x = Irrelevant
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

Performance of multiplication. The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7 μ s. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 μ s. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

Performance of division. The actual division needs 20 internal clock cycles. This translates to 2.0 μ s for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 μ s at 10 MHz.

Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

FUNCTIONAL DESCRIPTION (Continued)

Operation

Except for the programmable down counter length and clock input, T2 is identical to T0.

T0 and T1 retain all their features except that now they are extendable interims of the down-counter length.

The output of T2, under program control, goes to an output pin (P35). Also, the interrupt generated by T2 is ORed with the interrupt request generated by P32. Note that the service routine then has to poll the T2 flag bit and also clear it (Bit 7 of T2 Timer Mode Register).

On power up, T0 and T1 are configured in the 8-bit down counter length mode (to be compatible with Z86C91) and T2 is in the 32-bit mode with its output disabled (no interrupt is generated and T2 output DOES NOT go to port pin P35).

The UART uses T0 for generating the bit clock. This means, while using UART, T0 should be in 8-bit mode. So, while using the UART there are only two independent timer/counters.

The counters are configured in the following manner:

Timer	Mode	Byte
T0	8-bit	Low Byte (T0)
T0	16-bit	High Byte (T0) + Low Byte (T0)
T1	8-bit	Low Byte (T1)
T1	16-bit	High Byte (T1) + Low Byte (T1)
T1	24-bit	High Byte (T0) + High Byte (T1) + Low Byte (T1)
T2	16-bit	High Byte (T2) + Low Byte (T2)
T2	24-bit	High Byte (T0) + High Byte (T2) + Low Byte (T2)
T2	32-bit	High Byte (T0) + High Byte (T1) + High Byte (T2) + Low Byte (T2)

Note that the T2 interrupt is logically ORed with P32 to generate IRQ0.

The T2 Timer Mode register is shown in Figure 19. Upon reaching end of count, bit 7 of this register is set to one. This bit IS NOT reset in hardware and it has to be cleared by the interrupt service routine.

T2 interrogates the state of the Count Mode Bit (D2) once it has counted down to its zero value. T2 then makes the decision to continue counting (Module N Mode) or stop (Single Pass Mode). Observe this functionality if attempting to modify the count mode prior to the end of count bit (D7) being set.

The register map of the new CTC registers is shown in Figure 13. T0 high byte and T1 high byte are at the same relative locations as their respective low bytes, but in a different register bank.

The T2 prescaler register is shown in Figure 19. Bits 1 and 0 of this register control the various cascade modes of the counters.

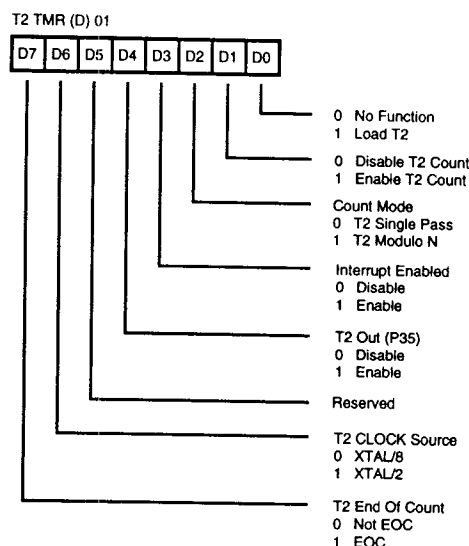


Figure 19. T2 Timer Mode Register (T2)

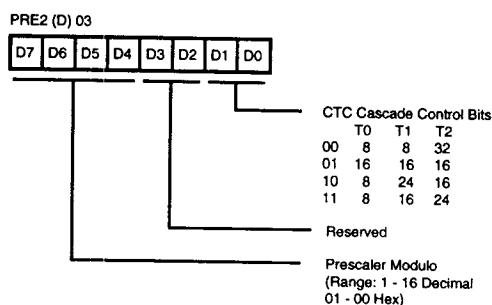


Figure 20. T2 Prescaler Register (PRE2)

Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

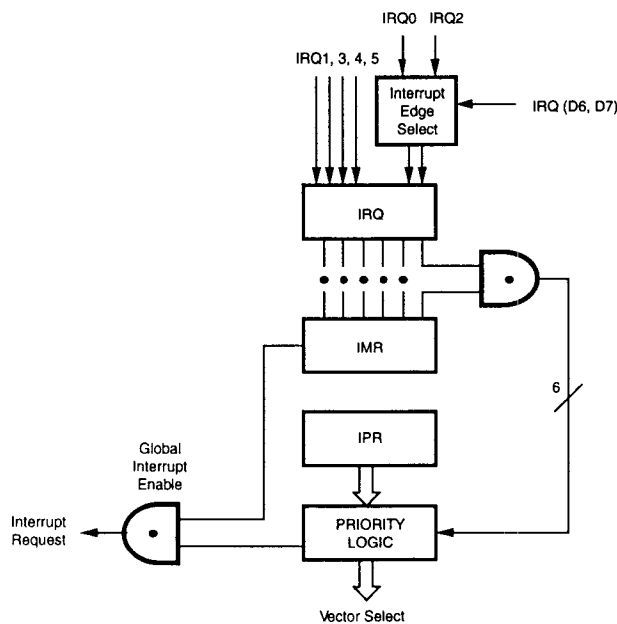


Figure 21. Interrupt Block Diagram

Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μ A or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF NOP ; clear the pipeline
6F STOP ; enter STOP mode
or
FF NOP ; clear the pipeline
7F HALT ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	C

* Voltages on all pins with respect to GND.

† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

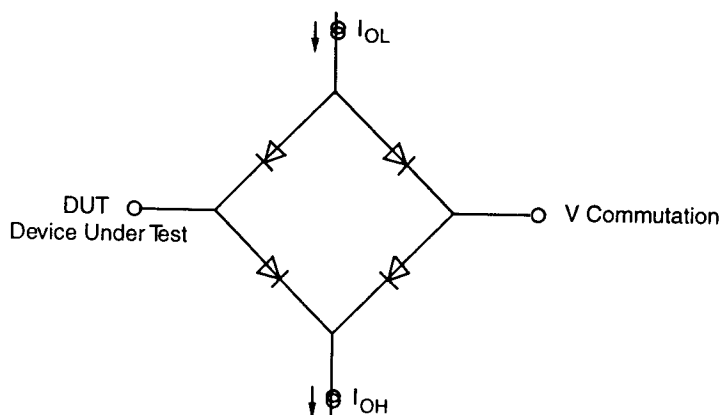


Figure 23. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

$$V_{CC} = 3.3V \pm 10\%$$

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} = 250 \mu\text{A}$
V_{CH}	Clock Input High Voltage	$0.8 V_{CC}$	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	$0.1 \times V_{CC}$		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	$0.7 \times V_{CC}$	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	$0.1 \times V_{CC}$		V	
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -1.0 \text{ mA}$
V_{OHI}	Output High Voltage	$V_{CC} - 100\text{mV}$			V	$I_{OH} = -100 \mu\text{A}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +1.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	$0.8 \times V_{CC}$	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	-0.03	$0.1 \times V_{CC}$		V	
I_{IL}	Input Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		μA	$V_{RL} = 0\text{V}$
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Stand By Current (HALT Mode)		12	8	mA	HALT Mode $V_{IN} = 0\text{V}$, V_{CC} @ 25 MHz [1]
I_{CC2}	Stand By Current (HALT Mode)		8	1	μA	STOP Mode $V_{IN} = 0\text{V}$, V_{CC} [1]
I_{AL}	Auto Latch Low Current	-10	10	5	μA	

Note:

[1] All inputs driven to 0V, V_{CC} and outputs floating.

AC CHARACTERISTICS

Additional Timing Diagram

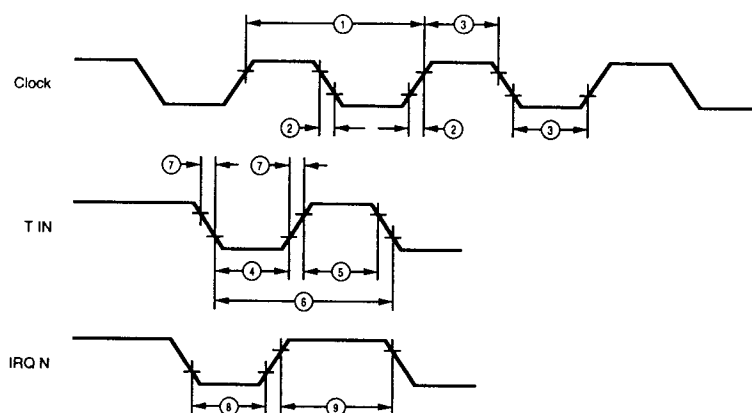


Figure 27. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

No	Symbol	Parameter	T _A = 0°C to +70° C						Units	Notes
			33 MHz		24 MHz		20 MHz			
			Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	30	1000	42	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		5		10		10	ns	[1]
3	TwC	Input Clock Width	10		11		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC			[2,3]

Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request via Port 3.
- [4] Interrupt request via Port 3 (P31-P33).
- [5] Interrupt request via Port 30.

AC CHARACTERISTICS Handshake Timing Table

No	Symbol	Parameter	T _A = 0°C to +70°C		Units	Data Direction
			Min	Max		
1	TsDI(DAV)	Data In Setup Time to /DAV	0		ns	In
2	ThDI(DAV)	RDY to Data In Hold Time	0		ns	In
3	TwDAV	/DAV Width	40		ns	In
4	TdDAVIf(RDYf)	/DAV to RDY Delay		70	ns	In
5	TdDAVIf(RDYr)	DAV Rise to RDY Wait Time		40	ns	In
6	TdRDYOr(DAVIf)	RDY Rise to DAV Delay	0		ns	In
7	TdDO(DAV)	Data Out to DAV Delay		TpC	ns	Out
8	TdDAVOf(RDYIf)	/DAV to RDY Delay	0		ns	Out
9	TdRDYIf(DAVOr)	RDY to /DAV Rise Delay		70	ns	Out
10	TwRDY	RDY Width	40		ns	Out
11	TdRDYIf(DAVOf)	RDY Rise to DAV Wait Time		40	ns	Out

Z8 CONTROL REGISTERS

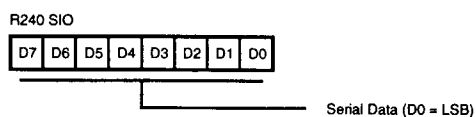


Figure 37. Serial I/O Register
(F0H: Read/Write)

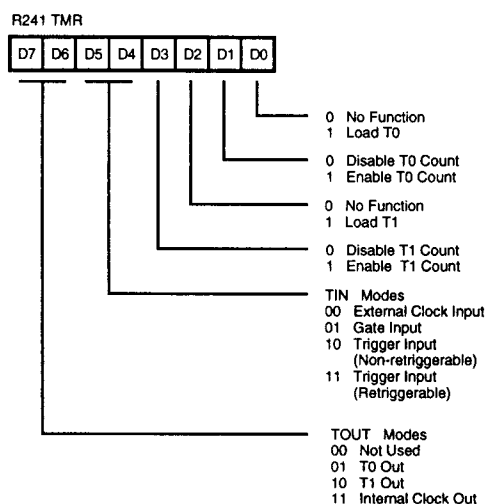


Figure 38. Timer Mode Register
(F1H: Read/Write)

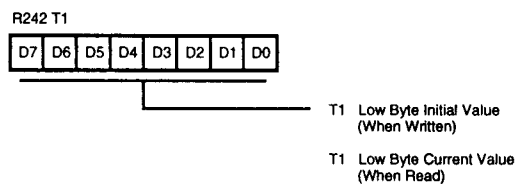


Figure 39. Counter/Timer 1 Register
(F2H: Read/Write)

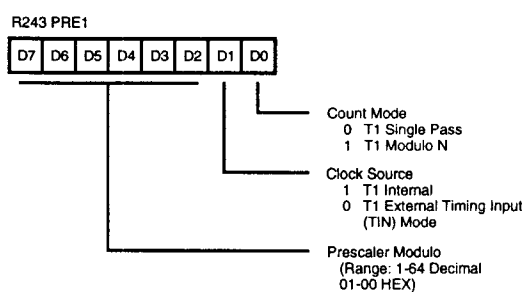


Figure 40. Prescaler 1 Register
(F3H: Write Only)

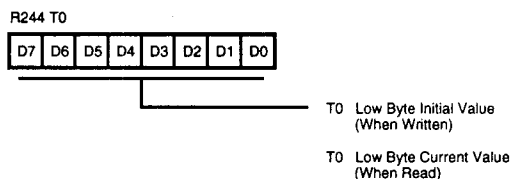


Figure 41. Counter/Timer 0 Register
(F4H: Read/Write)

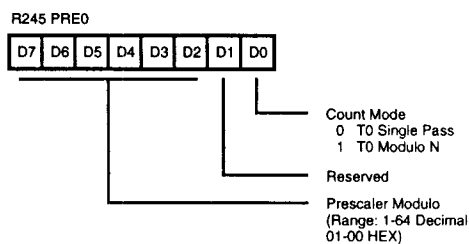


Figure 42. Prescaler 0 Register
(F5H: Write Only)

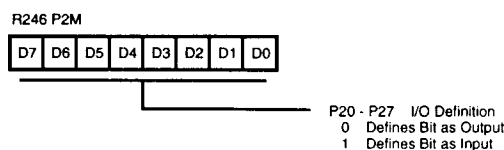


Figure 43. Port 2 Mode Register
(F6H: Write Only)

Z8 CONTROL REGISTERS (Continued)

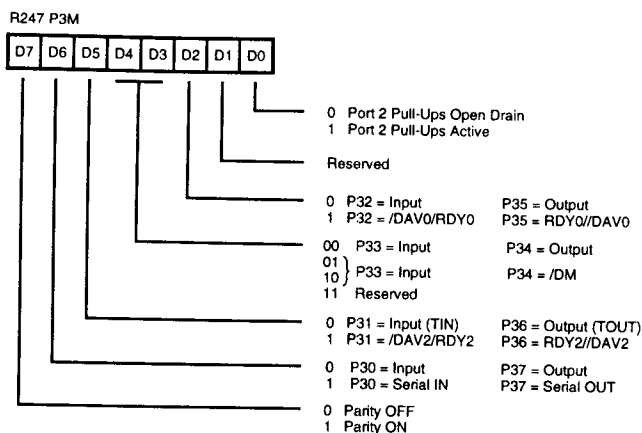


Figure 44. Port 3 Mode Register
(F7H: Write Only)

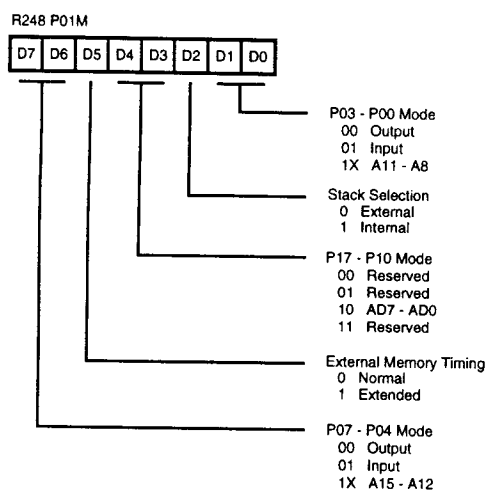


Figure 45. Ports 0 and 1 Mode Registers
(F8H: Write Only)

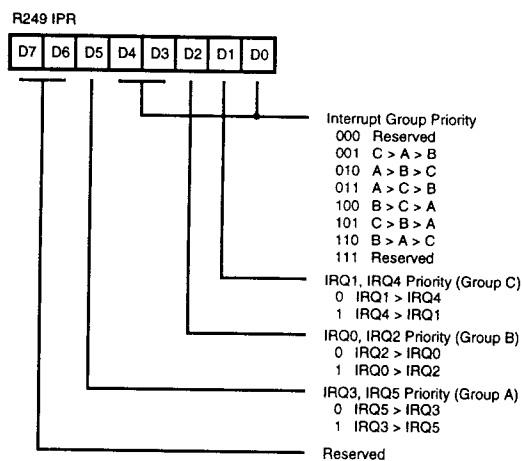


Figure 46. Interrupt Priority Register
(F9H: Write Only)

CONDITION CODES

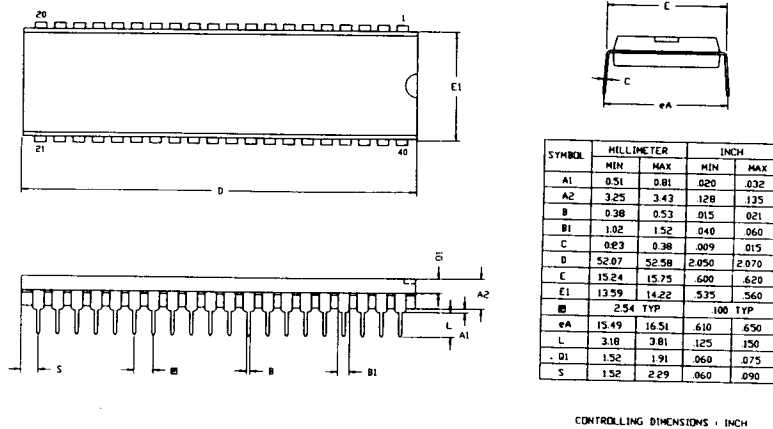
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION SUMMARY (Continued)

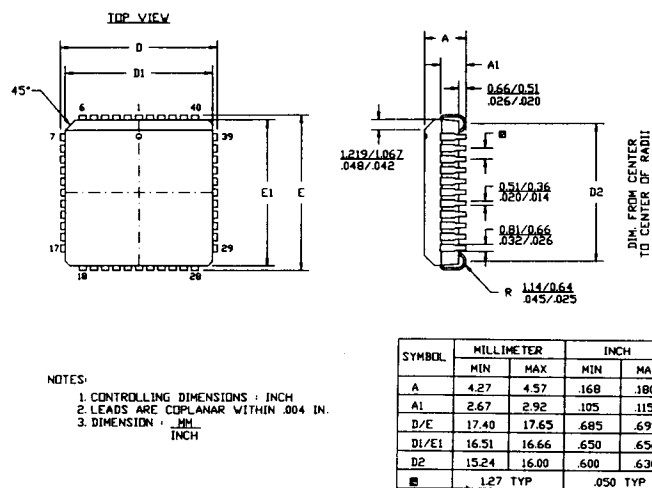
Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
ADC dst, src dst ← dst + src + C	†	1[]	*	*	*	*	0	*	
ADD dst, src dst ← dst + src	†	0[]	*	*	*	*	0	*	
AND dst, src dst ← dst AND src	†	5[]	-	*	*	0	-	-	
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR	D6 D4	-	-	-	-	-	-	
CCF C ← NOT C		EF	*	-	-	-	-	-	
CLR dst dst ← 0	R IR	B0 B1	-	-	-	-	-	-	
COM dst dst ← NOT dst	R IR	60 61	-	*	*	0	-	-	
CP dst, src dst - src	†	A[]	*	*	*	*	-	-	
DA dst dst ← DA dst	R IR	40 41	*	*	*	X	-	-	
DEC dst dst ← dst - 1	R IR	00 01	-	*	*	*	-	-	
DECW dst dst ← dst - 1	RR IR	80 81	-	*	*	*	-	-	
DI IMR(7) ← 0		8F	-	-	-	-	-	-	
DJNZ r, dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA	rA r = 0 - F	-	-	-	-	-	-	
EI IMR(7) ← 1		9F	-	-	-	-	-	-	
HALT		7F	-	-	-	-	-	-	

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
INC dst dst ← dst + 1	r R IR	rE r = 0 - F 20 21	-	*	*	*	-	-	
INCW dst dst ← dst + 1	RR IR	A0 A1	-	*	*	*	-	-	
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1		BF	*	*	*	*	*	*	
JP cc, dst if cc is true PC ← dst	DA IRR	cD c = 0 - F 30	-	-	-	-	-	-	
JR cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA	cB c = 0 - F	-	-	-	-	-	-	
LD dst, src dst ← src	r r R r r X r r R R R IR IR R	lm rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	
LDC dst, src	r lrr	C2	-	-	-	-	-	-	
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	lr lrr	C3	-	-	-	-	-	-	

PACKAGE INFORMATION



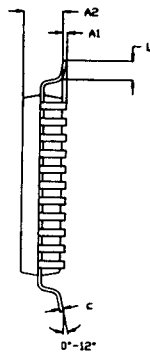
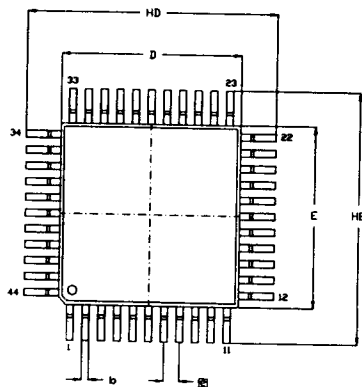
40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram

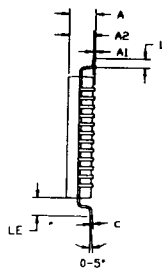
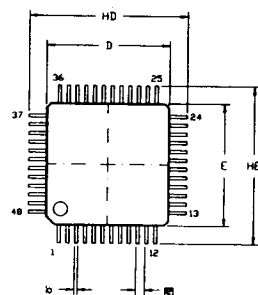
PACKAGE INFORMATION (Continued)

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10mm
.004"



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.05	2.25	.081	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
□	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.18	.004	.007
HD	8.60	9.40	.339	.370
D	6.90	7.10	.272	.280
HE	8.60	9.40	.339	.370
E	6.90	7.10	.272	.280
□	0.50 TYP		.020 TYP	
L	0.30	0.70	.012	.028
LE	0.90	1.10	.035	.043

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm
.004"

48-Pin VQFP Package Diagram