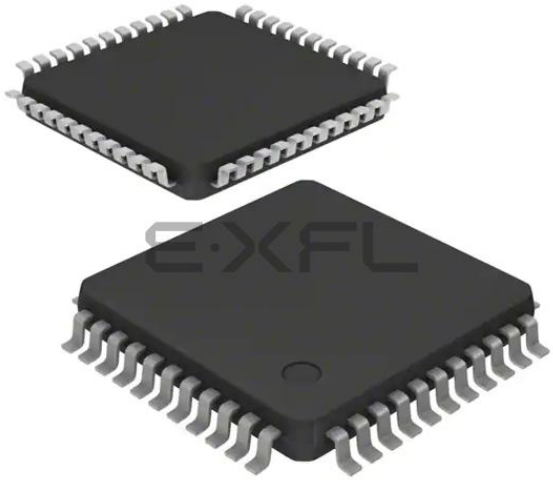

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | EBI/EMI, UART/USART |
| Peripherals | - |
| Number of I/O | 24 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 236 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86c9325fsg |

ZiLOG

*PRODUCT SPECIFICATION*

# Z86C93

## CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

### FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.
- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.
- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.
- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.
- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Two 16-bit counter timers with 6-bit prescalers.
- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.
- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.
- Additional emulation signals SCLK, IACK, and /SYNC are made available.
- Two low power standby modes, STOP and HALT
- Full-duplex UART
- 3.3 ± 10% volt operation at 25 MHz
- 5.0 ± 10% volt operation at 20, 25 and 33 MHz

### GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

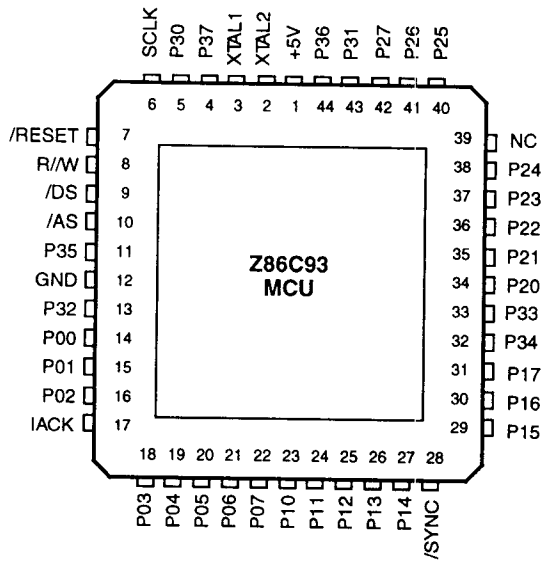



**Figure 4. 44-Pin PLCC**

**Table 2. 44-Pin PLCC Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | Input |
| 2 | XTAL2 | Crystal, Osc. Clock | Output |
| 3 | XTAL1 | Crystal, Osc. Clock | Input |
| 4 | P37 | Port 3 pin 7 | Output |
| 5 | P30 | Port 3 pin 0 | Input |
| 6 | SCLK | System Clock | Output |
| 7 | /RESET | Reset | Input |
| 8 | R/W | Read/Write | Output |
| 9 | /DS | Data Strobe | Output |
| 10 | /AS | Address Strobe | Output |
| 11 | P35 | Port 3 pin 5 | Output |
| 12 | GND | Ground GND | Input |
| 13 | P32 | Port 3 pin 2 | Input |

| No | Symbol | Function | Direction |
|---|---|---|---|
| 14-16 | P00-P02 | Port 0 pin 0,1,2 | In/Output |
| 17 | IACK | Int. Acknowledge | Output |
| 18-22 | P03-P07 | Port 0 pin 3,4,5,6,7 | In/Output |
| 23-27 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output |
| 28 | /SYNC | Synchronize Pin | Output |
| 29-31 | P15-P17 | Port 1 pin 5,6,7 | In/Output |
| 32 | P34 | Port 3 pin 4 | Output |
| 33 | P33 | Port 3 pin 3 | Input |
| 34-38 | P20-P24 | Port 2 pin 0,1,2,3,4 | In/Output |
| 39 | N/C | Not Connected (20 MHz) | Input |
| | /WAIT | WAIT (25 or 33 MHz) | Input |
| 40-42 | P25-P27 | Port 2 pin 5,6,7 | In/Output |
| 43 | P31 | Port 3 pin 1 | Input |
| 44 | P36 | Port 3 pin 6 | Output |

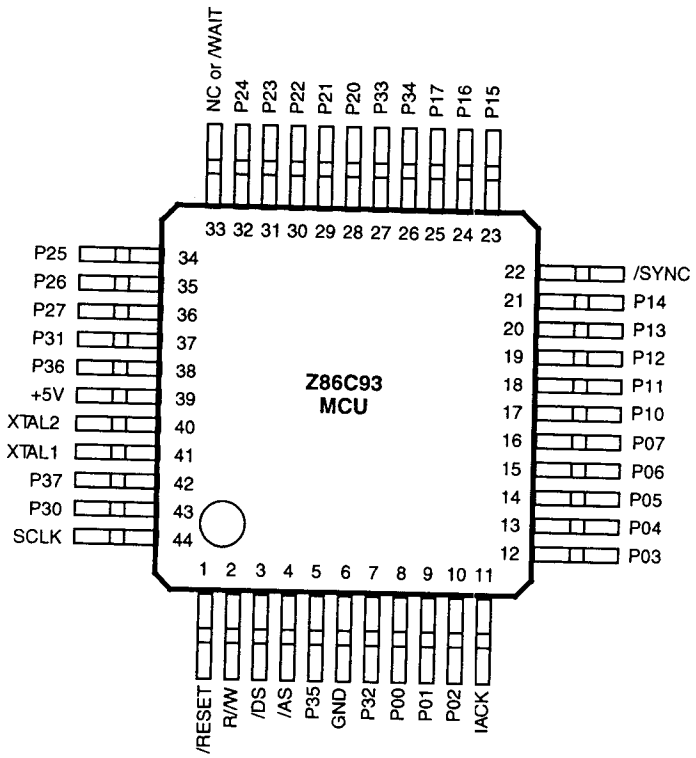



**Figure 5. 44-Pin QFP**

**Table 3. 44-Pin QFP Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | /RESET | Reset | Input |
| 2 | R/W | Read/Write | Output |
| 3 | /DS | Data Strobe | Output |
| 4 | /AS | Address Strobe | Output |
| 5 | P35 | Port 3 pin 5 | Input |
| 6 | GND | Ground GND | Input |
| 7 | P32 | Port 3 pin 2 | Input |
| 8-10 | P00-P02 | Port 0 pin 0,1,2 | In/Output |
| 11 | IACK | Int. Acknowledge | Output |
| 12-16 | P03-P07 | Port 0 pin 3,4,5,6,7 | In/Output |
| 17-21 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output |
| 22 | /SYNC | Synchronize Pin | Output |
| 23-25 | P15-P17 | Port 1 pin 5,6,7 | In/Output |
| 26 | P34 | Port 3 pin 4 | Output |
| 27 | P33 | Port 3 pin 3 | Input |
| 28-32 | P20-P24 | Port 2 pin 0,1,2,3,4 | In/Output |
| 33 | N/C | Not Connected (20 MHz) | Input |
| | /WAIT | WAIT (25 or 33 MHz) | Input |
| 34-36 | P25-P27 | Port 2 pin 5,6,7 | In/Output |
| 37 | P31 | Port 3 pin 1 | Input |
| 38 | P36 | Port 3 pin 6 | Output |
| 39 | $V_{CC}$ | Power Supply | Input |
| 40 | XTAL2 | Crystal, Osc. Clock | Output |
| 41 | XTAL1 | Crystal, Osc. Clock | Input |
| 42 | P37 | Port 3 pin 7 | Output |
| 43 | P30 | Port 3 pin 0 | Input |
| 44 | SCLK | System Clock | Output |

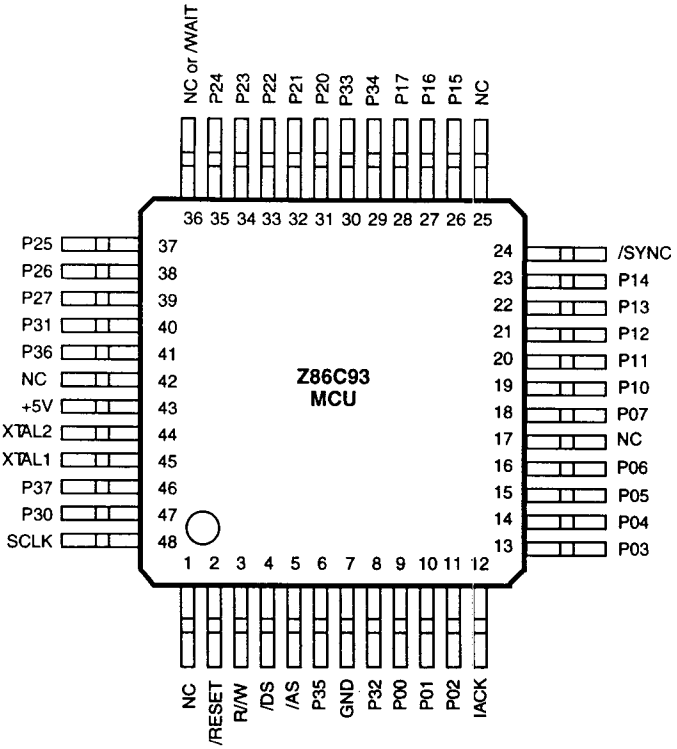



**Figure 6. 48-Pin VQFP Package**

**Table 4. 48-Pin VQFP Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1 | N/C | Not Connected | Input |
| 2 | /RESET | Reset | Input |
| 3 | R/W | Read/Write | Output |
| 4 | /DS | Data Strobe | Output |
| 5 | /AS | Address Strobe | Output |
| 6 | P35 | Port 3 pin 5 | Input |
| 7 | GND | Ground GND | Input |
| 8 | P32 | Port 3 pin 2 | Input |
| 9-11 | P00-P02 | Port 0 pin 3,4,5,6 | In/Output |
| 12 | IACK | Int. Acknowledge | Output |
| 13-16 | P03-P06 | Port 0 pin 3,4,5,6 | In/Output |
| 17 | N/C | Not Connected | Input |
| 18 | P07 | Port 0 pin 7 | In/Output |
| 19-23 | P10-P14 | Port 1 pin 0,1,2,3,4 | In/Output |
| 24 | /SYNC | Synchronize Pin | Output |

| No | Symbol | Function | Direction |
|---|---|---|---|
| 25 | N/C | Not Connected | Input |
| 26-28 | P15-P17 | Port 1 pin 5,6,7 | In/Output |
| 29 | P34 | Port 3 pin 4 | Output |
| 30 | P33 | Port 3 pin 33 | Input |
| 31-35 | P20-P24 | Port 2 pin 0,1,2,3,4 | In/Output |
| 36 | N/C | Not Connected (20 MHz) | Input |
| | /WAIT | WAIT (25 or 33 MHz) | Input |
| 37-39 | P25-P27 | Port 2 pin 5,6,7 | In/Output |
| 40 | P31 | Port 3 pin 1 | Input |
| 41 | P36 | Port 3 pin 6 | Output |
| 42 | N/C | Not Connected | Input |
| 43 | $V_{cc}$ | Power Supply | Input |
| 44 | XTAL2 | Crystal, Osc. Clock | Output |
| 45 | XTAL1 | Crystal, Osc. Clock | Input |
| 46 | P37 | Port 3 pin 7 | Output |
| 47 | P30 | Port 3 pin 0 | Input |
| 48 | SCLK | System Clock | Output |

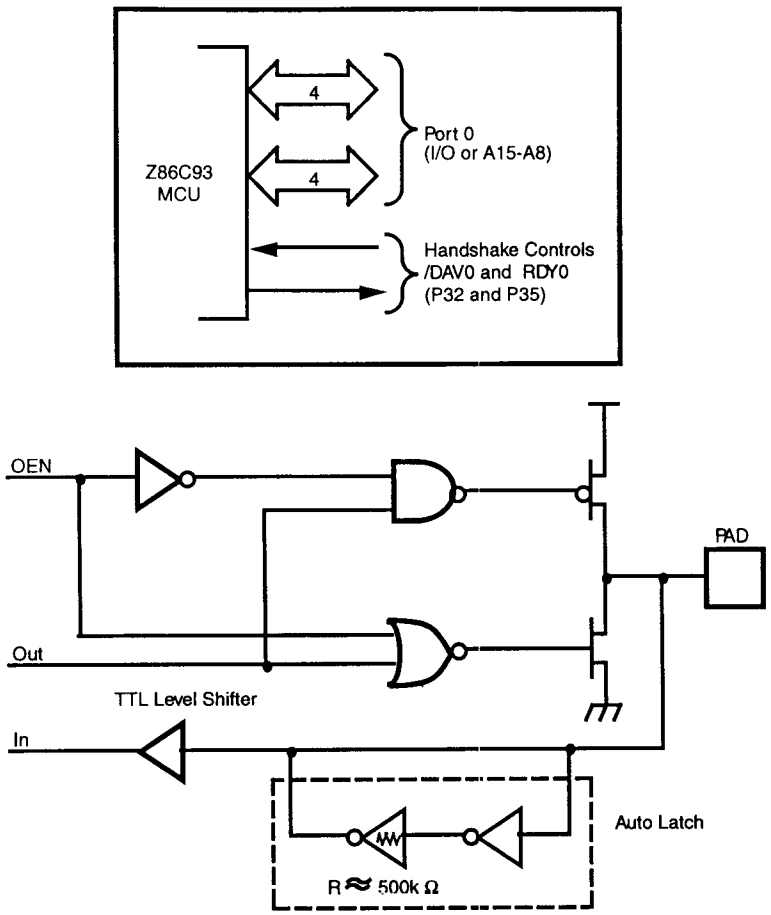



**Figure 7. Port 0 Configuration**

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

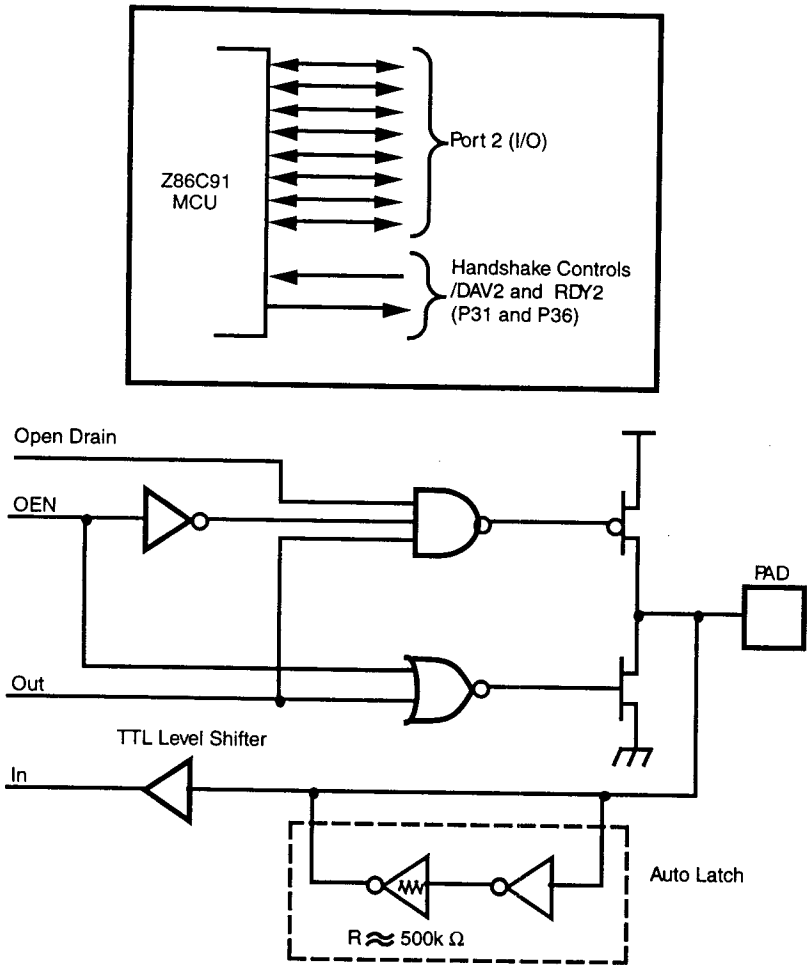



**Figure 9. Port 2 Configuration**

**Port 3 P30-P37.** Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

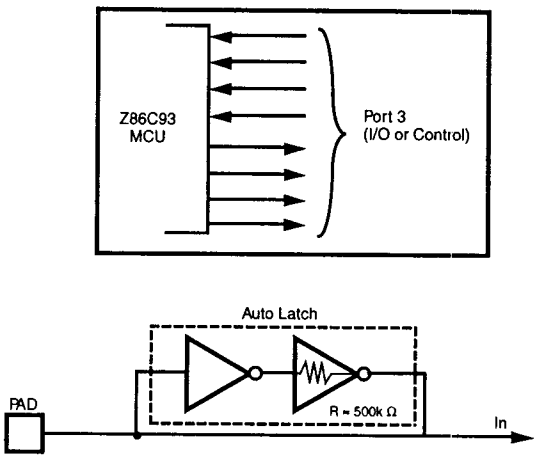



**Figure 10. Port 3 Configuration**

**Table 5. Port 3 Pin Assignments**

| Pin # | I/O | CTC1 | Int. | P0HS | P2HS | UART | Ext. |
|---|---|---|---|---|---|---|---|
| P30 | In | | IRQ3 | | | Serial In | |
| P31 | In | $T_{IN}$ | IRQ2 | | D/R | | |
| P32 | In | | IRQ0 | D/R | | | |
| P33 | In | | IRQ1 | | | | |
| P34 | Out | | | | | | DM |
| P35 | Out | | | R/D | | | |
| P36 | Out | $T_{OUT}$ | | | R/D | | |
| P37 | Out | | | | | Serial Out | |

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals ($T_{IN}$ and $T_{OUT}$), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

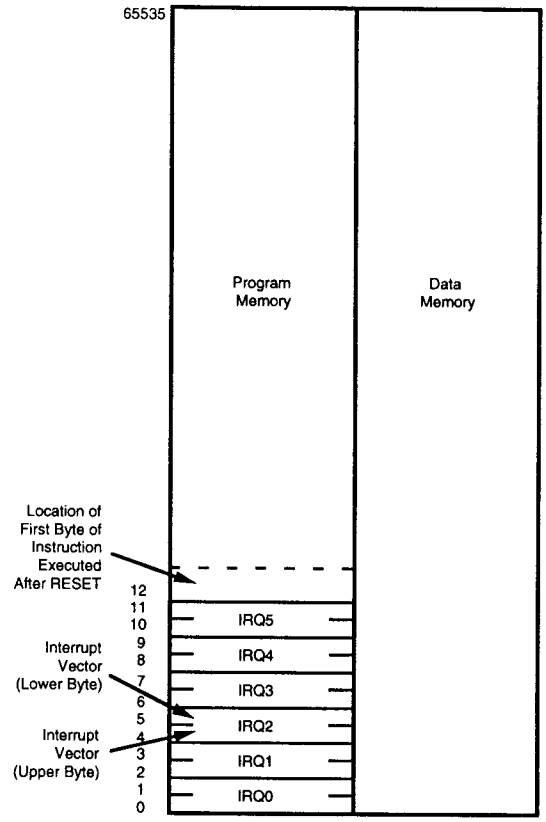



**Figure 12. Program and Data Memory Configuration**

**Expanded Register File.** The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area (Figure 13). The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14). The registers that are used in the multiply/divide unit reside in the Expanded Register File at Bank E and those for the additional timer control words reside in Bank D. The rest of the Expanded Register is not physically implemented and is open for future expansion.

**Register File.** The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers. The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C93 also allows short 4-bit register addressing using the Register Pointer (Figure 15). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

**Note:** Register Group E0-EF can only be accessed through working registers and indirect addressing modes.

**Stack.** The Z86C93 has a 16-bit Stack Pointer (R254-R255), used for external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH, Bits 8-15) can be used as a general-purpose register when using internal stack only.

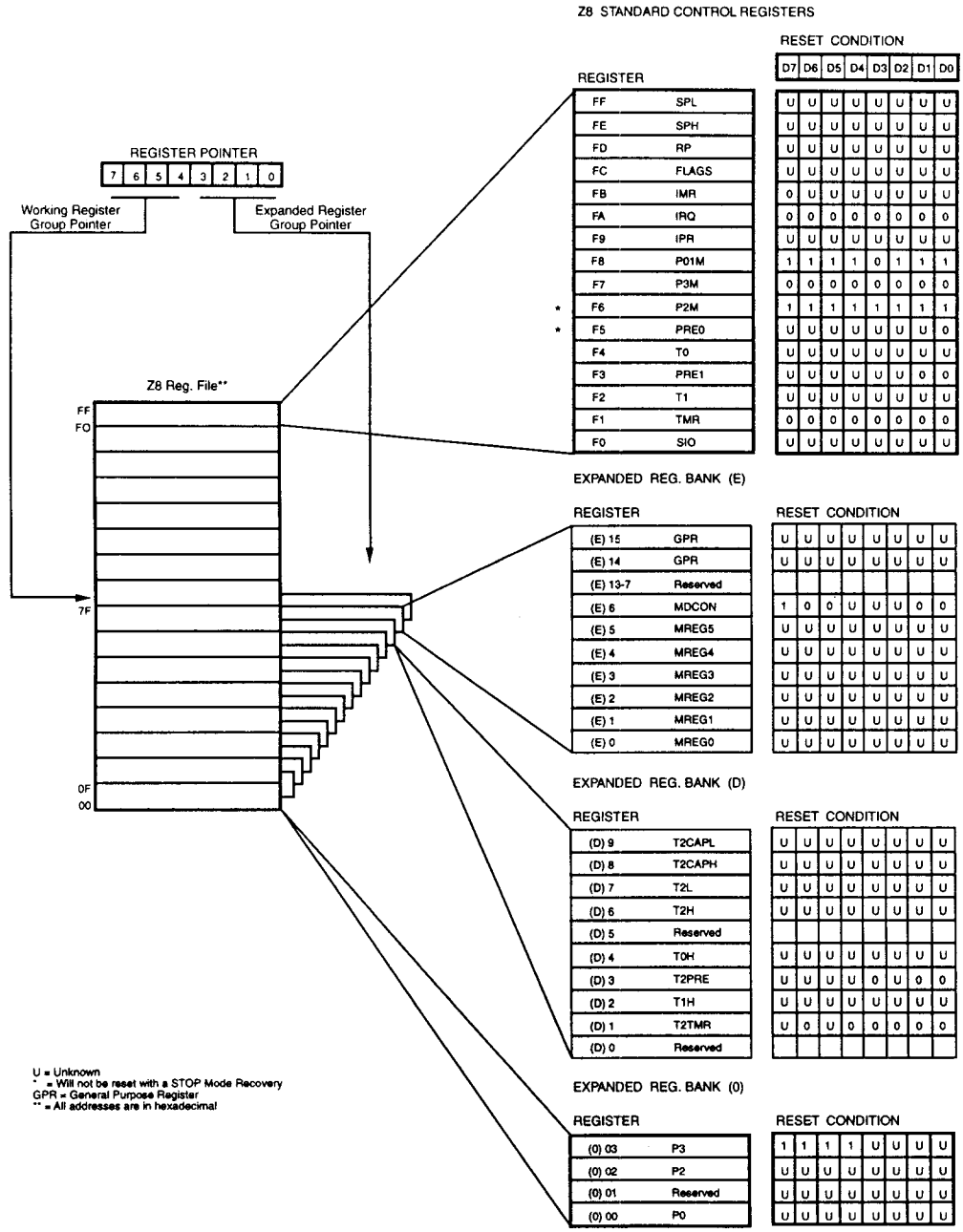



**Figure 13. Register File**

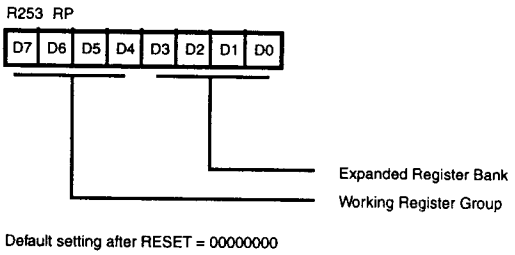



**Figure 14. Register Pointer Register**

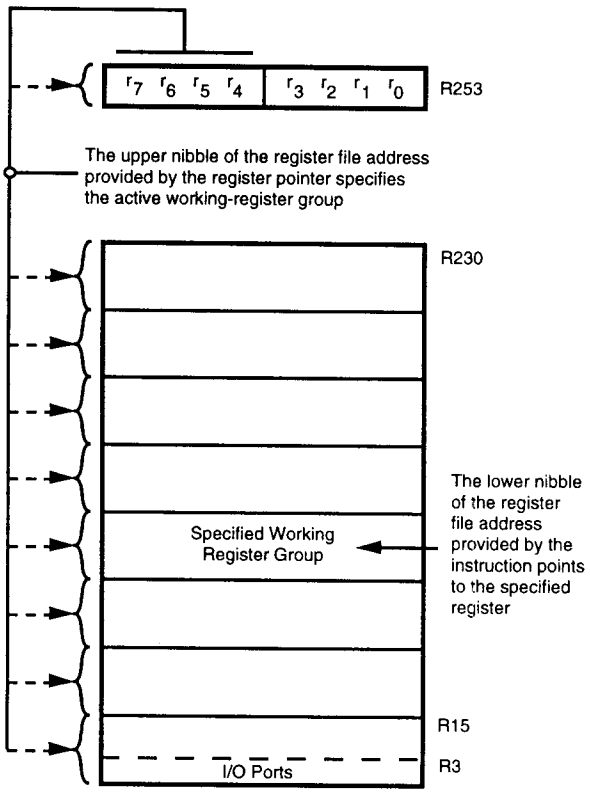



**Figure 15. Register Pointer**

DIVZR. *Division by Zero* (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined
x = Irrelevant
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

**Performance of multiplication.** The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7 µs. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 µs. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

**Performance of division.** The actual division needs 20 internal clock cycles. This translates to 2.0 µs for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 µs at 10 MHz.

## Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

## Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=OFFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
          or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage* | -0.3 | +7.0 | V |
| $T_{STG}$ | Storage Temp | -65 | +150 | C |
| $T_A$ | Oper Ambient Temp | † | † | C |

* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

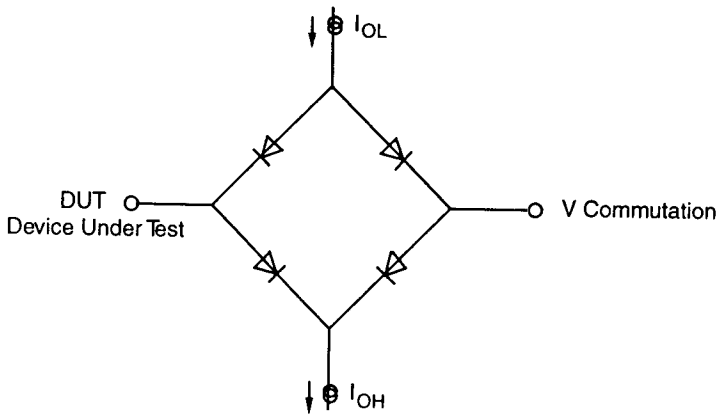



**Figure 23. Test Load Diagram**

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5.0V ± 10%

| Sym | Parameter | $T_A$ = 0°C to +70°C Min | Max | Typical at 25°C | Units | Conditions |
|---|---|---|---|---|---|---|
| | Max Input Voltage | | 7 | | V | $I_{IN}$ 250 µA |
| $V_{CH}$ | Clock Input High Voltage | 3.8 | $V_{CC}$ | | V | Driven by External Clock Generator |
| $V_{CL}$ | Clock Input Low Voltage | -0.03 | 0.8 | | V | Driven by External Clock Generator |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | | V | |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.8 | | V | |
| $V_{OH}$ | Output High Voltge | 2.4 | | | V | $I_{OH}$=-2.0 mA |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ -100mV | | | V | $I_{OH}$ = -100 µA |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | V | $I_{OL}$ = +5 mA |
| $V_{RH}$ | Reset Input High Voltage | 3.8 | $V_{CC}$ | | V | |
| $V_{RI}$ | Reset Input Low Voltage | -0.03 | 0.8 | | V | |
| $I_{IL}$ | Input Leakage | -2 | 2 | | µA | Test at 0V, $V_{CC}$ |
| $I_{OL}$ | Output Leakage | -2 | 2 | | µA | Test at 0V, $V_{CC}$ |
| $I_{IR}$ | Reset Input Current | | -80 | | µA | $V_{RL}$ = 0V |
| $I_{CC}$ | Supply Current | | 55 | 35 | mA | @ 33 MHz [1] |
| | | | 40 | 25 | mA | @ 25 MHz [1] |
| | | | 30 | 20 | mA | @ 20 MHz [1] |
| $I_{CC1}$ | Standby Current (HALT Mode) | | 15 | 9 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 25 MHz [1] |
| | | | 20 | 15 | | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 33 MHz [1] |
| | | | 12 | 7 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 20 MHz [1] |
| $I_{CC2}$ | Standby Current (STOP Mode) | | 10 | 1 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ [1] |
| $I_{AL}$ | Auto Latch Current | -16 | 16 | 5 | µA | |

**Note:**

[1] All inputs driven to 0V, or $V_{cc}$ and outputs floating.

## AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

| | | | $T_A$ = 0°C to +70°C | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 25 MHz | | 20 MHz | | Typical | |
| No | Sym | Parameter | Min | Max | Min | Max | Min | Max | $V_{cc}$=5.0V @ 25°C | Units |
| 1 | TdA(AS) | Address Valid To /AS Rise Delay | 13 | | 22 | | 26 | | | ns |
| 2 | TdAS(A) | /AS Rise To Address Hold Time | 20 | | 25 | | 28 | | | ns |
| 3 | TdAS(DI) | /AS Rise Data In Req'd Valid Delay | | 90 | | 130 | | 160 | | ns |
| 4 | TwAS | /AS Low Width | 20 | | 28 | | 36 | | | ns |
| 5 | TdAZ(DSR) | Address Float To /DS (Read) | 0 | | 0 | | 0 | | | ns |
| 6 | TwDSR | /DS (Read) Low Width | 65 | | 100 | | 130 | | | ns |
| 7 | TwDSW | /DS (Write) Low Width | 40 | | 65 | | 75 | | | ns |
| 8 | TdDSR(DI) | /DS (Read) To Data in Req'd Valid Delay | | 30 | | 78 | | 100 | | ns |
| 9 | ThDSR(DI) | /DS Rise (Read) to Data In Hold Time | 0 | | 0 | | 0 | | | ns |
| 10 | TdDS(A) | /DS Rise To Address Active Delay | 25 | | 34 | | 40 | | | ns |
| 11 | TdDS(AS) | /DS Rise To /AS Delay | 16 | | 30 | | 36 | | | ns |
| 12 | TdR/W(AS) | R/W To /AS Rise Delay | 12 | | 26 | | 32 | | | ns |
| 13 | TdDS(R/W) | /DS Rise To R/W Valid Delay | 12 | | 30 | | 36 | | | ns |
| 14 | TdDO(DSW) | Data Out To /DS (Write) Delay | 12 | | 34 | | 40 | | | ns |
| 15 | ThDSW(DO) | /DS Rise (Write) To Data Out Hold Time | 12 | | 34 | | 40 | | | ns |
| 16 | TdA(DI) | Address To Data In Req'd Valid Delay | | 110 | | 160 | | 200 | | ns |
| 17 | TdAS(DSR) | /AS Rise To /DS (Read) Delay | 20 | | 40 | | 48 | | | ns |
| 18 | TaDI(DSR) | Data In Set-up Time To /DS Rise Read | 16 | | 30 | | 36 | | | ns |
| 19 | TdDM(AS) | /DM To /AS Rise Delay | 10 | | 22 | | 26 | | | ns |
| 20 | TdDS(DM) | /DS Rise To /DM Valid Delay | | | | | | | 34* | ns |
| 21 | ThDS(A) | /DS Rise To Address Valid Hold Time | | | | | | | 34* | ns |
| 22 | TdXT(SCR) | XTAL Falling to SCLK Rising | | | | | | | 20* | ns |
| 23 | TdXT(SCF) | XTAL Falling to SCLK Falling | | | | | | | 23* | ns |
| 24 | TdXT(DSRF) | XTAL Falling to/DS Read Falling | | | | | | | 29* | ns |
| 25 | TdXT(DSRR) | XTAL Falling to /DS Read Rising | | | | | | | 29* | ns |
| 26 | TdXT(DSWF) | XTAL Falling to /DS Write Falling | | | | | | | 29* | ns |
| 27 | TdXT(DSWF) | XTAL Falling to /DS Write Rising | | | | | | | 29* | ns |
| 28 | TsW(XT) | Wait Set-up Time | | | | | | | 10* | ns |
| 29 | ThW(XT) | Wait Hold Time | | | | | | | 15* | ns |
| 30 | TwW | Wait Width (One Wait Time) | | | | | | | 25* | ns |

**Notes:**
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
* Preliminary value to be characterized.

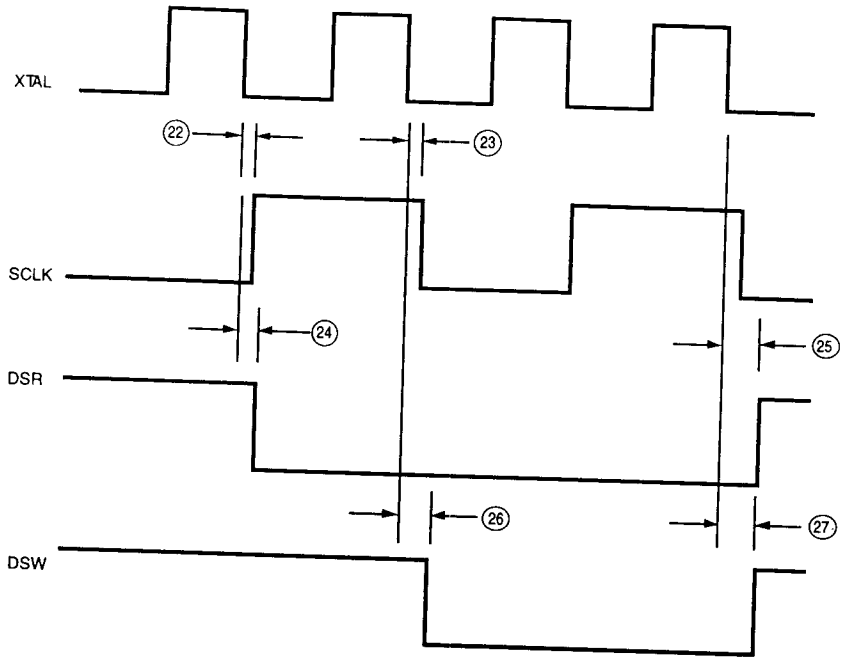



**Figure 25. XTAL/SCLK To DSR and DSW Timing**

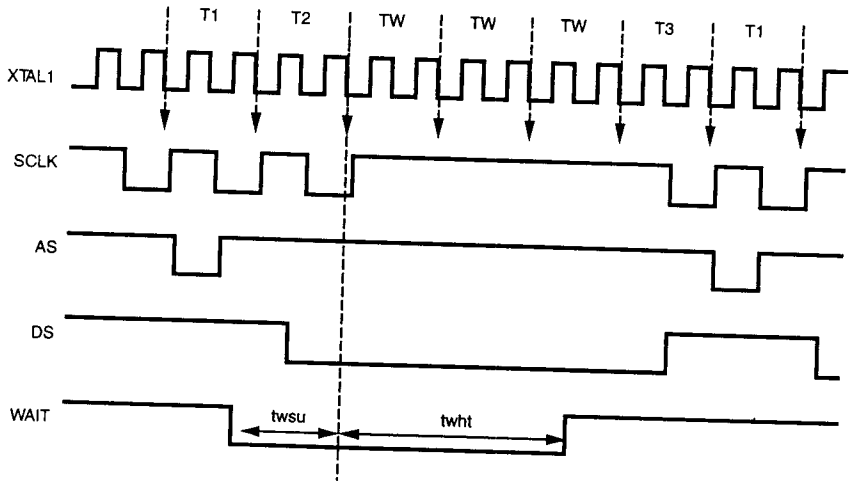



**Figure 26. XTAL/SCLK To WAIT Timing (25 MHz Device Only)**

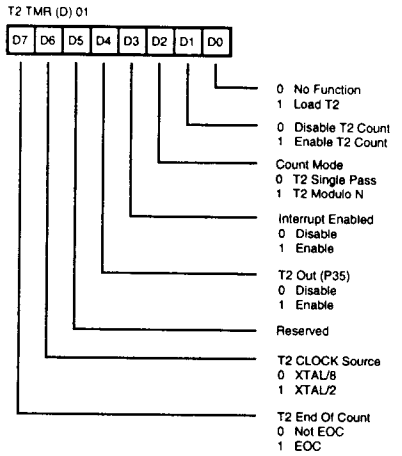



**Figure 30. Timer 2 Mode Register (01H: Read/Write)**

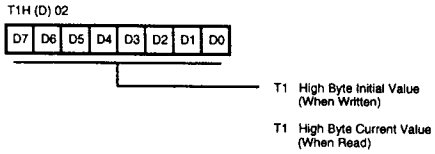



**Figure 31. Counter Timer 1 Register High Byte (02H: Read/Write)**

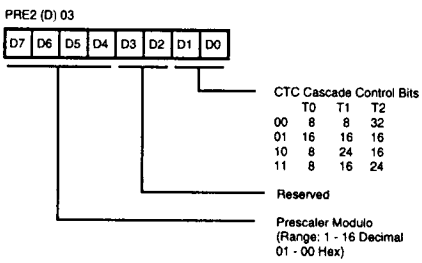



**Figure 32. Prescaler 2 Register High Byte (03H: Write Only)**

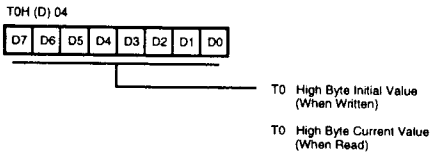



**Figure 33. Counter Timer 0 Register High Byte (04H: Read/Write)**

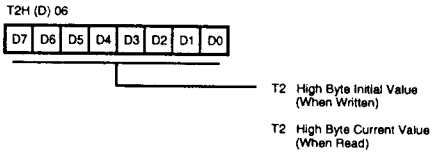



**Figure 34. Counter Timer 2 Register High Byte (06H: Read/Write)**

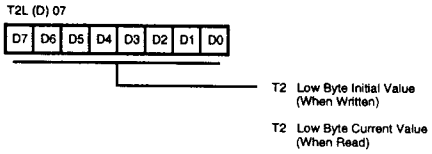



**Figure 35. Counter Timer 2 Register Low Byte (07H: Read/Write)**

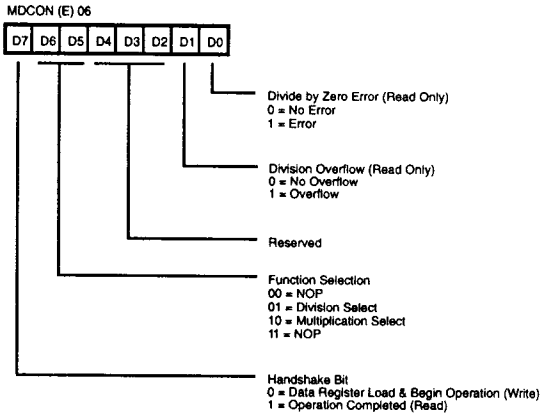
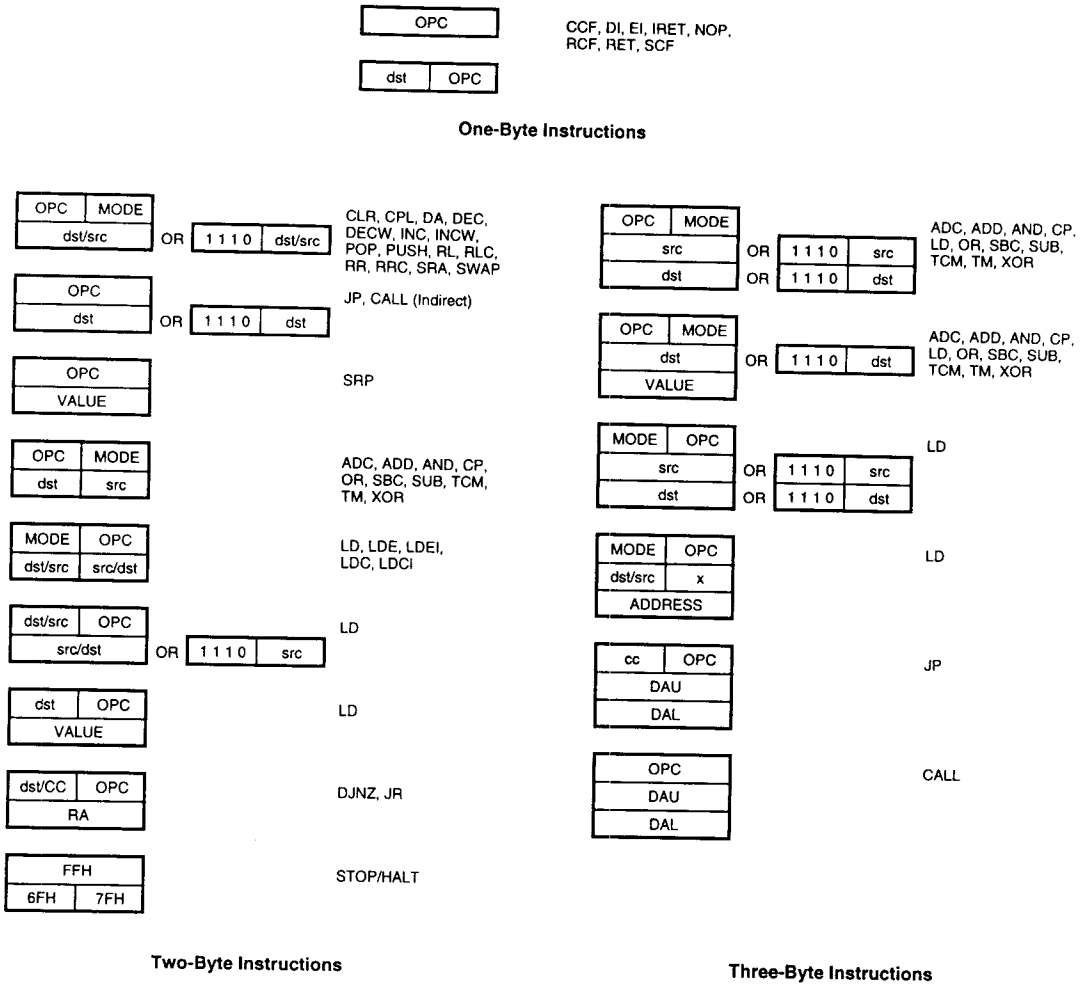



**Figure 36. Multiply/Divide Control Register (MDCON)**

## INSTRUCTION FORMATS




## INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

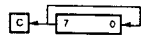
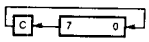
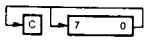
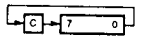
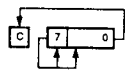
dst ← dst + src

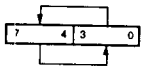
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

## INSTRUCTION SUMMARY (Continued)

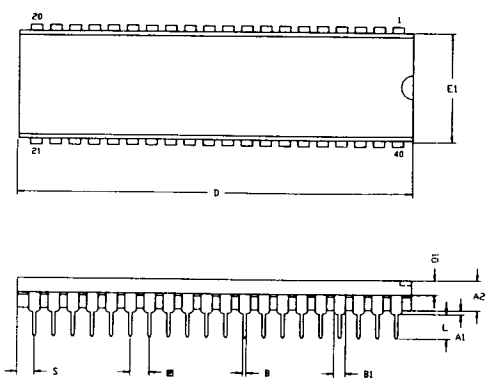
| Instruction and Operation | Address Mode dst | Address Mode src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **NOP** | | | FF | - | - | - | - | - | - |
| **OR** dst, src<br>dst←dst OR src | † | | 4[ ] | - | * | * | 0 | - | - |
| **POP** dst<br>dst←@SP;<br>SP←SP + 1 | R<br>IR | | 50<br>51 | - | - | - | - | - | - |
| **PUSH** src<br>SP←SP - 1;<br>@SP←src | | R<br>IR | 70<br>71 | - | - | - | - | - | - |
| **RCF**<br>C←0 | | | CF | 0 | - | - | - | - | - |
| **RET**<br>PC←@SP;<br>SP←SP + 2 | | | AF | - | - | - | - | - | - |
| **RL** dst<br>  | R<br>IR | | 90<br>91 | * | * | * | * | - | - |
| **RLC** dst<br>  | R<br>IR | | 10<br>11 | * | * | * | * | - | - |
| **RR** dst<br>  | R<br>IR | | E0<br>E1 | * | * | * | * | - | - |
| **RRC** dst<br>  | R<br>IR | | C0<br>C1 | * | * | * | * | - | - |
| **SBC** dst, src<br>dst←dst←src←C | † | | 3[ ] | * | * | * | * | 1 | * |
| **SCF**<br>C←1 | | | DF | 1 | - | - | - | - | - |
| **SRA** dst<br>  | R<br>IR | | D0<br>D1 | * | * | * | 0 | - | - |
| **SRP** src<br>RP←src | | Im | 31 | - | - | - | - | - | - |

| Instruction and Operation | Address Mode dst | Address Mode src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **STOP** | | | 6F | - | - | - | - | - | - |
| **SUB** dst, src<br>dst←dst←src | † | | 2[ ] | * | * | * | * | 1 | * |
| **SWAP** dst<br>  | R<br>IR | | F0<br>F1 | X | * | * | X | - | - |
| **TCM** dst, src<br>(NOT dst)<br>AND src | † | | 6[ ] | - | * | * | 0 | - | - |
| **TM** dst, src<br>dst AND src | † | | 7[ ] | - | * | * | 0 | - | - |
| **XOR** dst, src<br>dst←dst<br>XOR src | † | | B[ ] | - | * | * | 0 | - | - |

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

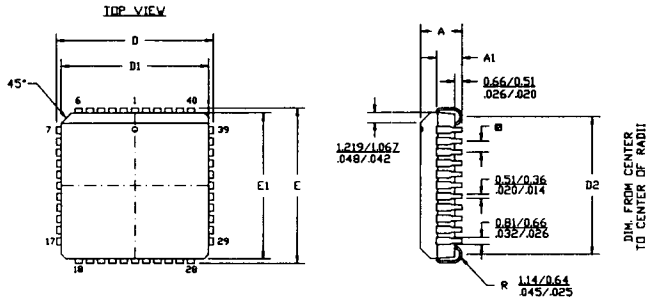
| Address Mode dst | Address Mode src | Lower Opcode Nibble |
|---|---|---|
| r | r | [2] |
| r | Ir | [3] |
| R | R | [4] |
| R | IR | [5] |
| R | IM | [6] |
| IR | IM | [7] |




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | 020 | .032 |
| A2 | 3.25 | 3.43 | 128 | .135 |
| B | 0.38 | 0.53 | 015 | 021 |
| B1 | 1.02 | 1.52 | 040 | 060 |
| C | 0.23 | 0.38 | 009 | 015 |
| D | 52.07 | 52.58 | 2.050 | 2.070 |
| E | 15.24 | 15.75 | .600 | .620 |
| E1 | 13.59 | 14.22 | .535 | .560 |
| eB | 2.54 TYP | | 100 TYP | |
| eA | 15.49 | 16.51 | .610 | .650 |
| L | 3.18 | 3.81 | .125 | 150 |
| D1 | 1.52 | 1.91 | 060 | 075 |
| S | 1.52 | 2.29 | .060 | .090 |

CONTROLLING DIMENSIONS : INCH

**40-Pin DIP Package Diagram**




NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM
INCH

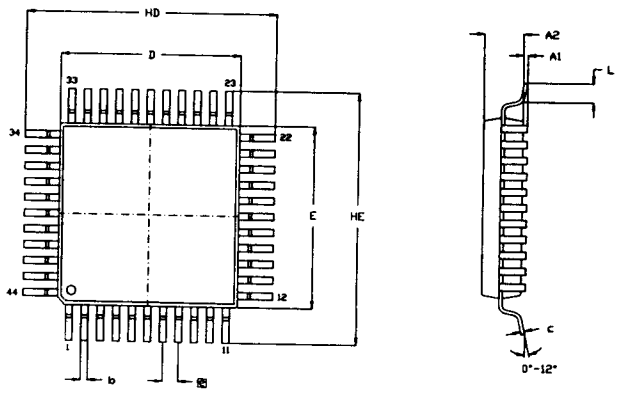
| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.27 | 4.57 | .168 | .180 |
| A1 | 2.67 | 2.92 | .105 | .115 |
| D/E | 17.40 | 17.65 | .685 | .695 |
| D1/E1 | 16.51 | 16.66 | .650 | .656 |
| D2 | 15.24 | 16.00 | .600 | .630 |
| eB | 1.27 TYP | | .050 TYP | |

**44-Pin PLCC Package Diagram**

## PACKAGE INFORMATION (Continued)

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

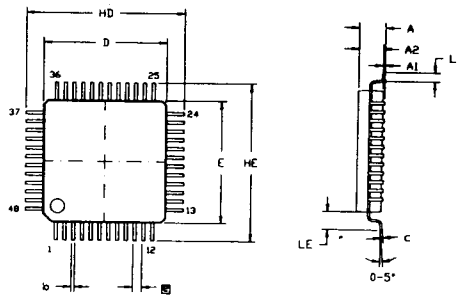
| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.05 | 0.25 | .002 | .010 |
| A2 | 2.05 | 2.25 | .081 | .089 |
| b | 0.25 | 0.45 | .010 | .018 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 13.70 | 14.30 | .539 | .563 |
| D | 9.90 | 10.10 | .390 | .398 |
| HE | 13.70 | 14.30 | .539 | .563 |
| E | 9.90 | 10.10 | .390 | .398 |
| e | 0.80 TYP | | .031 TYP | |
| L | 0.60 | 1.20 | .024 | .047 |




**44-Pin QFP Package Diagram**

| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.60 | .053 | .063 |
| A1 | 0.05 | 0.20 | .002 | .008 |
| A2 | 1.30 | 1.50 | .051 | .059 |
| b | 0.15 | 0.26 | .006 | .010 |
| c | 0.10 | 0.18 | .004 | .007 |
| HD | 8.60 | 9.40 | .339 | .370 |
| D | 6.90 | 7.10 | .272 | .280 |
| HE | 8.60 | 9.40 | .339 | .370 |
| E | 6.90 | 7.10 | .272 | .280 |
| e | 0.50 TYP | | .020 TYP | |
| L | 0.30 | 0.70 | .012 | .028 |
| LE | 0.90 | 1.10 | .035 | .043 |

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"




**48-Pin VQFP Package Diagram**