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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z86c9325psg">https://www.e-xfl.com/product-detail/zilog/z86c9325psg</a>

## GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and Counter/Timer blocks.

### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	$V_{CC}$ GND	$V_{DD}$ $V_{SS}$

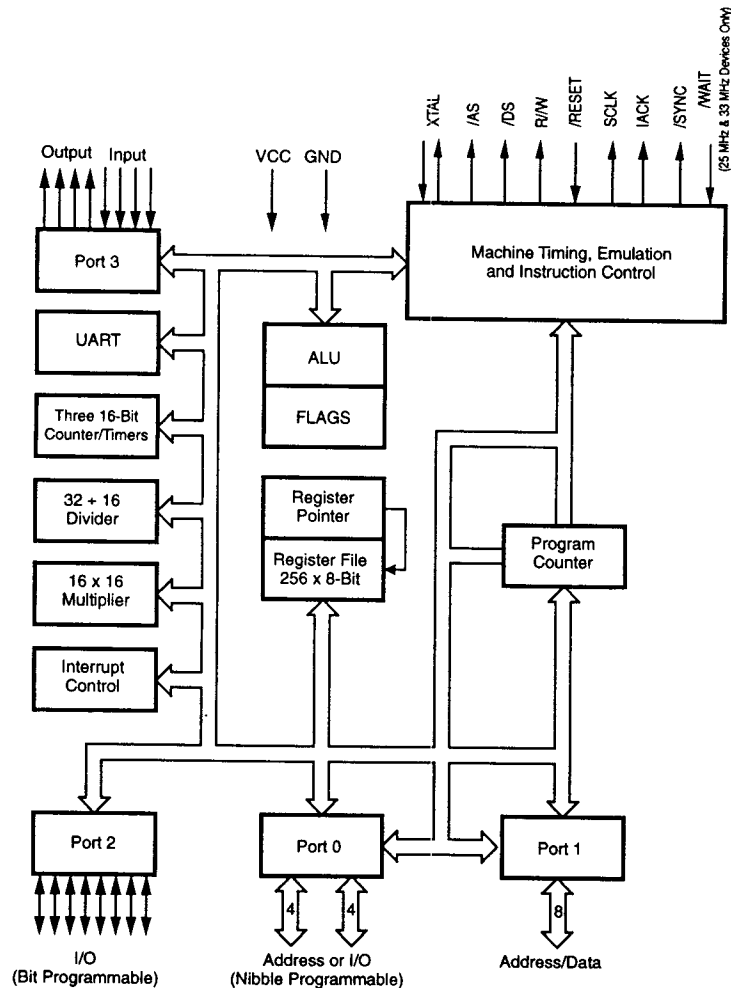


Figure 1. Functional Block Diagram

## PIN DESCRIPTION

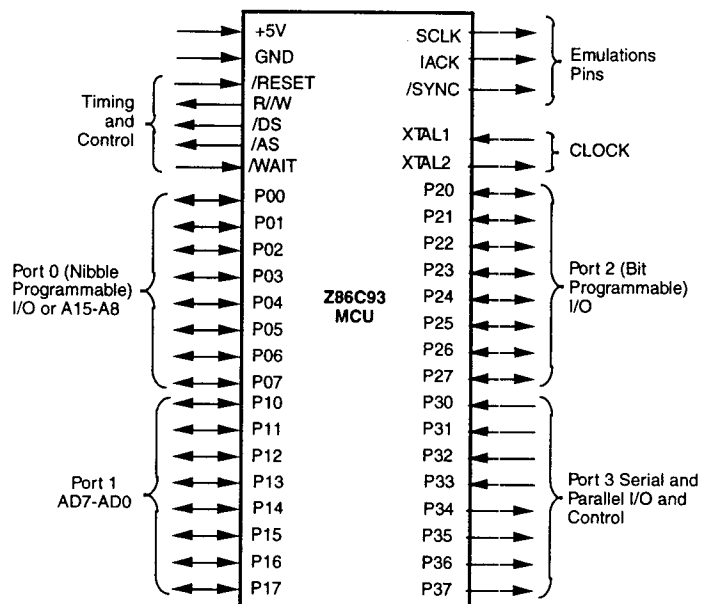


Figure 2. Pin Functions

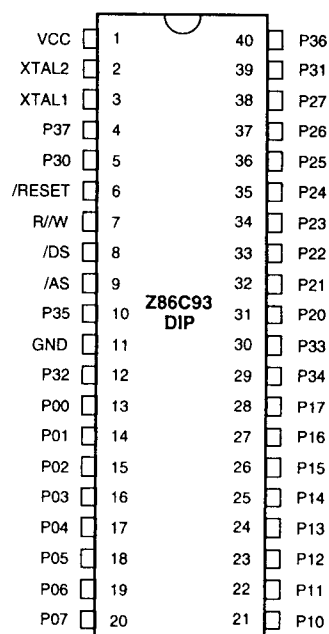


Figure 3. 40-Pin DIP

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input
2	XTAL1	Crystal, Oscillator Clock	Input
3	XTAL2	Crystal, Oscillator Clock	Output
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground, GND	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pin 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pin 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

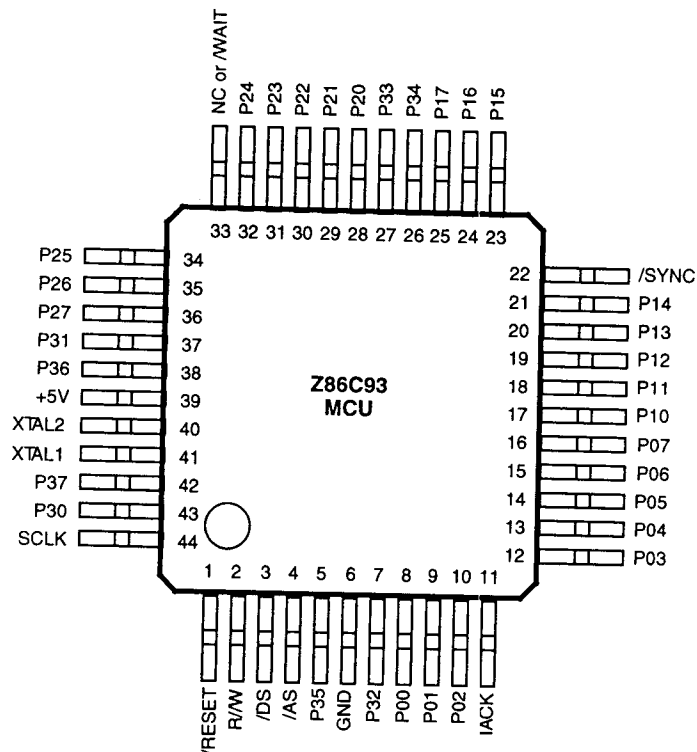
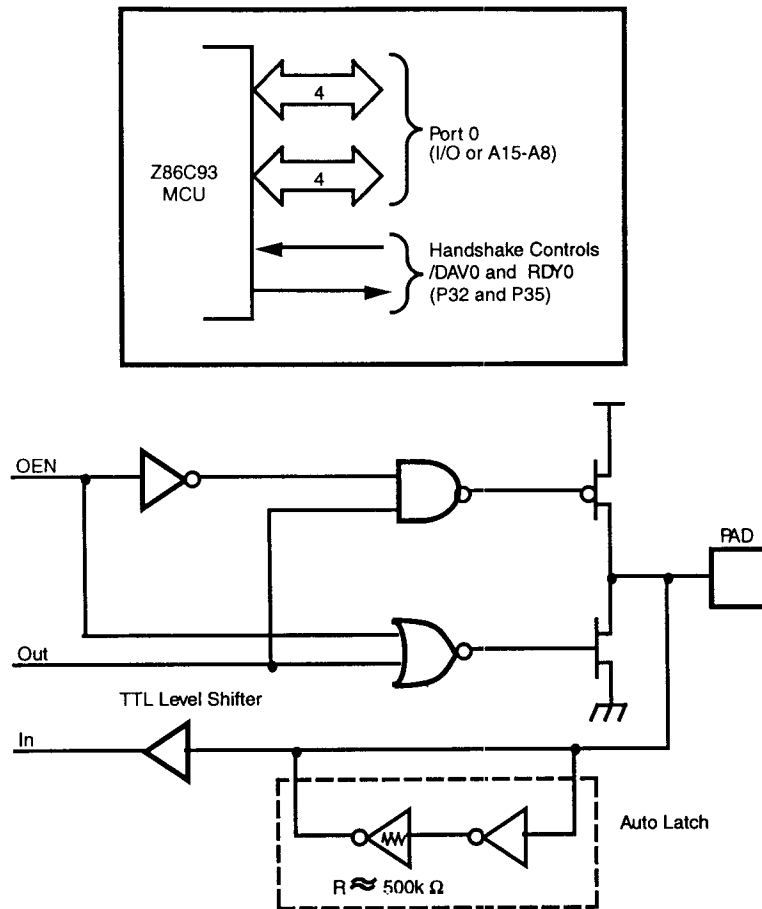


Figure 5. 44-Pin QFP

Table 3. 44-Pin QFP Pin Identification

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	/RESET	Reset	Input	26	P34	Port 3 pin 4	Output
2	R/W	Read/Write	Output	27	P33	Port 3 pin 3	Input
3	/DS	Data Strobe	Output	28-32	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
4	/AS	Address Strobe	Output	33	N/C	Not Connected (20 MHz)	Input
5	P35	Port 3 pin 5	Input		/WAIT	WAIT (25 or 33 MHz)	Input
6	GND	Ground GND	Input	34-36	P25-P27	Port 2 pin 5,6,7	In/Output
7	P32	Port 3 pin 2	Input	37	P31	Port 3 pin 1	Input
8-10	P00-P02	Port 0 pin 0,1,2	In/Output	38	P36	Port 3 pin 6	Output
11	IACK	Int. Acknowledge	Output	39	V <sub>cc</sub>	Power Supply	Input
12-16	P03-P07	Port 0 pin 3,4,5,6,7	In/Output	40	XTAL2	Crystal, Osc. Clock	Output
17-21	P10-P14	Port 1 pin 0,1,2,3,4	In/Output	41	XTAL1	Crystal, Osc. Clock	Input
22	/SYNC	Synchronize Pin	Output	42	P37	Port 3 pin 7	Output
23-25	P15-P17	Port 1 pin 5,6,7	In/Output	43	P30	Port 3 pin 0	Input
				44	SCLK	System Clock	Output



**Figure 7. Port 0 Configuration**

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal

assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

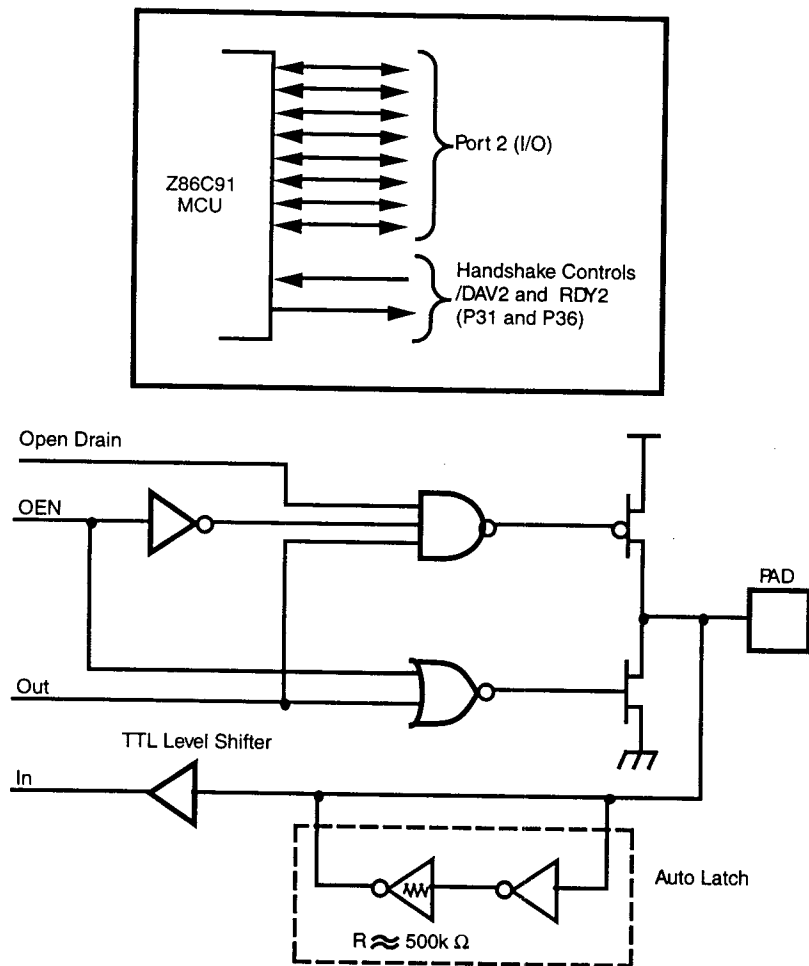


Figure 9. Port 2 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output

ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

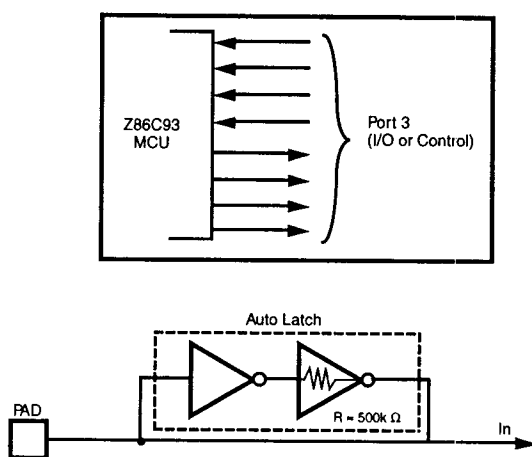


Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In	$T_{IN}$	IRQ3	D/R	D/R	Serial In	
P31	In		IRQ2				
P32	In		IRQ0				
P33	In		IRQ1				
P34	Out	$T_{OUT}$		R/D	R/D	Serial Out	DM
P35	Out						
P36	Out						
P37	Out						

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted,

regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

## PIN FUNCTIONS (Continued)

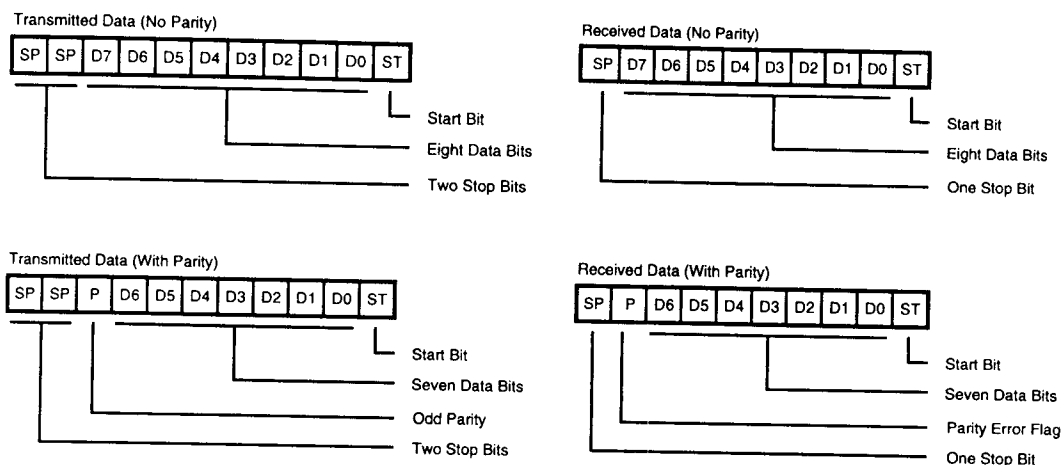


Figure 11. Serial Data Formats

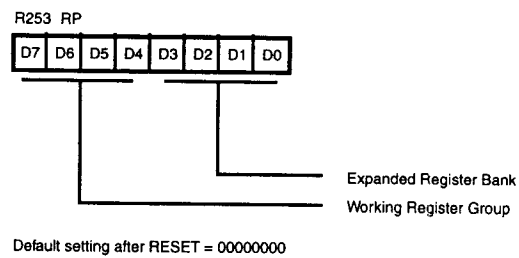
## ADDRESS SPACE

**Program Memory.** The Z86C93 can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

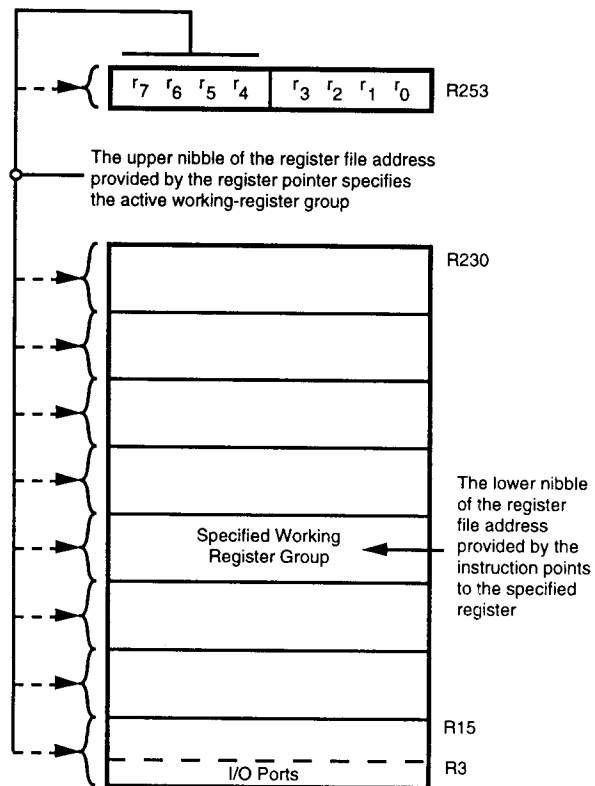
**Data Memory.** The Z96C93 can address up to 64 Kbytes of external data memory. External data memory is included with, or separated from, the external program memory

space. /DM, an optional I/O function that can be programmed to appear on pin P34 is used to distinguish between data and program memory space (Figure 12). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.





**Figure 14. Register Pointer Register**



**Figure 15. Register Pointer**

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## FUNCTIONAL DESCRIPTION (Continued)

**DIVZR. Division by Zero (D0).** When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined  
x = Irrelevant  
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

**Performance of multiplication.** The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7  $\mu$ s. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30  
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1  $\mu$ s. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

**Performance of division.** The actual division needs 20 internal clock cycles. This translates to 2.0  $\mu$ s for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42  
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6  $\mu$ s at 10 MHz.

## Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

## FUNCTIONAL DESCRIPTION (Continued)

### Operation

Except for the programmable down counter length and clock input, T2 is identical to T0.

T0 and T1 retain all their features except that now they are extendable interims of the down-counter length.

The output of T2, under program control, goes to an output pin (P35). Also, the interrupt generated by T2 is ORed with the interrupt request generated by P32. Note that the service routine then has to poll the T2 flag bit and also clear it (Bit 7 of T2 Timer Mode Register).

On power up, T0 and T1 are configured in the 8-bit down counter length mode (to be compatible with Z86C91) and T2 is in the 32-bit mode with its output disabled (no interrupt is generated and T2 output DOES NOT go to port pin P35).

The UART uses T0 for generating the bit clock. This means, while using UART, T0 should be in 8-bit mode. So, while using the UART there are only two independent timer/counters.

The counters are configured in the following manner:

Timer	Mode	Byte
T0	8-bit	Low Byte (T0)
T0	16-bit	High Byte (T0) + Low Byte (T0)
T1	8-bit	Low Byte (T1)
T1	16-bit	High Byte (T1) + Low Byte (T1)
T1	24-bit	High Byte (T0) + High Byte (T1) + Low Byte (T1)
T2	16-bit	High Byte (T2) + Low Byte (T2)
T2	24-bit	High Byte (T0) + High Byte (T2) + Low Byte (T2)
T2	32-bit	High Byte (T0) + High Byte (T1) + High Byte (T2) + Low Byte (T2)

Note that the T2 interrupt is logically ORed with P32 to generate IRQ0.

The T2 Timer Mode register is shown in Figure 19. Upon reaching end of count, bit 7 of this register is set to one. This bit IS NOT reset in hardware and it has to be cleared by the interrupt service routine.

T2 interrogates the state of the Count Mode Bit (D2) once it has counted down to its zero value. T2 then makes the decision to continue counting (Module N Mode) or stop (Single Pass Mode). Observe this functionality if attempting to modify the count mode prior to the end of count bit (D7) being set.

The register map of the new CTC registers is shown in Figure 13. T0 high byte and T1 high byte are at the same relative locations as their respective low bytes, but in a different register bank.

The T2 prescaler register is shown in Figure 19. Bits 1 and 0 of this register control the various cascade modes of the counters.

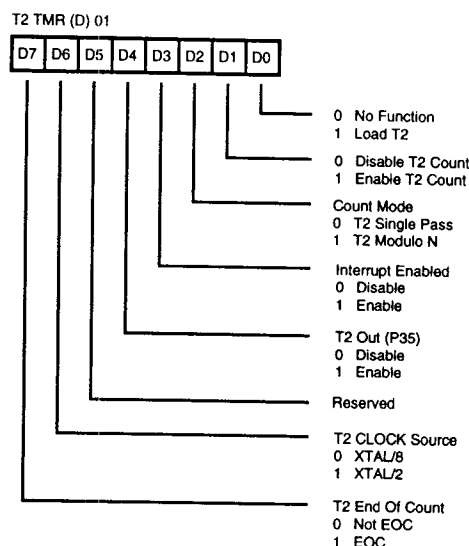


Figure 19. T2 Timer Mode Register (T2)

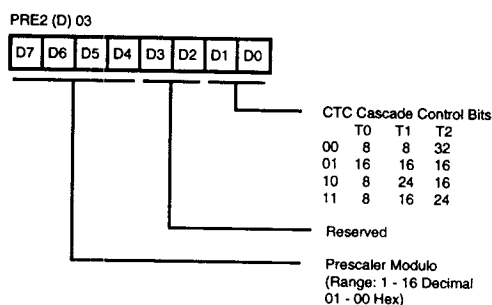


Figure 20. T2 Prescaler Register (PRE2)

## Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58<sup>th</sup> TpC cycle following the internal sample point, which corresponds to the 63<sup>rd</sup> TpC cycle following the external interrupt sample point.

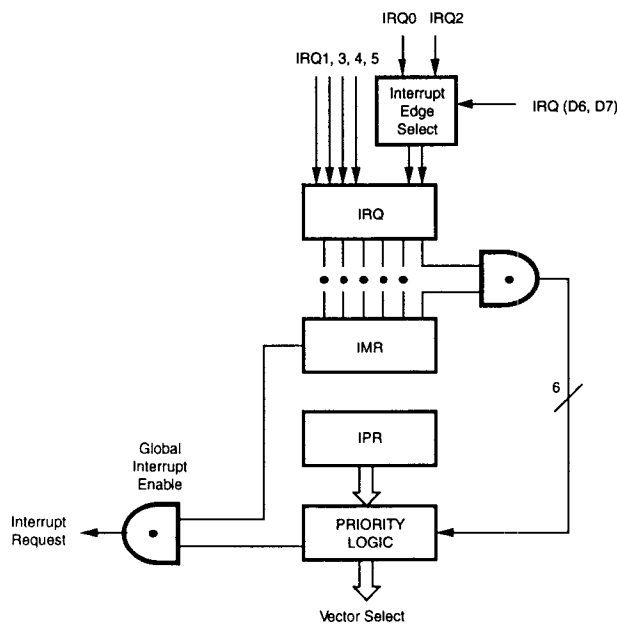


Figure 21. Interrupt Block Diagram

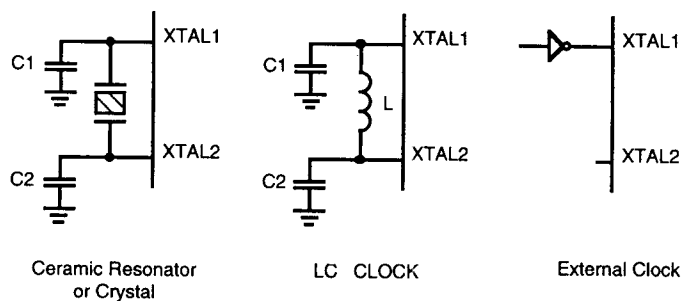
**Table 7. Interrupt Types, Sources, and Vectors**

Name	Source	Vector Location	Comments
IRQ 0	/DAV 0, P32, T2	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ 1,	P33	2, 3	External (P33), Fall Edge Triggered
IRQ 2	/DAV 2, P31, T <sub>IN</sub>	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ 3	P30, Serial In	6, 7	External (P30), Fall Edge Triggered
IRQ 4	T0, Serial Out	8, 9	Internal
IRQ 5	T1	10, 11	Internal

## Clock

The Z86C93 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The external clock levels

are not TTL. The crystal should be AT cut, 1 MHz to 25 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground (Figure 20).



**Figure 22. Oscillator Configuration**

## Power Down Modes

**HALT.** Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R/W are HIGH. The outputs retain their preview value, and the inputs are floating.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10  $\mu$ A or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF NOP ; clear the pipeline
6F STOP ; enter STOP mode
or
FF NOP ; clear the pipeline
7F HALT ; enter HALT mode
```

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage*	-0.3	+7.0	V
$T_{STG}$	Storage Temp	-65	+150	C
$T_A$	Oper Ambient Temp	†	†	C

\* Voltages on all pins with respect to GND.

† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).

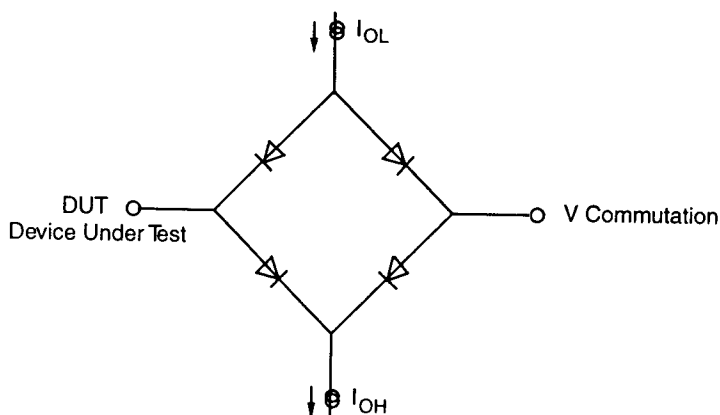


Figure 23. Test Load Diagram

## AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

No	Sym	Parameter	T <sub>a</sub> = 0°C to +70°C						Typical V <sub>cc</sub> =5.0V @ 25°C	Units
			33 MHz		25 MHz		20 MHz			
			Min	Max	Min	Max	Min	Max		
1	TdA(AS)	Address Valid To /AS Rise Delay	13		22		26			ns
2	TdAS(A)	/AS Rise To Address Hold Time	20		25		28			ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		90		130		160		ns
4	TwAS	/AS Low Width	20		28		36			ns
5	TdAZ(DSR)	Address Float To /DS (Read)	0		0		0			ns
6	TwDSR	/DS (Read) Low Width	65		100		130			ns
7	TwDSW	/DS (Write) Low Width	40		65		75			ns
8	TdDSR(DI)	/DS (Read) To Data in Req'd Valid Delay		30		78		100		ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0			ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		34		40			ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36			ns
12	TdR/W(AS)	R/W To /AS Rise Delay	12		26		32			ns
13	TdDS(R/W)	/DS Rise To R/W Valid Delay	12		30		36			ns
14	TdDO(DSW)	Data Out To /DS (Write) Delay	12		34		40			ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40			ns
16	TdA(DI)	Address To Data In Req'd Valid Delay		110		160		200		ns
17	TdAS(DSR)	/AS Rise To /DS (Read) Delay	20		40		48			ns
18	TaDI(DSR)	Data In Set-up Time To /DS Rise Read	16		30		36			ns
19	TdDM(AS)	/DM To /AS Rise Delay	10		22		26			ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay							34*	ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time							34*	ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising							20*	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling							23*	ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling							29*	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising							29*	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling							29*	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising							29*	ns
28	TsW(XT)	Wait Set-up Time							10*	ns
29	ThW(XT)	Wait Hold Time							15*	ns
30	TwW	Wait Width (One Wait Time)							25*	ns

### Notes:

When using extended memory timing add 2 TpC.

Timing numbers given are for minimum TpC.

\* Preliminary value to be characterized.

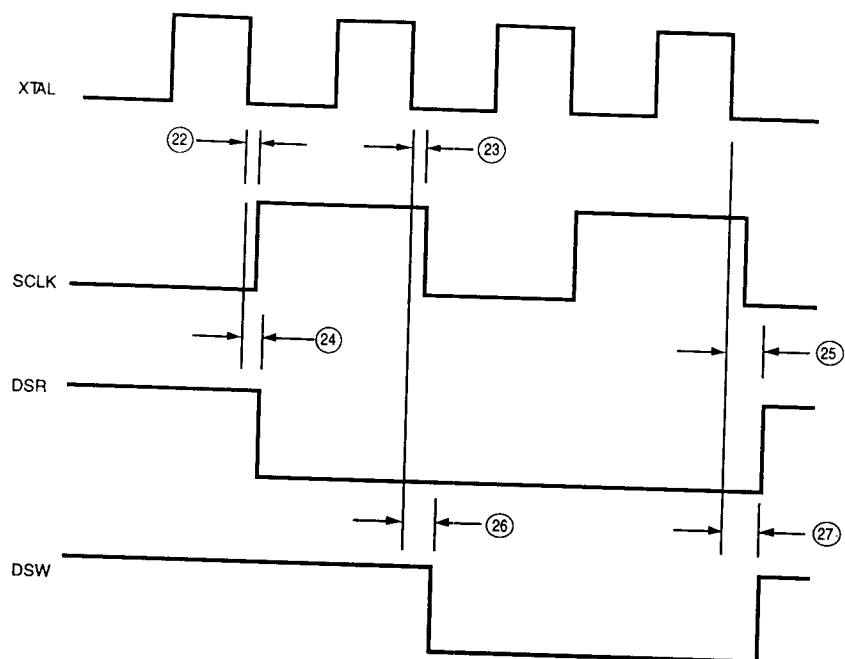


Figure 25. XTAL/SCLK To DSR and DSW Timing

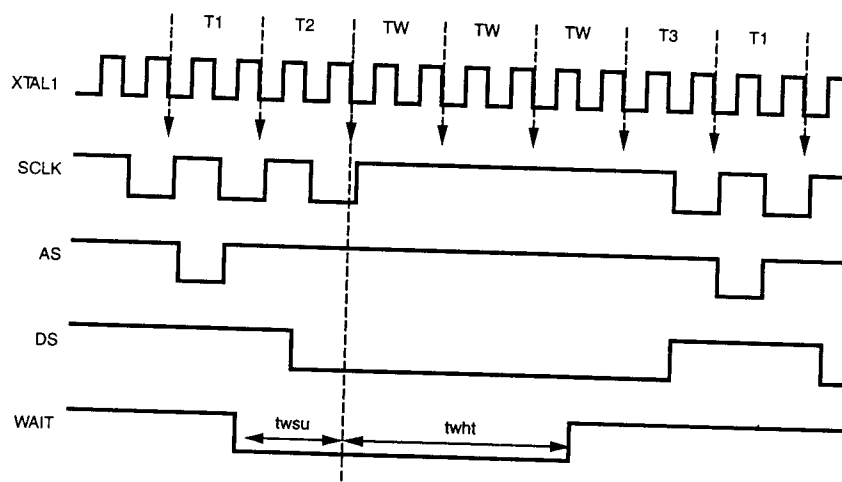


Figure 26. XTAL/SCLK To WAIT Timing  
(25 MHz Device Only)



## AC CHARACTERISTICS

### Additional Timing Diagram

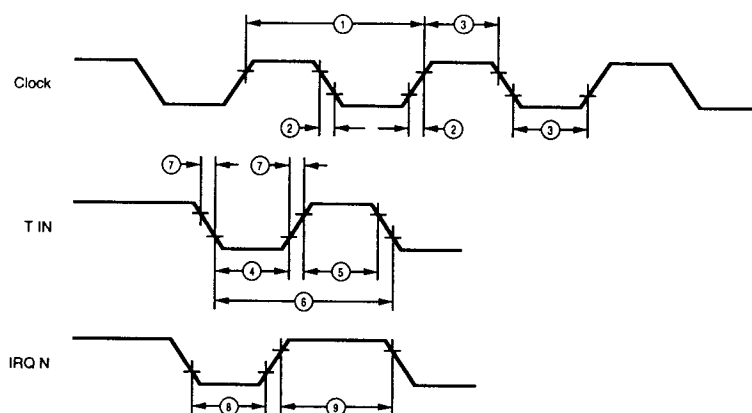


Figure 27. Additional Timing

## AC CHARACTERISTICS

### Additional Timing Table

No	Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C						Units	Notes
			33 MHz		24 MHz		20 MHz			
			Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	30	1000	42	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		5		10		10	ns	[1]
3	TwC	Input Clock Width	10		11		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC			[2,3]

#### Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request via Port 3.
- [4] Interrupt request via Port 3 (P31-P33).
- [5] Interrupt request via Port 30.

# AC CHARACTERISTICS Handshake Timing Table

No	Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C		Units	Data Direction
			Min	Max		
1	TsDI(DAV)	Data In Setup Time to /DAV	0		ns	In
2	ThDI(DAV)	RDY to Data In Hold Time	0		ns	In
3	TwDAV	/DAV Width	40		ns	In
4	TdDAVIf(RDYf)	/DAV to RDY Delay		70	ns	In
5	TdDAVIf(RDYr)	DAV Rise to RDY Wait Time		40	ns	In
6	TdRDYOr(DAVIf)	RDY Rise to DAV Delay	0		ns	In
7	TdDO(DAV)	Data Out to DAV Delay		TpC	ns	Out
8	TdDAVOf(RDYIf)	/DAV to RDY Delay	0		ns	Out
9	TdRDYIf(DAVOr)	RDY to /DAV Rise Delay		70	ns	Out
10	TwRDY	RDY Width	40		ns	Out
11	TdRDYIf(DAVOf)	RDY Rise to DAV Wait Time		40	ns	Out

## Z8 CONTROL REGISTERS (Continued)

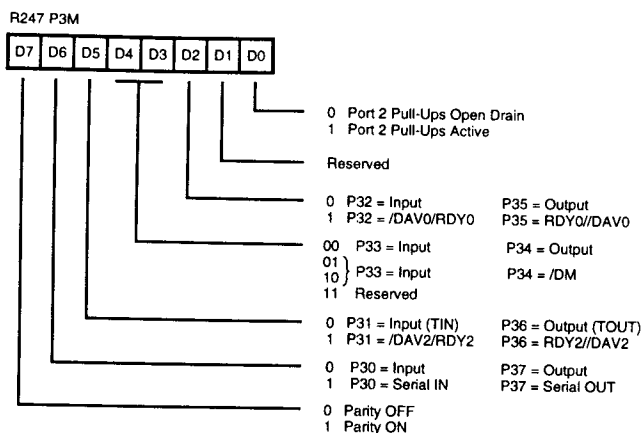


Figure 44. Port 3 Mode Register  
(F7H: Write Only)

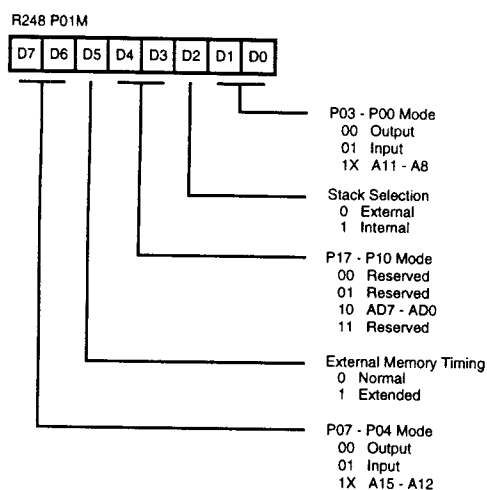


Figure 45. Ports 0 and 1 Mode Registers  
(F8H: Write Only)

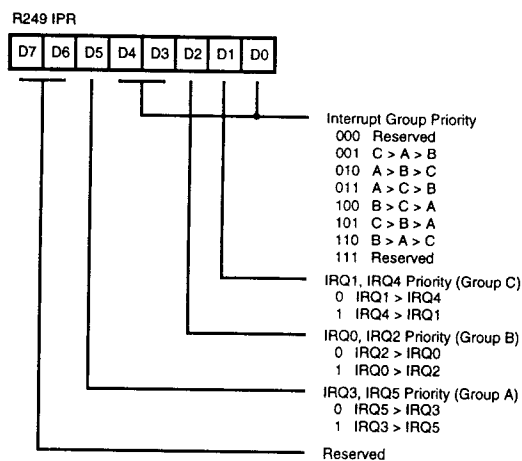
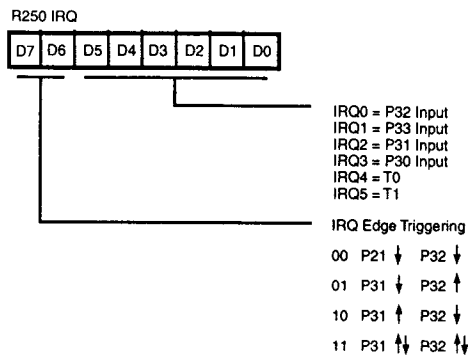
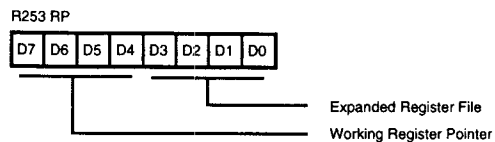


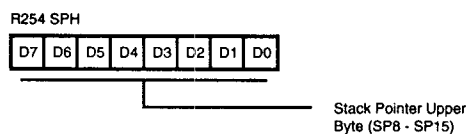
Figure 46. Interrupt Priority Register  
(F9H: Write Only)



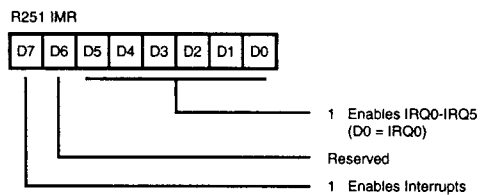
**Figure 47. Interrupt Request Register (FAH: Read/Write)**



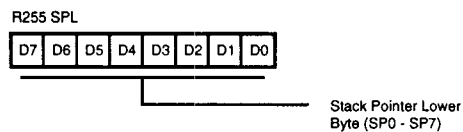
**Figure 50. Register Pointer (FDH: Read/Write)**



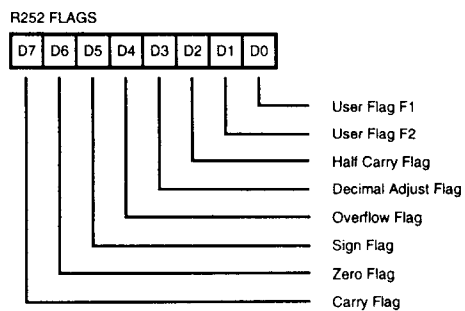
**Figure 51. Stack Pointer High (FEH: Read/Write)**



**Figure 48. Interrupt Mask Register (FBH: Read/Write)**



**Figure 52. Stack Pointer Low (FFH: Read/Write)**



**Figure 49. Flag Register (FCH: Read/Write)**

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## ORDERING INFORMATION

### Z86C93

20 MHz

44-pin PLCC  
Z86C9320VSC

44-pin QFP  
Z86C9320FSC

40-pin DIP  
Z86C9320PSC

48-pin VQFP  
Z80C9320ASC

25 MHz

44-pin PLCC  
Z86C9325VSC

44-pin QFP  
Z86C9325FSC

40-pin DIP  
Z86C9325PSC

48-pin VQFP  
Z80C9325ASC

33 MHz

44-pin PLCC  
Z86C9333VSC

44-pin QFP  
Z86C9333FSC

40-pin DIP  
Z86C9333PSC

48-pin VQFP  
Z80C9333ASC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

#### Package

V = Plastic Leaded Chip Carrier

P = Plastic Dual In Line Package

#### Longer Lead Time

F = Plastic Quad Flat Pack

A = Very Small Quad Flat Pack

#### Temperature

S = 0°C to +70°C

#### Speed

20 = 20 MHz

25 = 25 MHz

33 = 33 MHz

#### Environmental

C = Standard Flow

#### Example:

Z 86C93 33 V S C is an 86C93 33 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow

