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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9325vsc

GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and Counter/Timer blocks.

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

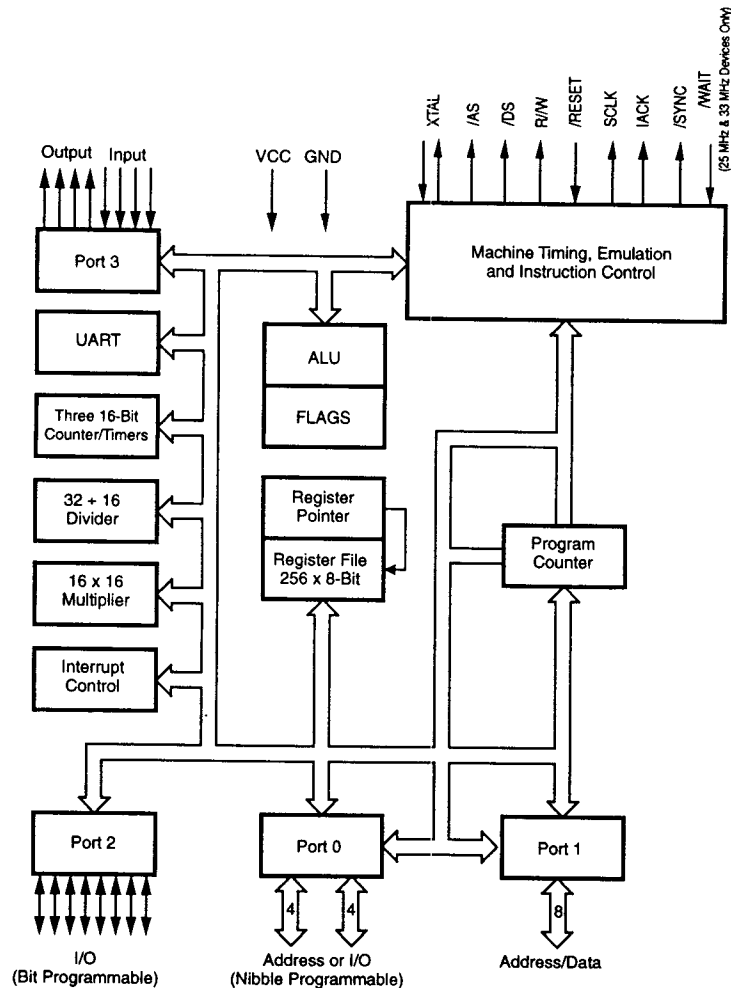


Figure 1. Functional Block Diagram

PIN DESCRIPTION

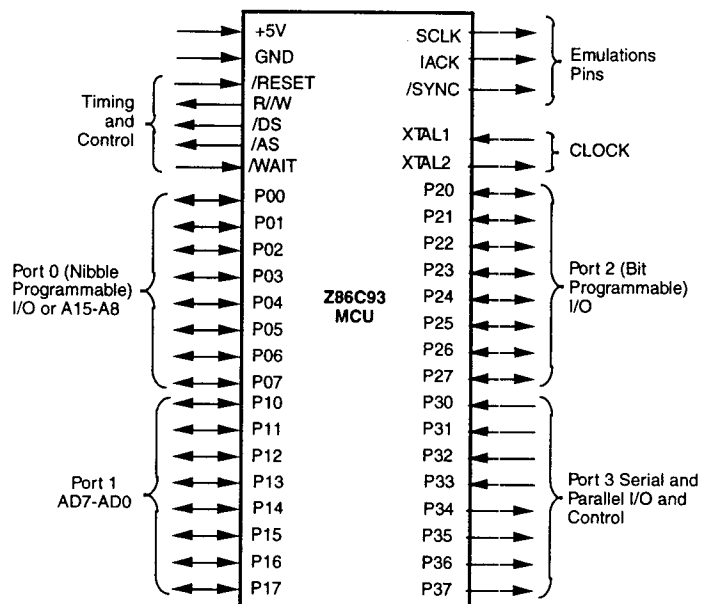


Figure 2. Pin Functions

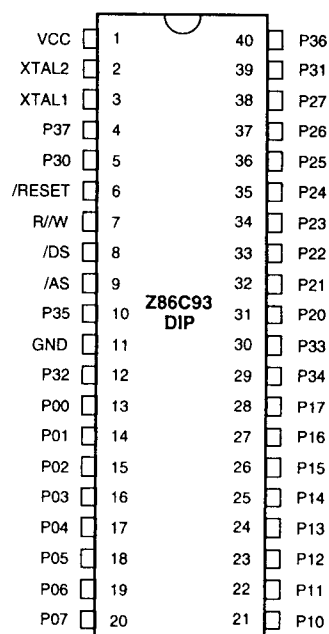


Figure 3. 40-Pin DIP

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL1	Crystal, Oscillator Clock	Input
3	XTAL2	Crystal, Oscillator Clock	Output
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground, GND	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pin 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pin 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

PIN DESCRIPTION (Continued)

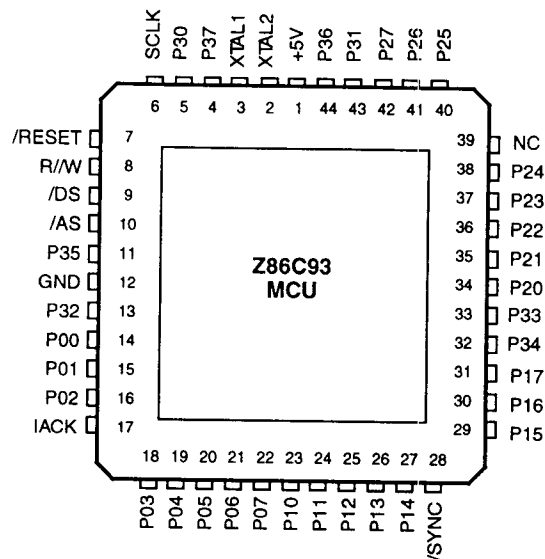


Figure 4. 44-Pin PLCC

Table 2. 44-Pin PLCC Pin Identification

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	V _{cc}	Power Supply	Input	14-16	P00-P02	Port 0 pin 0,1,2	In/Output
2	XTAL2	Crystal, Osc. Clock	Output	17	IACK	Int. Acknowledge	Output
3	XTAL1	Crystal, Osc. Clock	Input	18-22	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
5	P30	Port 3 pin 0	Input	28	/SYNC	Synchronize Pin	Output
6	SCLK	System Clock	Output	29-31	P15-P17	Port 1 pin 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output
8	R/W	Read/Write	Output	33	P33	Port 3 pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected (20 MHz)	Input
11	P35	Port 3 pin 5	Output		/WAIT	WAIT (25 or 33 MHz)	Input
12	GND	Ground GND	Input	40-42	P25-P27	Port 2 pin 5,6,7	In/Output
13	P32	Port 3 pin 2	Input	43	P31	Port 3 pin 1	Input
				44	P36	Port 3 pin 6	Output

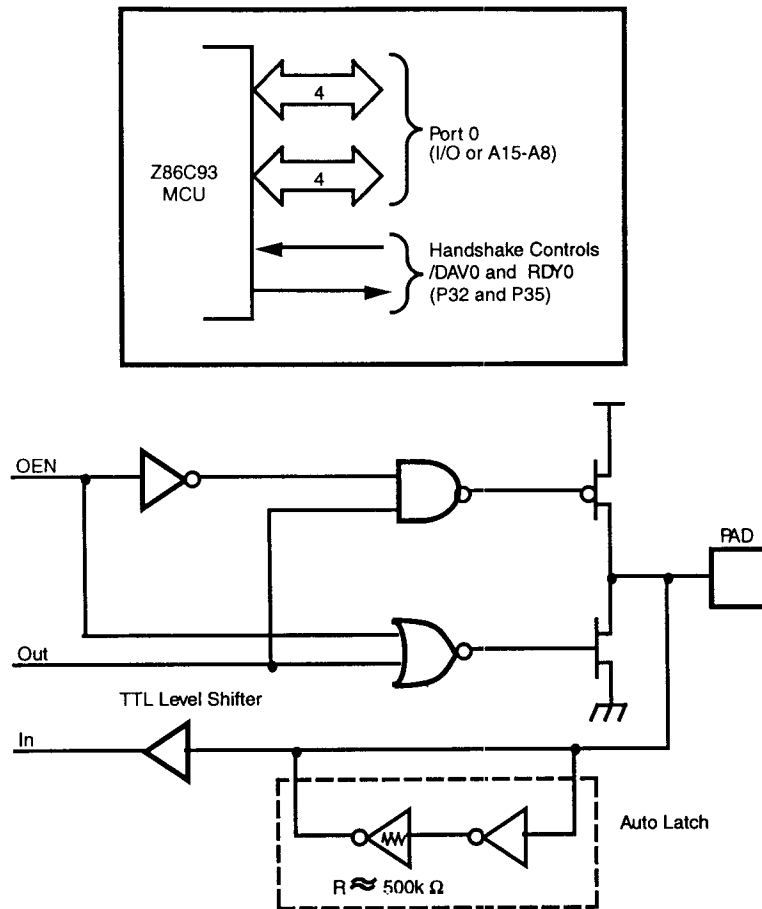


Figure 7. Port 0 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output

ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

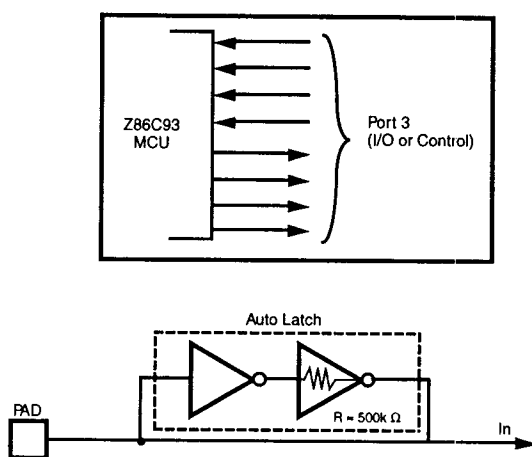


Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In	T_{IN}	IRQ3	D/R	D/R	Serial In	
P31	In		IRQ2				
P32	In		IRQ0				
P33	In		IRQ1				
P34	Out	T_{OUT}		R/D	R/D	Serial Out	DM
P35	Out						
P36	Out						
P37	Out						

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted,

regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

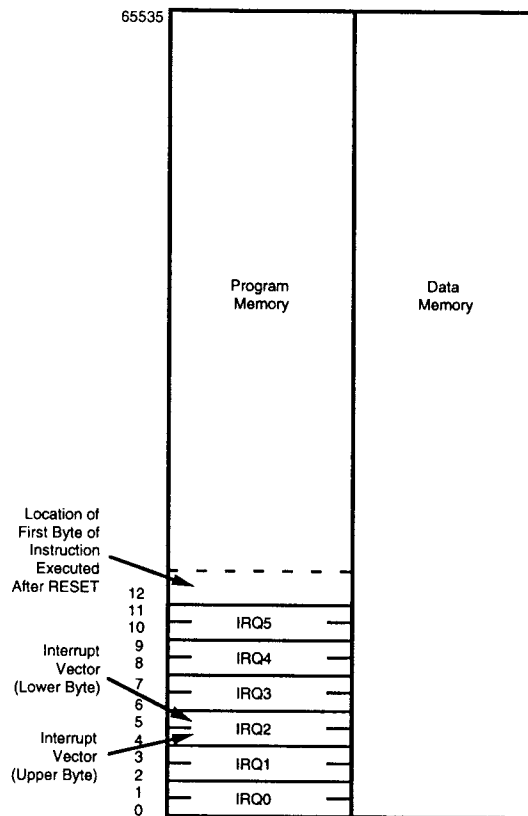


Figure 12. Program and Data Memory Configuration

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area (Figure 13). The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14). The registers that are used in the multiply/divide unit reside in the Expanded Register File at Bank E and those for the additional timer control words reside in Bank D. The rest of the Expanded Register is not physically implemented and is open for future expansion.

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control

and status registers. The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C93 also allows short 4-bit register addressing using the Register Pointer (Figure 15). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Group E0-EF can only be accessed through working registers and indirect addressing modes.

Stack. The Z86C93 has a 16-bit Stack Pointer (R254-R255), used for external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH, Bits 8-15) can be used as a general-purpose register when using internal stack only.

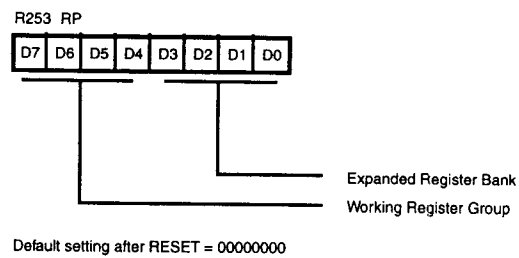


Figure 14. Register Pointer Register

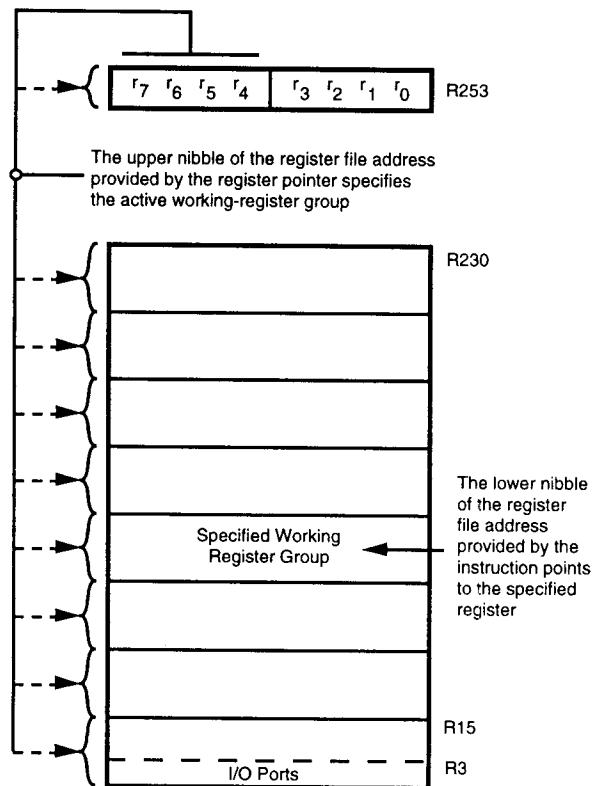


Figure 15. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

DIVZR. Division by Zero (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined
x = Irrelevant
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

Performance of multiplication. The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7 μ s. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 μ s. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

Performance of division. The actual division needs 20 internal clock cycles. This translates to 2.0 μ s for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 μ s at 10 MHz.

Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

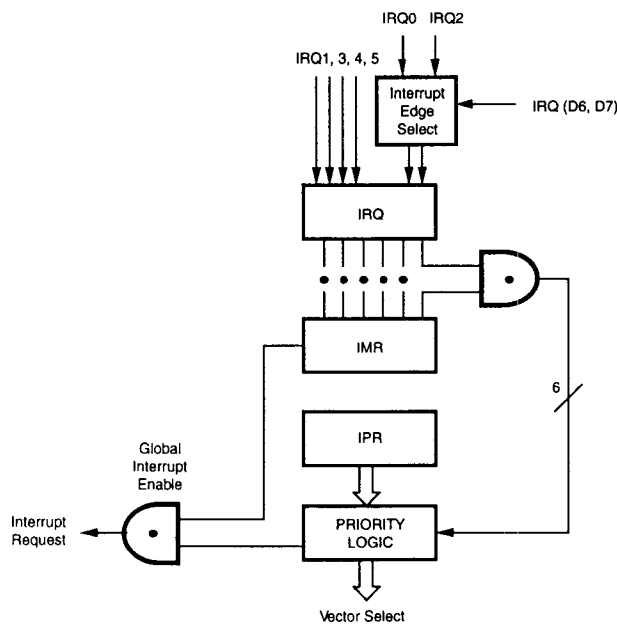


Figure 21. Interrupt Block Diagram

DC ELECTRICAL CHARACTERISTICS

$$V_{CC} = 3.3V \pm 10\%$$

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} = 250 \mu\text{A}$
V_{CH}	Clock Input High Voltage	$0.8 V_{CC}$	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	$0.1 \times V_{CC}$		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	$0.7 \times V_{CC}$	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	$0.1 \times V_{CC}$		V	
V_{OH}	Output High Voltage	1.8			V	$I_{OH} = -1.0 \text{ mA}$
V_{OHI}	Output High Voltage	$V_{CC} - 100\text{mV}$			V	$I_{OH} = -100 \mu\text{A}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +1.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	$0.8 \times V_{CC}$	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	$0.1 \times V_{CC}$		V	
I_{IL}	Input Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		μA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		μA	$V_{RI} = 0\text{V}$
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Stand By Current (HALT Mode)		12	8	mA	HALT Mode $V_{IN} = 0\text{V}$, V_{CC} @ 25 MHz [1]
I_{CC2}	Stand By Current (HALT Mode)		8	1	μA	STOP Mode $V_{IN} = 0\text{V}$, V_{CC} [1]
I_{AL}	Auto Latch Low Current	-10	10	5	μA	

Note:

[1] All inputs driven to 0V, V_{CC} and outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram

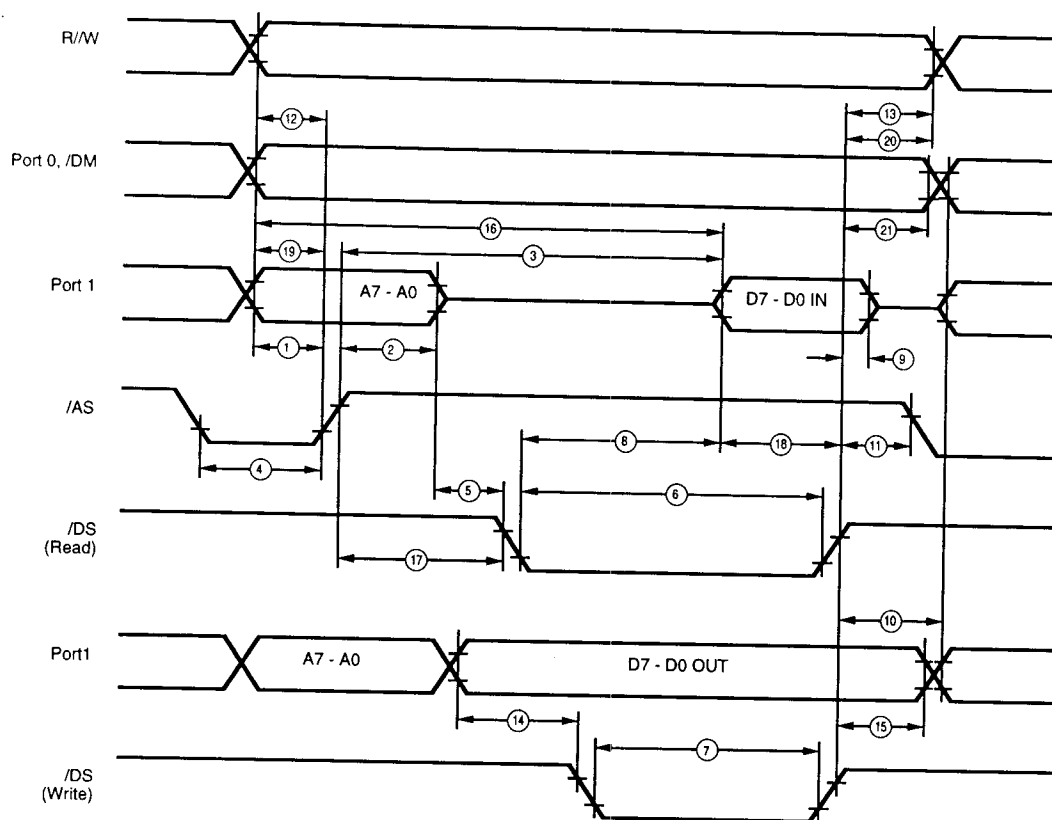


Figure 24. External I/O or Memory Read/Write Timing

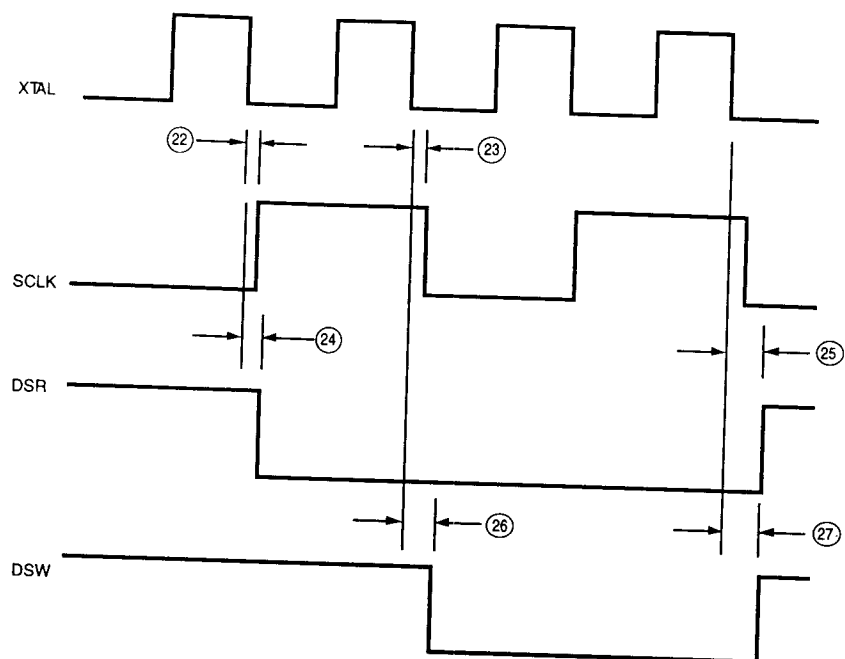


Figure 25. XTAL/SCLK To DSR and DSW Timing

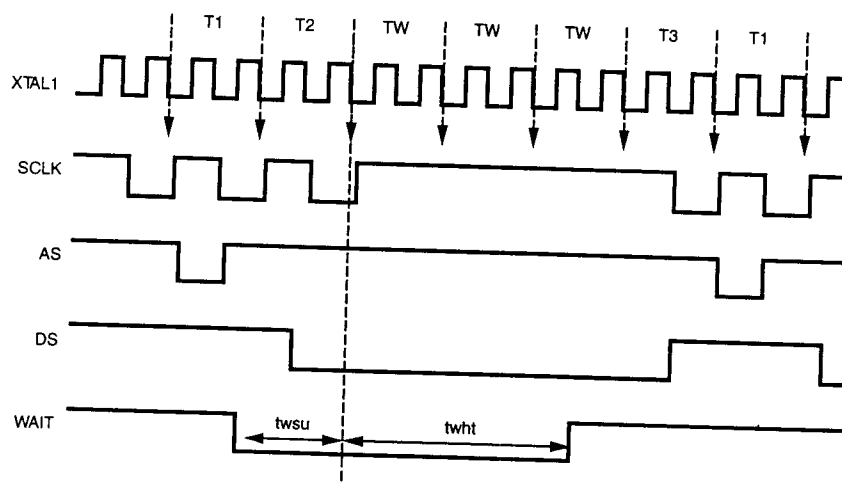


Figure 26. XTAL/SCLK To WAIT Timing
(25 MHz Device Only)

EXPANDED REGISTER FILE CONTROL REGISTERS

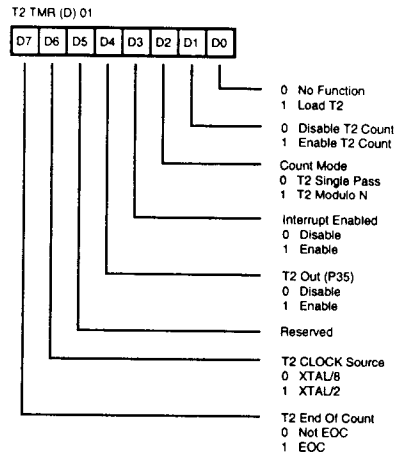


Figure 30. Timer 2 Mode Register (01H: Read/Write)

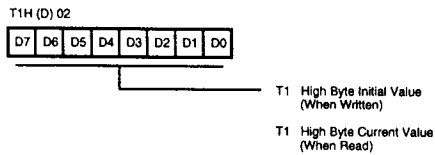


Figure 31. Counter Timer 1 Register High Byte (02H: Read/Write)

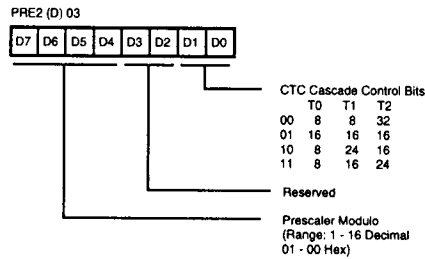


Figure 32. Prescaler 2 Register High Byte (03H: Write Only)

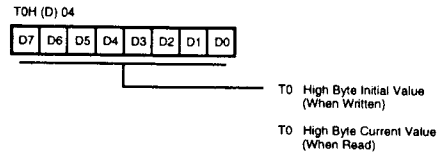


Figure 33. Counter Timer 0 Register High Byte (04H: Read/Write)

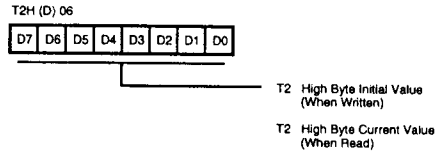


Figure 34. Counter Timer 2 Register High Byte (06H: Read/Write)

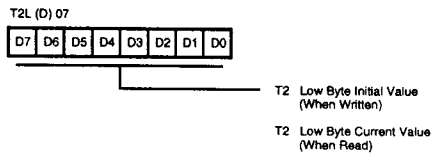


Figure 35. Counter Timer 2 Register Low Byte (07H: Read/Write)

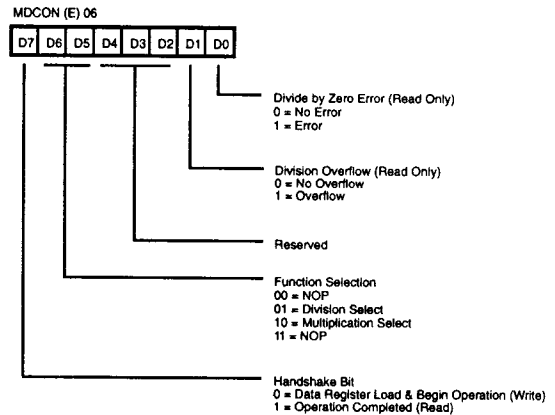


Figure 36. Multiply/Divide Control Register (MDCON)

Z8 CONTROL REGISTERS (Continued)

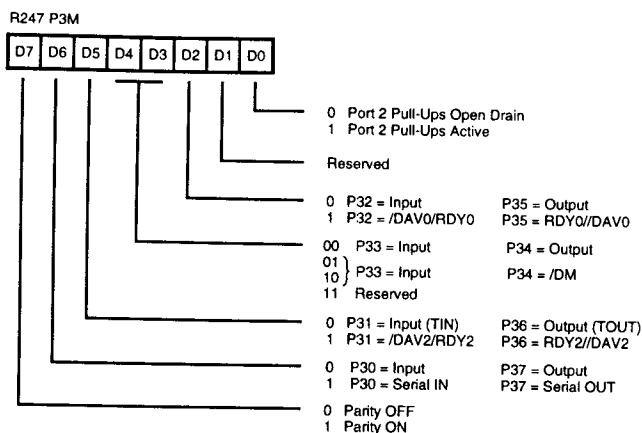


Figure 44. Port 3 Mode Register
(F7H: Write Only)

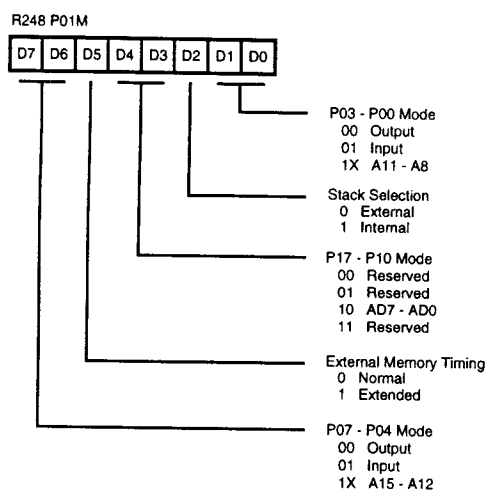


Figure 45. Ports 0 and 1 Mode Registers
(F8H: Write Only)

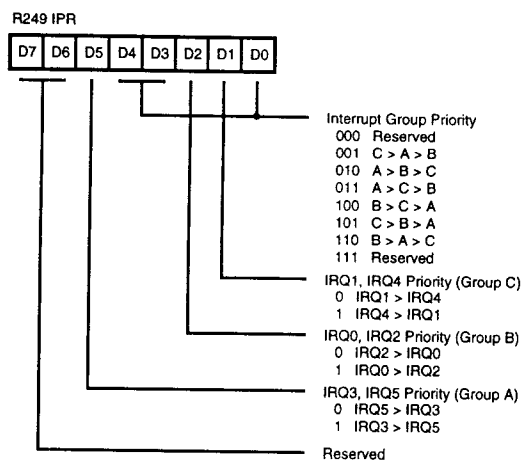


Figure 46. Interrupt Priority Register
(F9H: Write Only)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

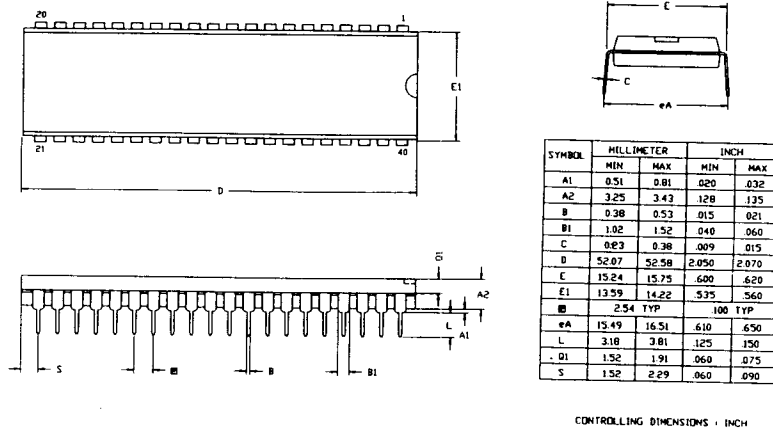
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION SUMMARY (Continued)

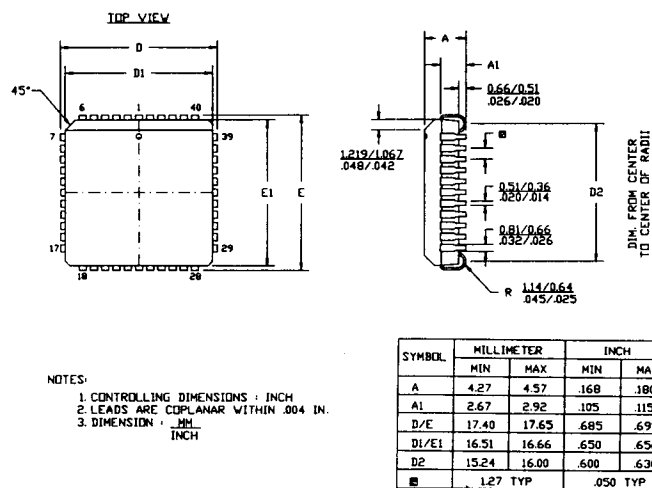
Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected							
			C	Z	S	V	D	H		
ADC dst, src dst ← dst + src + C	†	1[]	*	*	*	*	0	*		
ADD dst, src dst ← dst + src	†	0[]	*	*	*	*	0	*		
AND dst, src dst ← dst AND src	†	5[]	-	*	*	0	-	-		
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR	D6 D4	-	-	-	-	-	-		
CCF C ← NOT C		EF	*	-	-	-	-	-		
CLR dst dst ← 0	R IR	B0 B1	-	-	-	-	-	-		
COM dst dst ← NOT dst	R IR	60 61	-	*	*	0	-	-		
CP dst, src dst - src	†	A[]	*	*	*	*	-	-		
DA dst dst ← DA dst	R IR	40 41	*	*	*	X	-	-		
DEC dst dst ← dst - 1	R IR	00 01	-	*	*	*	-	-		
DECW dst dst ← dst - 1	RR IR	80 81	-	*	*	*	-	-		
DI IMR(7) ← 0		8F	-	-	-	-	-	-		
DJNZ r, dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA	rA r = 0 - F	-	-	-	-	-	-		
EI IMR(7) ← 1		9F	-	-	-	-	-	-		
HALT		7F	-	-	-	-	-	-		

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected							
			C	Z	S	V	D	H		
INC dst dst ← dst + 1	r R IR	rE r = 0 - F 20 21	-	*	*	*	-	-		
INCW dst dst ← dst + 1	RR IR	A0 A1	-	*	*	*	-	-		
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1		BF	*	*	*	*	*	*		
JP cc, dst if cc is true PC ← dst	DA IRR	cD c = 0 - F 30	-	-	-	-	-	-		
JR cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA	cB c = 0 - F	-	-	-	-	-	-		
LD dst, src dst ← src	r r R r r X r lr R R R IR IR R	lm rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-		
LDC dst, src	r lrr	C2	-	-	-	-	-	-		
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	lr lrr	C3	-	-	-	-	-	-		

PACKAGE INFORMATION



40-Pin DIP Package Diagram



44-Pin PLCC Package Diagram

ORDERING INFORMATION

Z86C93

20 MHz

44-pin PLCC
Z86C9320VSC

44-pin QFP
Z86C9320FSC

40-pin DIP
Z86C9320PSC

48-pin VQFP
Z80C9320ASC

25 MHz

44-pin PLCC
Z86C9325VSC

44-pin QFP
Z86C9325FSC

40-pin DIP
Z86C9325PSC

48-pin VQFP
Z80C9325ASC

33 MHz

44-pin PLCC
Z86C9333VSC

44-pin QFP
Z86C9333FSC

40-pin DIP
Z86C9333PSC

48-pin VQFP
Z80C9333ASC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package

V = Plastic Leaded Chip Carrier

P = Plastic Dual In Line Package

Longer Lead Time

F = Plastic Quad Flat Pack

A = Very Small Quad Flat Pack

Temperature

S = 0°C to +70°C

Speed

20 = 20 MHz

25 = 25 MHz

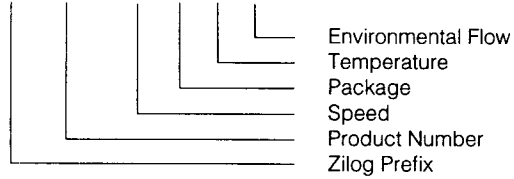
33 = 33 MHz

Environmental

C = Standard Flow

Example:

Z 86C93 33 V S C is an 86C93 33 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow



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