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Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9333asg

Z86C93

CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.

- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.

- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.

- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.

- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.

- Vectored, priority interrupts for I/O, counter/timers and UART.

- On-chip oscillator that accepts crystal or external clock drive.

- Two 16-bit counter timers with 6-bit prescalers.

- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.

- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.

- Additional emulation signals SCLK, IACK, and /SYNC are made available.

- Two low power standby modes, STOP and HALT

- Full-duplex UART

- 3.3 ± 10% volt operation at 25 MHz

- 5.0 ± 10% volt operation at 20, 25 and 33 MHz

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

GENERAL DESCRIPTION (Continued)

There are 256 registers located on-chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/ Divide Unit and Counter/Timer blocks.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

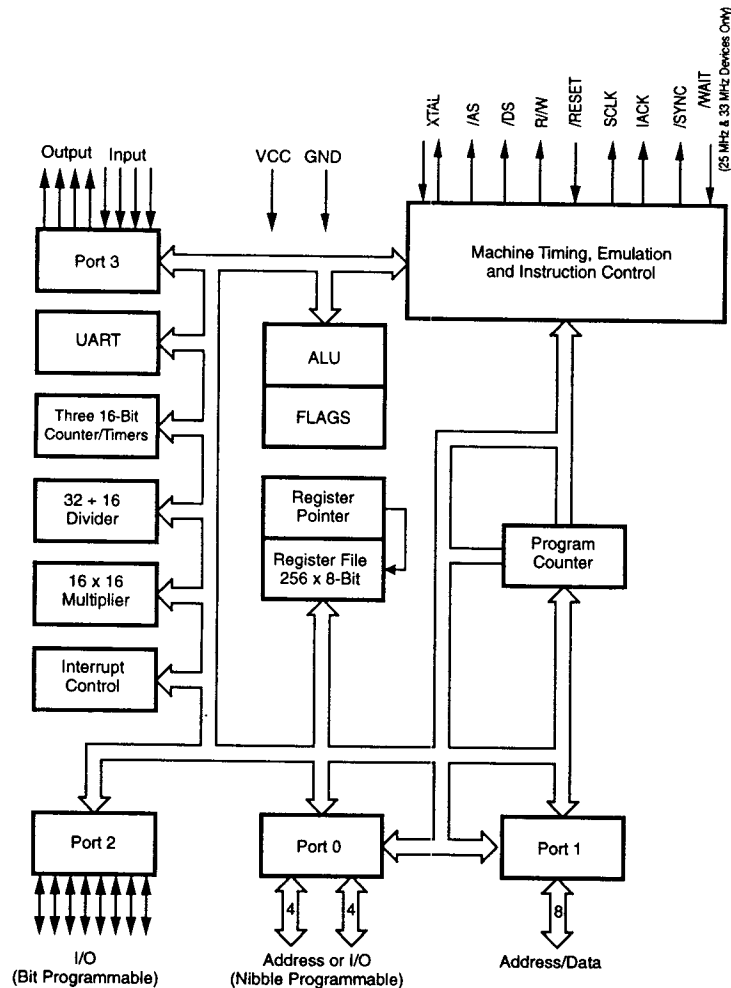| Connection	Circuit	Device
Power	V_{cc}	V_{DD}
Ground	GND	V_{SS}

Figure 1. Functional Block Diagram

PIN DESCRIPTION
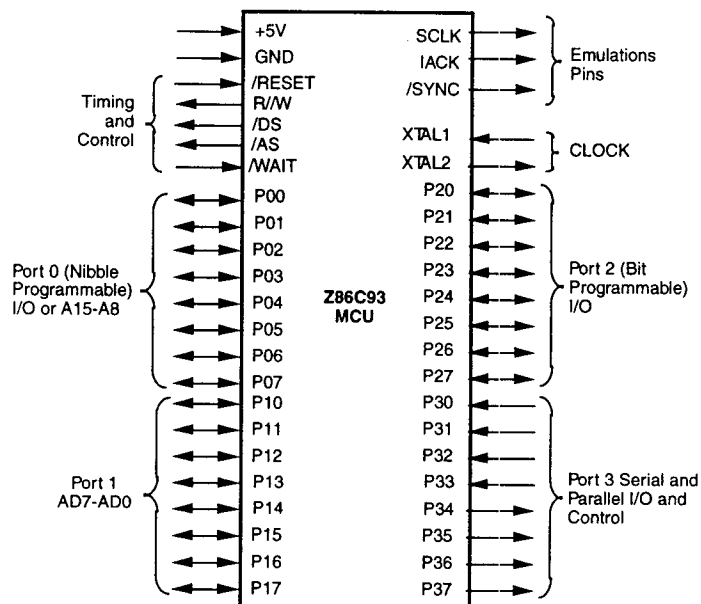
Figure 2. Pin Functions
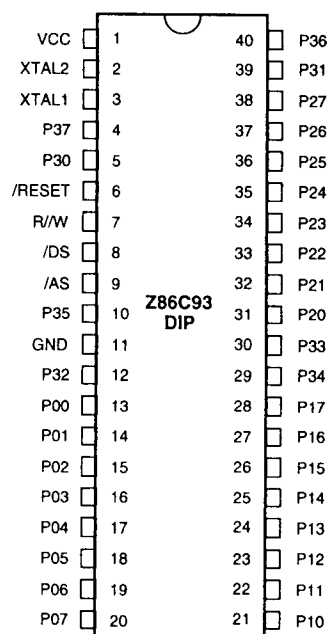
Figure 3. 40-Pin DIP

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{cc}	Power Supply	Input
2	XTAL1	Crystal, Oscillator Clock	Input
3	XTAL2	Crystal, Oscillator Clock	Output
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground, GND	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pin 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pin 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

3
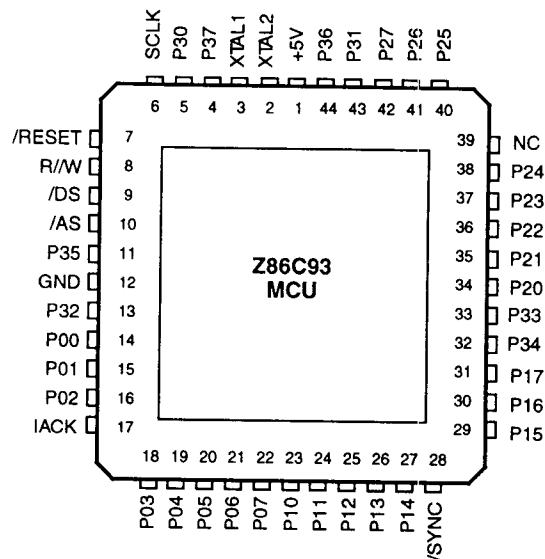
Figure 4. 44-Pin PLCC

Table 2. 44-Pin PLCC Pin Identification

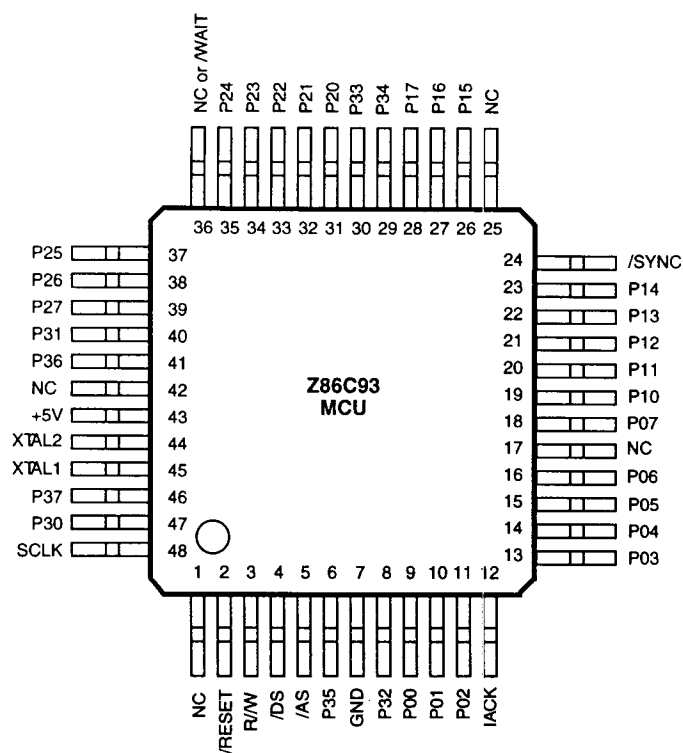| No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0 pin 0,1,2	In/Output
2	XTAL2	Crystal, Osc. Clock	Output	17	IACK	Int. Acknowledge	Output
3	XTAL1	Crystal, Osc. Clock	Input	18-22	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
5	P30	Port 3 pin 0	Input	28	/SYNC	Synchronize Pin	Output
6	SCLK	System Clock	Output	29-31	P15-P17	Port 1 pin 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3 pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected (20 MHz)	Input
11	P35	Port 3 pin 5	Output		/WAIT	WAIT (25 or 33 MHz)	Input
12	GND	Ground GND	Input	40-42	P25-P27	Port 2 pin 5,6,7	In/Output
13	P32	Port 3 pin 2	Input	43	P31	Port 3 pin 1	Input
				44	P36	Port 3 pin 6 .	Output

Figure 6. 48-Pin VQFP Package

Table 4. 48-Pin VQFP Pin Identification

No	Symbol	Function	Direction	No	Symbol	Function	Direction
1	N/C	Not Connected	Input	25	N/C	Not Connected	Input
2	/RESET	Reset	Input	26-28	P15-P17	Port 1 pin 5,6,7	In/Output
3	R/W	Read/Write	Output	29	P34	Port 3 pin 4	Output
4	/DS	Data Strobe	Output	30	P33	Port 3 pin 33	Input
5	/AS	Address Strobe	Output	31-35	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
6	P35	Port 3 pin 5	Input	36	N/C	Not Connected (20 MHz)	Input
7	GND	Ground GND	Input		/WAIT	WAIT (25 or 33 MHz)	Input
8	P32	Port 3 pin 2	Input	37-39	P25-P27	Port 2 pin 5,6,7	In/Output
9-11	P00-P02	Port 0 pin 3,4,5,6	In/Output	40	P31	Port 3 pin 1	Input
12	IACK	Int. Acknowledge	Output	41	P36	Port 3 pin 6	Output
				42	N/C	Not Connected	Input
13-16	P03-P06	Port 0 pin 3,4,5,6	In/Output	43	V_{cc}	Power Supply	Input
17	N/C	Not Connected	Input	44	XTAL2	Crystal, Osc. Clock	Output
18	P07	Port 0 pin 7	In/Output	45	XTAL1	Crystal, Osc. Clock	Input
19-23	P10-P14	Port 1 pin 0,1,2,3,4	In/Output	46	P37	Port 3 pin 7	Output
24	/SYNC	Synchronize Pin	Output	47	P30	Port 3 pin 0	Input
				48	SCLK	System Clock	Output

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).
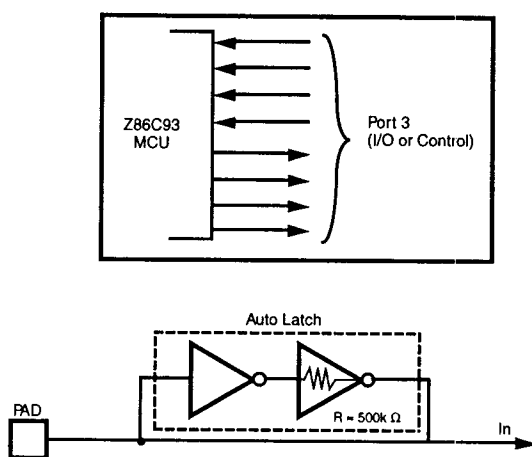

Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In		IRQ3			Serial In	
P31	In	T_{IN}	IRQ2		D/R		
P32	In		IRQ0	D/R			
P33	In		IRQ1				
P34	Out						DM
P35	Out			R/D			
P36	Out	T_{OUT}			R/D		
P37	Out					Serial Out	

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.
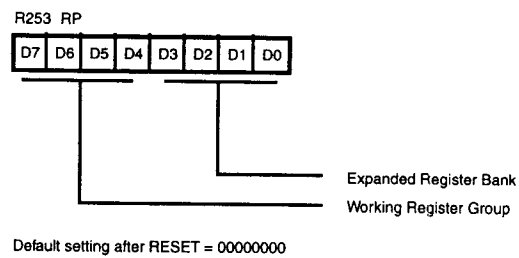
R253 RP

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Expanded Register Bank
Working Register Group

Default setting after RESET = 00000000

Figure 14. Register Pointer Register

r_7 r_6 r_5 r_4 r_3 r_2 r_1 r_0 R253

The upper nibble of the register file address
provided by the register pointer specifies
the active working-register group

R230

The lower nibble
of the register
file address
provided by the
instruction points
to the specified
register

Specified Working
Register Group

R15
R3
I/O Ports

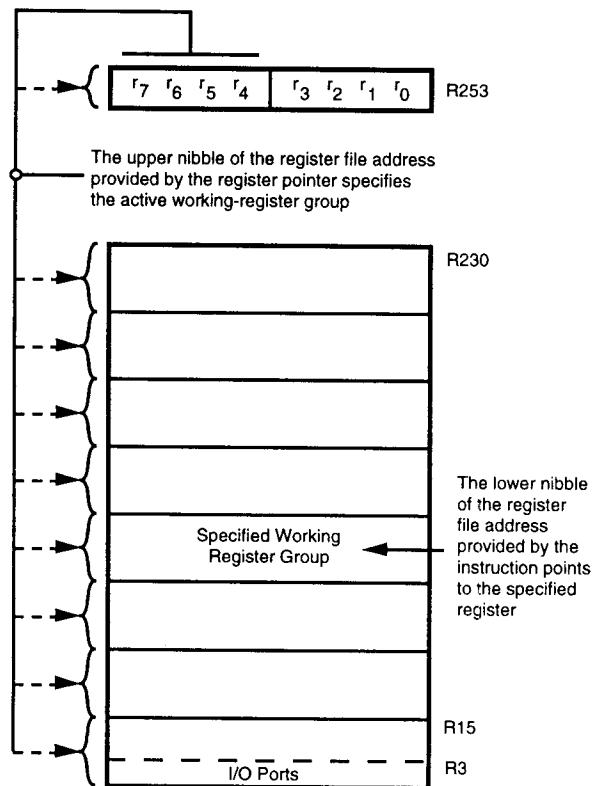**Figure 15. Register Pointer**

DIVZR. *Division by Zero* (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

> u = Undefined
> x = Irrelevant
> b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

> 1. Load multiplier and multiplicand.
> 2. Load MDCON register to start multiply operation.
> 3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

Performance of multiplication. The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7 μs. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 μs. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

Performance of division. The actual division needs 20 internal clock cycles. This translates to 2.0 μs for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 μs at 10 MHz.

Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers are cascaded by connecting the T0 output to the input of T1. Either T0 or T1 can be outputted via P36.

The following are the enhancements made to the counter/timer block on the Z86C93 (Figure 18):

■ T0 counter length is extended to 16 bits. For example, T0 now has a 6-bit prescaler and 16-bit down counter.

■ T1 counter length is extended to 16 bits. For example, T1 now has a 6-bit prescaler and 16-bit down counter.

■ A new counter/timer T2 is added. T2 has a 4-bit prescaler and a 16-bit down counter with capture register.

These three counters are cascadable as shown in Table 6. The result is that T2 may be extendable to 32 bits and T1 extendable to 24 bits. Bits 1 and 0 (CAS1 AND CAS0) of the T2 Prescaler Register (PRE2) determine the counter length.

Table 6. Counter Length Configurations

CAS 1	CAS0	T0	T1	T2
0	0	8	8	32
0	1	16	16	16
1	0	8	24	16
1	1	8	16	24

The controlling clock input to T2 is programmed to XTAL/2 or XTAL/8 (only when T2 counter length is 16 bits), which results in a resolution of 100 ns at an external XTAL clock speed of 20 MHz.

Capture Register. T2 has a 16-bit capture register associated with T2 HIGH BYTE and T2 LOW BYTE registers. The negative going transition on pin P33 enables the latching of the current T2 value (16 bits) into the capture register. The register mapping of the capture register is in Bank D (Figure 13). Note that the negative transition on P33 is capable of generating an interrupt. Also, the negative transition on P33 always latches the current T2 value into the capture register. There is no need for a control bit to enable/disable the latching; the capture register is read only.
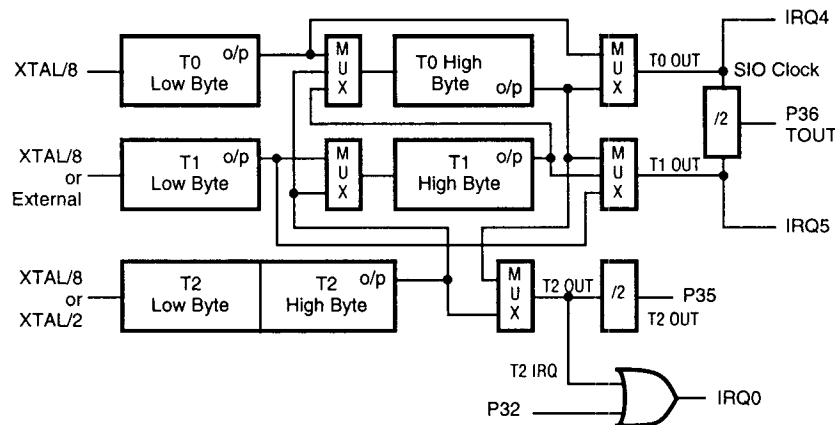

Figure 18. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Operation

Except for the programmable down counter length and clock input, T2 is identical to T0.

T0 and T1 retain all their features except that now they are extendable interims of the down-counter length.

The output of T2, under program control, goes to an output pin (P35). Also, the interrupt generated by T2 is ORed with the interrupt request generated by P32. Note that the service routine then has to poll the T2 flag bit and also clear it (Bit 7 of T2 Timer Mode Register).

On power up, T0 and T1 are configured in the 8-bit down counter length mode (to be compatible with Z86C91) and T2 is in the 32-bit mode with its output disabled (no interrupt is generated and T2 output DOES NOT go to port pin P35).

The UART uses T0 for generating the bit clock. This means, while using UART, T0 should be in 8-bit mode. So, while using the UART there are only two independent timer/counters.

The counters are configured in the following manner:

Timer	Mode	Byte
T0	8-bit	Low Byte (T0)
T0	16-bit	High Byte (T0) + Low Byte (T0)
T1	8-bit	Low Byte (T1)
T1	16-bit	High Byte (T1)+ Low Byte (T1)
T1	24-bit	High Byte (T0) + High Byte (T1) + Low Byte (T1)
T2	16-bit	High Byte (T2) + Low Byte (T2)
T2	24-bit	High Byte (T0) + High Byte (T2) + Low Byte (T2)
T2	32-bit	High Byte (T0) + High Byte (T1) + High Byte (T2) + Low Byte (T2)

Note that the T2 interrupt is logically ORed with P32 to generate IRQ0.

The T2 Timer Mode register is shown in Figure 19. Upon reaching end of count, bit 7 of this register is set to one. This bit IS NOT reset in hardware and it has to be cleared by the interrupt service routine.

T2 interrogates the state of the Count Mode Bit (D2) once it has counted down to it's zero value. T2 then makes the decision to continue counting (Module N Mode) or stop (Single Pass Mode). Observe this functionality if attempting to modify the count mode prior to the end of count bit (D7) being set.

The register map of the new CTC registers is shown in Figure 13. T0 high byte and T1 high byte are at the same relative locations as their respective low bytes, but in a different register bank.

The T2 prescaler register is shown in Figure 19. Bits 1 and 0 of this register control the various cascade modes of the counters.

T2 TMR (D) 01

| 0 | No Function |
| 1 | Load T2 |

| 0 | Disable T2 Count |
| 1 | Enable T2 Count |

Count Mode
0 T2 Single Pass
1 T2 Modulo N

Interrupt Enabled
0 Disable
1 Enable

T2 Out (P35)
0 Disable
1 Enable

Reserved

T2 CLOCK Source
0 XTAL/8
1 XTAL/2

T2 End Of Count
0 Not EOC
1 EOC
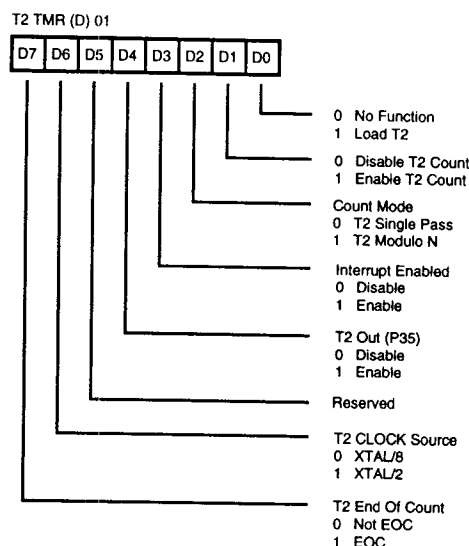
Figure 19. T2 Timer Mode Register (T2)

PRE2 (D) 03

CTC Cascade Control Bits

	T0	T1	T2
00	8	8	32
01	16	16	16
10	8	24	16
11	8	16	24

Reserved

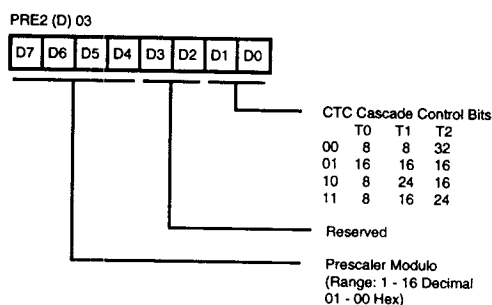Prescaler Modulo
(Range: 1 - 16 Decimal
01 - 00 Hex)

Figure 20. T2 Prescaler Register (PRE2)

Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction:

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.
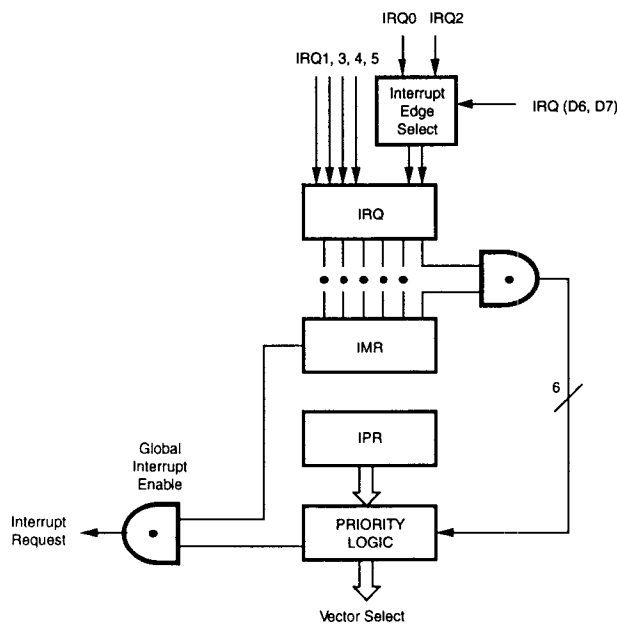

Figure 21. Interrupt Block Diagram

Power Down Modes

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. During HALT mode, /DS, /AS and R//W are HIGH. The outputs retain their preview value, and the inputs are floating.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA or less. The STOP mode is terminated by a /RESET, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	C

* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Test Load Diagram (Figure 23).
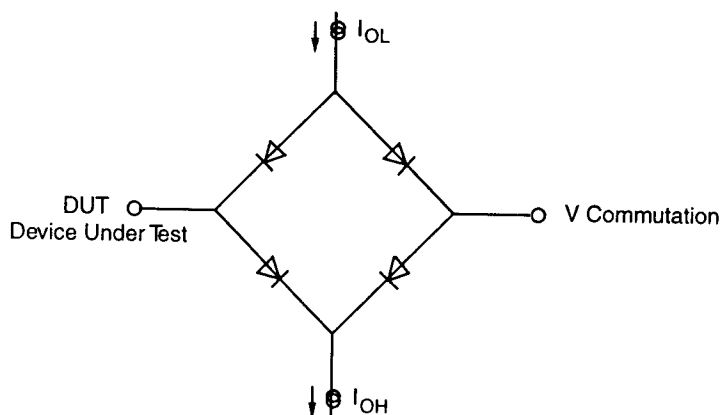

Figure 23. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS
$V_{CC} = 3.3V \pm 10\%$

Sym	Parameter	$T_A = 0°C$ to $+70°C$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	$0.8 V_{CC}$	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	$0.1 x V_{CC}$		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	$0.7 x V_{CC}$	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	$0.1 x V_{CC}$		V	
V_{OH}	Output High Voltge	1.8			V	$I_{OH} = -1.0$ mA
V_{OH}	Output High Voltge	$V_{CC} - 100mV$			V	$I_{OH} = -100$ µA
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +1.0$ mA
V_{RH}	Reset Input High Voltage	$0.8 x V_{CC}$	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	$0.1 x V_{CC}$		V	
I_{IL}	Input Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		µA	$V_{RL} = 0V$
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Stand By Current (HALT Mode)		12	8	mA	HALT Mode V_{IN}=0V, V_{CC} @ 25 MHz [1]
I_{CC2}	Stand By Current (HALT Mode)		8	1	µA	STOP Mode V_{IN}=0V, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	-10	10	5	µA	

Note:
[1] All inputs driven to 0V, V_{CC} and outputs floating.

AC CHARACTERISTICS
External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

No	Sym	Parameter	$T_A = 0°C$ to $+70°C$ 33 MHz Min	33 MHz Max	25 MHz Min	25 MHz Max	20 MHz Min	20 MHz Max	Typical V_{cc}=5.0V @ 25°C	Units
1	TdA(AS)	Address Valid To /AS Rise Delay	13		22		26			ns
2	TdAS(A)	/AS Rise To Address Hold Time	20		25		28			ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		90		130		160		ns
4	TwAS	/AS Low Width	20		28		36			ns
5	TdAZ(DSR)	Address Float To /DS (Read)	0		0		0			ns
6	TwDSR	/DS (Read) Low Width	65		100		130			ns
7	TwDSW	/DS (Write) Low Width	40		65		75			ns
8	TdDSR(DI)	/DS (Read) To Data in Req'd Valid Delay		30		78		100		ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0			ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		34		40			ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36			ns
12	TdR/W(AS)	R/W To /AS Rise Delay	12		26		32			ns
13	TdDS(R/W)	/DS Rise To R/W Valid Delay	12		30		36			ns
14	TdDO(DSW)	Data Out To /DS (Write) Delay	12		34		40			ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40			ns
16	TdA(DI)	Address To Data In Req'd Valid Delay		110		160		200		ns
17	TdAS(DSR)	/AS Rise To /DS (Read) Delay	20		40		48			ns
18	TaDI(DSR)	Data In Set-up Time To /DS Rise Read	16		30		36			ns
19	TdDM(AS)	/DM To /AS Rise Delay	10		22		26			ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay							34*	ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time							34*	ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising							20*	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling							23*	ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling							29*	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising							29*	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling							29*	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising							29*	ns
28	TsW(XT)	Wait Set-up Time							10*	ns
29	ThW(XT)	Wait Hold Time							15*	ns
30	TwW	Wait Width (One Wait Time)							25*	ns

Notes:
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
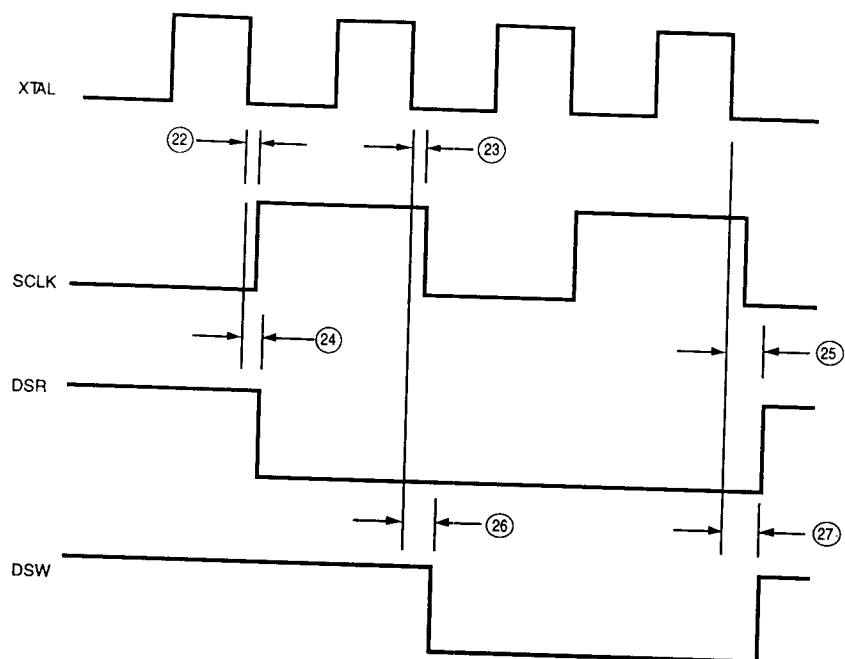* Preliminary value to be characterized.
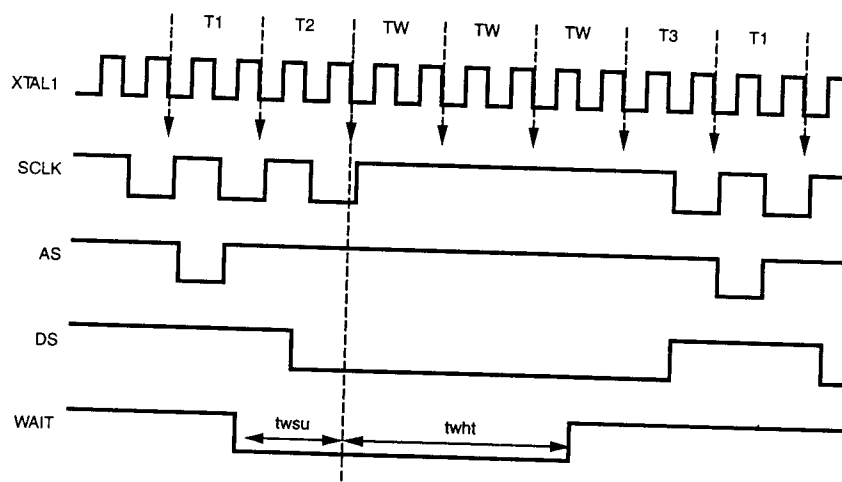
Figure 25. XTAL/SCLK To DSR and DSW Timing

Figure 26. XTAL/SCLK To WAIT Timing
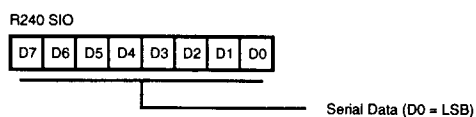**(25 MHz Device Only)**

Z8 CONTROL REGISTERS

R240 SIO

D7	D6	D5	D4	D3	D2	D1	D0

Serial Data (D0 = LSB)

**Figure 37. Serial I/O Register
(F0H: Read/Write)**

R241 TMR

D7	D6	D5	D4	D3	D2	D1	D0

0 No Function
1 Load T0

0 Disable T0 Count
1 Enable T0 Count

0 No Function
1 Load T1

0 Disable T1 Count
1 Enable T1 Count

TIN Modes
00 External Clock Input
01 Gate Input
10 Trigger Input
(Non-retriggerable)
11 Trigger Input
(Retriggerable)

TOUT Modes
00 Not Used
01 T0 Out
10 T1 Out
11 Internal Clock Out
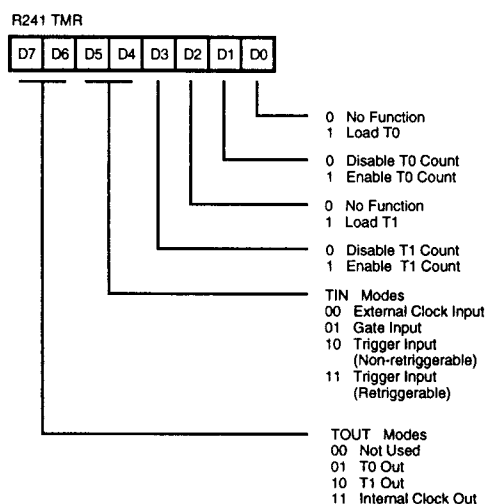
**Figure 38. Timer Mode Register
(F1H: Read/Write)**

R242 T1

D7	D6	D5	D4	D3	D2	D1	D0

T1 Low Byte Initial Value
(When Written)

T1 Low Byte Current Value
(When Read)
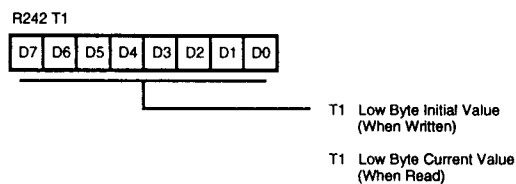
**Figure 39. Counter/Timer 1 Register
(F2H: Read/Write)**

R243 PRE1

D7	D6	D5	D4	D3	D2	D1	D0

Count Mode
0 T1 Single Pass
1 T1 Modulo N

Clock Source
1 T1 Internal
0 T1 External Timing Input
(TIN) Mode

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
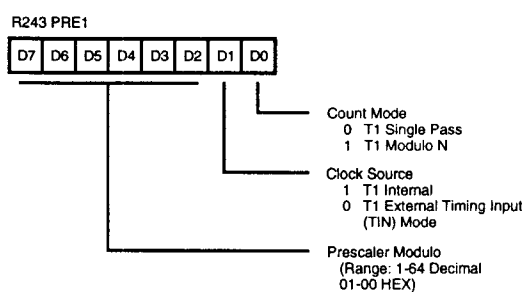
**Figure 40. Prescaler 1 Register
(F3H: Write Only)**

R244 T0

D7	D6	D5	D4	D3	D2	D1	D0

T0 Low Byte Initial Value
(When Written)

T0 Low Byte Current Value
(When Read)
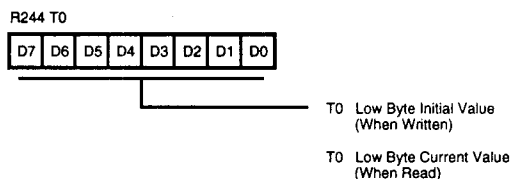
**Figure 41. Counter/Timer 0 Register
(F4H: Read/Write)**

R245 PRE0

D7	D6	D5	D4	D3	D2	D1	D0

Count Mode
0 T0 Single Pass
1 T0 Modulo N

Reserved

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
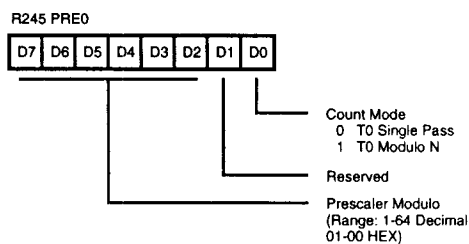
**Figure 42. Prescaler 0 Register
(F5H: Write Only)**

R246 P2M

D7	D6	D5	D4	D3	D2	D1	D0

P20 - P27 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input
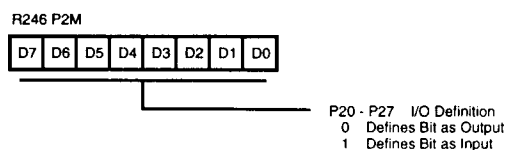
**Figure 43. Port 2 Mode Register
(F6H: Write Only)**

R250 IRQ

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = P30 Input
IRQ4 = T0
IRQ5 = T1

IRQ Edge Triggering

00 P21 ↓   P32 ↓
01 P31 ↓   P32 ↑
10 P31 ↑   P32 ↓
11 P31 ↕   P32 ↕
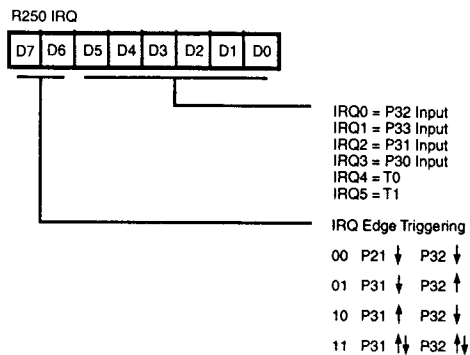
**Figure 47. Interrupt Request Register
(FAH: Read/Write)**

R251 IMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1 Enables IRQ0-IRQ5
(D0 = IRQ0)

Reserved

1 Enables Interrupts

**Figure 48. Interrupt Mask Register
(FBH: Read/Write)**

R252 FLAGS

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

User Flag F1
User Flag F2
Half Carry Flag
Decimal Adjust Flag
Overflow Flag
Sign Flag
Zero Flag
Carry Flag

**Figure 49. Flag Register
(FCH: Read/Write)**

R253 RP

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Expanded Register File
Working Register Pointer

**Figure 50. Register Pointer
(FDH: Read/Write)**

R254 SPH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stack Pointer Upper
Byte (SP8 - SP15)
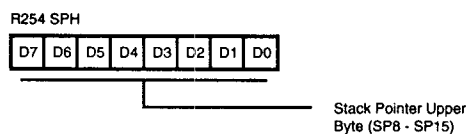
**Figure 51. Stack Pointer High
(FEH: Read/Write)**

R255 SPL

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stack Pointer Lower
Byte (SP0 - SP7)

**Figure 52. Stack Pointer Low
(FFH: Read/Write)**

INSTRUCTION FORMATS

```
        OPC
```
CCF, DI, EI, IRET, NOP,
RCF, RET, SCF

```
  dst  |  OPC
```

One-Byte Instructions

```
  OPC  |  MODE
      dst/src        OR    1 1 1 0  |  dst/src
```
CLR, CPL, DA, DEC,
DECW, INC, INCW,
POP, PUSH, RL, RLC,
RR, RRC, SRA, SWAP

```
        OPC
        dst            OR    1 1 1 0  |  dst
```
JP, CALL (Indirect)

```
        OPC
       VALUE
```
SRP

```
  OPC  |  MODE
  dst  |  src
```
ADC, ADD, AND, CP,
OR, SBC, SUB, TCM,
TM, XOR

```
  MODE  |  OPC
 dst/src | src/dst
```
LD, LDE, LDEI,
LDC, LDCI

```
 dst/src |  OPC
      src/dst         OR    1 1 1 0  |  src
```
LD

```
  dst  |  OPC
       VALUE
```
LD

```
 dst/CC |  OPC
        RA
```
DJNZ, JR

```
        FFH
  6FH  |  7FH
```
STOP/HALT

Two-Byte Instructions

```
  OPC  |  MODE
        src            OR    1 1 1 0  |  src
        dst            OR    1 1 1 0  |  dst
```
ADC, ADD, AND, CP,
LD, OR, SBC, SUB,
TCM, TM, XOR

```
  OPC  |  MODE
        dst            OR    1 1 1 0  |  dst
       VALUE
```
ADC, ADD, AND, CP,
LD, OR, SBC, SUB,
TCM, TM, XOR

```
  MODE  |  OPC
        src            OR    1 1 1 0  |  src
        dst            OR    1 1 1 0  |  dst
```
LD

```
  MODE  |  OPC
 dst/src |  x
      ADDRESS
```
LD

```
   cc  |  OPC
        DAU
        DAL
```
JP

```
        OPC
        DAU
        DAL
```
CALL

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

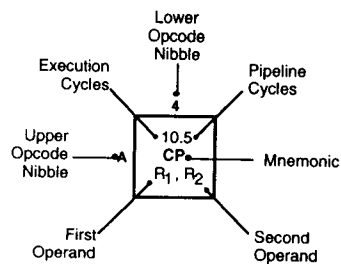indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI Ir1, Irr2												6.1 DI
9	6.5 RL R1	6.5 RL IR1	12.0 LDE r2, Irr1	18.0 LDEI Ir2, Irr1												6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2				10.5 LD r1,x,R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r2, Irr1	18.0 LDCI Ir2, Irr1	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP

Bytes per Instruction

2	3	2	3	1

Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand,
Second Operand

Note: The blank areas are not defined.

* 2-byte instruction appears
as a 3-byte instruction

Key diagram:
Lower Opcode Nibble / Execution Cycles / Pipeline Cycles / Upper Opcode Nibble / Mnemonic / First Operand / Second Operand

```
            4
    A   10.5  CP
        R1, R2
```

Notes: