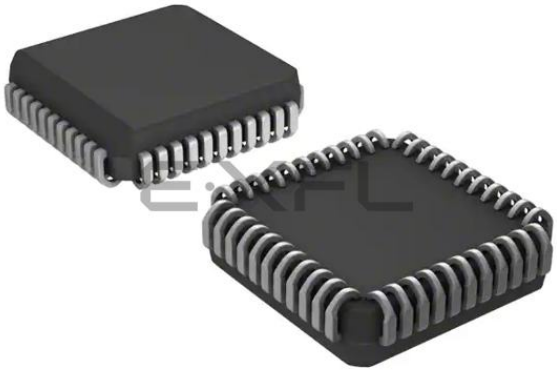

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	24
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9333vsc00tr

ZiLOG

PRODUCT SPECIFICATION

Z86C93

CMOS Z8® MULTIPLY/DIVIDE MICROCONTROLLER

FEATURES

- Complete microcontroller, up to 24 I/O lines, and up to 64 Kbytes of addressable external space each for program and data memory.
- 16-bit x 16-bit hardwired multiplier with 32-bit product in 17 clock cycles.
- 32-bit x 16-bit hardwired divider with 16-bit quotient and 16-bit remainder in 20 clock cycles.
- 256-byte register file, including 236 general-purpose registers, up to three I/O port registers and 16 status and control registers.
- 17-byte Expanded Register File, including two general-purpose registers and 15 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Two 16-bit counter timers with 6-bit prescalers.
- Third 16-bit counter/timer with 4-bit prescaler, one capture register and a fast decrement mode.
- Register Pointer for short, fast instructions that can access any one of the sixteen working register groups.
- Additional emulation signals SCLK, IACK, and /SYNC are made available.
- Two low power standby modes, STOP and HALT
- Full-duplex UART
- 3.3 ± 10% volt operation at 25 MHz
- 5.0 ± 10% volt operation at 20, 25 and 33 MHz

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier and 32-bit/16-bit divider and three 16-bit counter timers (Figure 1). A capture register and a fast decrement mode is also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP and 48-pin VQFP (Figures 2, 3, 4, 5 and 6). Besides the four additional signals (SCLK, IACK, /SYNC and /WAIT), the Z86C93 is compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

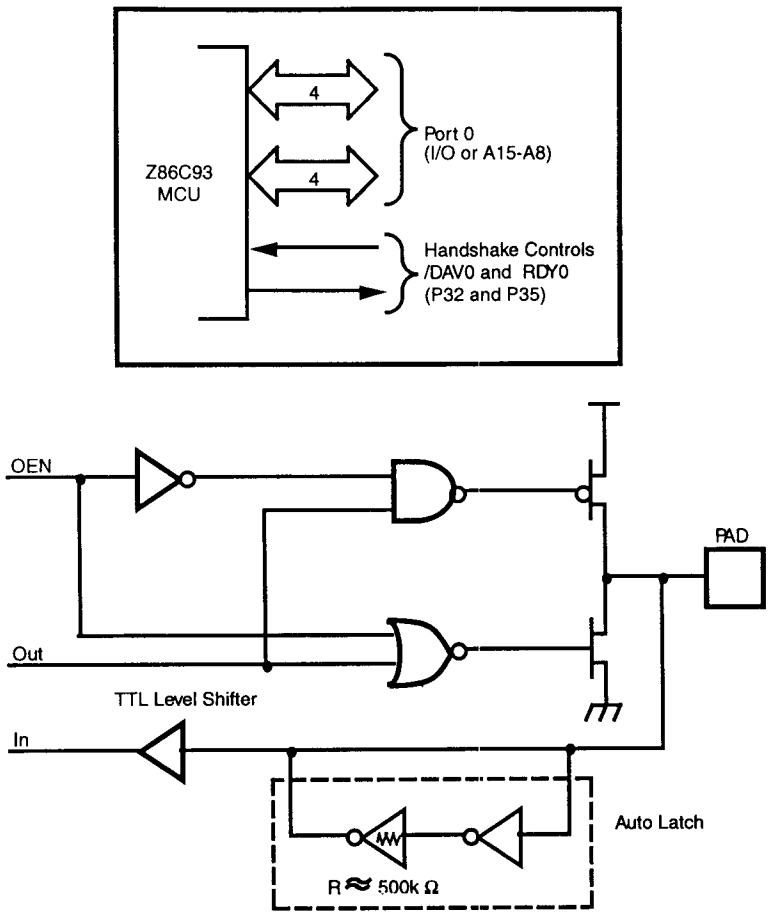


Figure 7. Port 0 Configuration

Port 2. (P20-P27). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 9).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

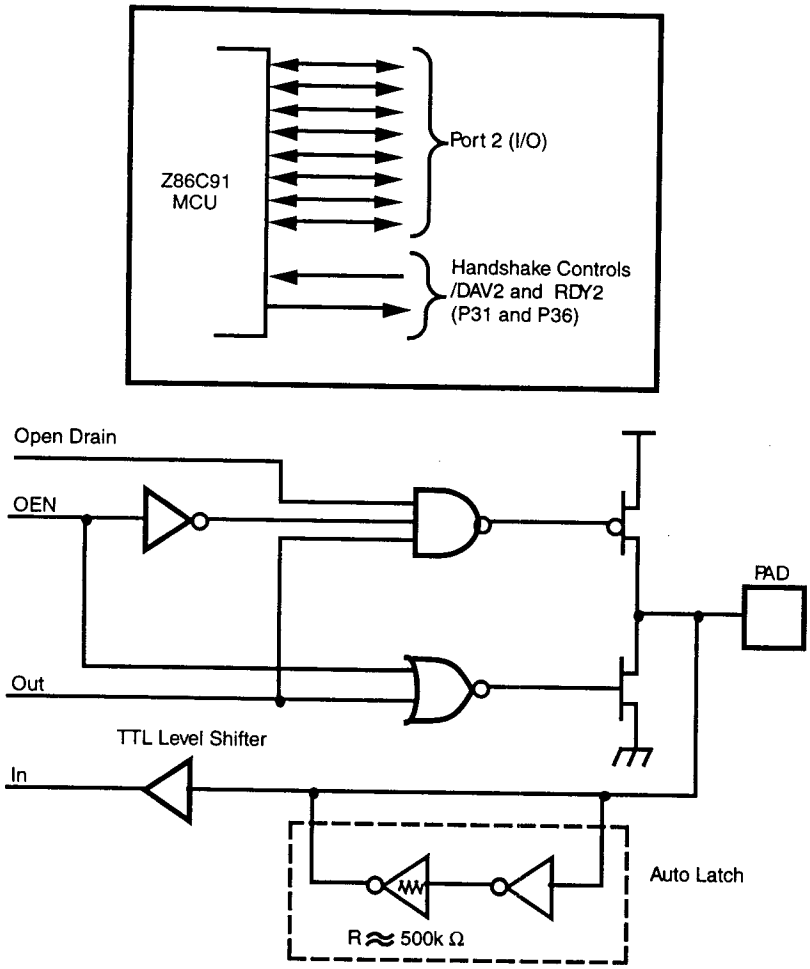


Figure 9. Port 2 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output ports. These eight I/O lines have four fixed (P30-P33) input and four fixed (P34-P37) output ports. Port 3 pins P30 and P37 when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 10 and Table 5).

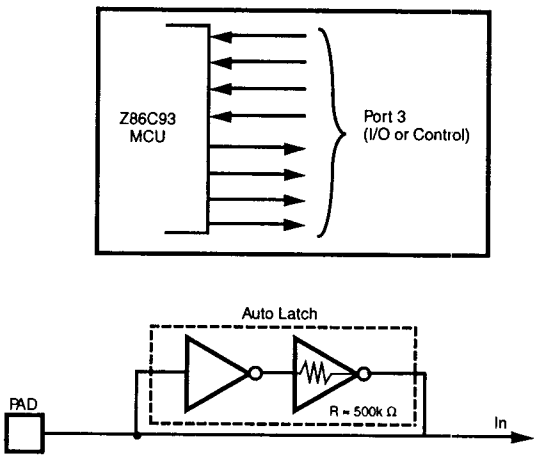


Figure 10. Port 3 Configuration

Table 5. Port 3 Pin Assignments

Pin #	I/O	CTC1	Int.	P0HS	P2HS	UART	Ext.
P30	In		IRQ3			Serial In	
P31	In	T_{IN}	IRQ2		D/R		
P32	In		IRQ0	D/R			
P33	In		IRQ1				
P34	Out						DM
P35	Out			R/D			
P36	Out	T_{OUT}			R/D		
P37	Out					Serial Out	

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Port 3 lines P30 and P37 can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer 0.

The Z86C93 automatically adds a start bit and two stop bits to transmitted data (Figure 10). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

The Auto Latch on Port 3 puts a valid CMOS level on all CMOS inputs that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level rather than a floating node reduces excessive supply current flow in the input buffer.

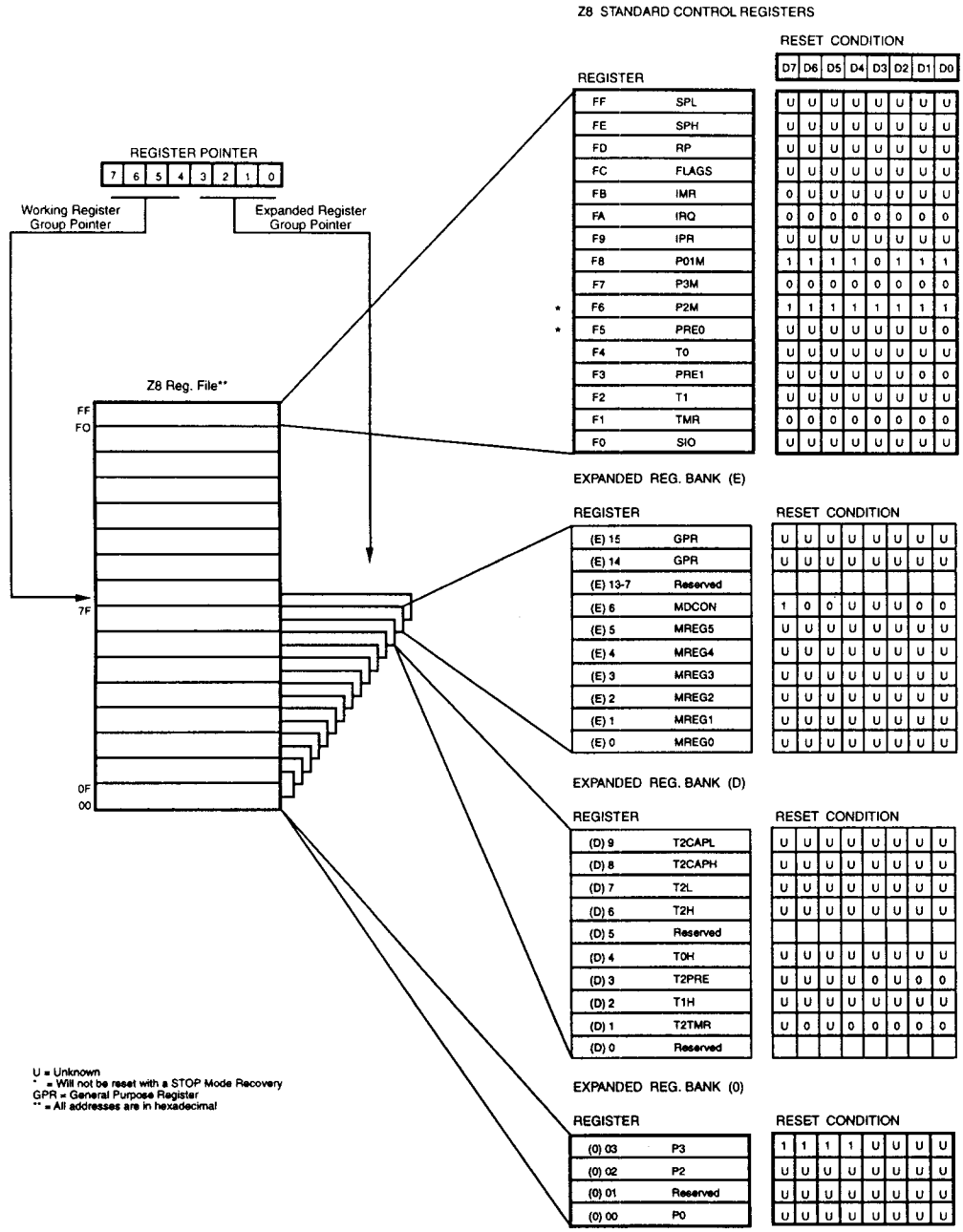


Figure 13. Register File

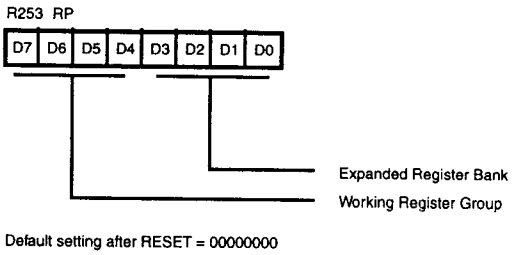


Figure 14. Register Pointer Register

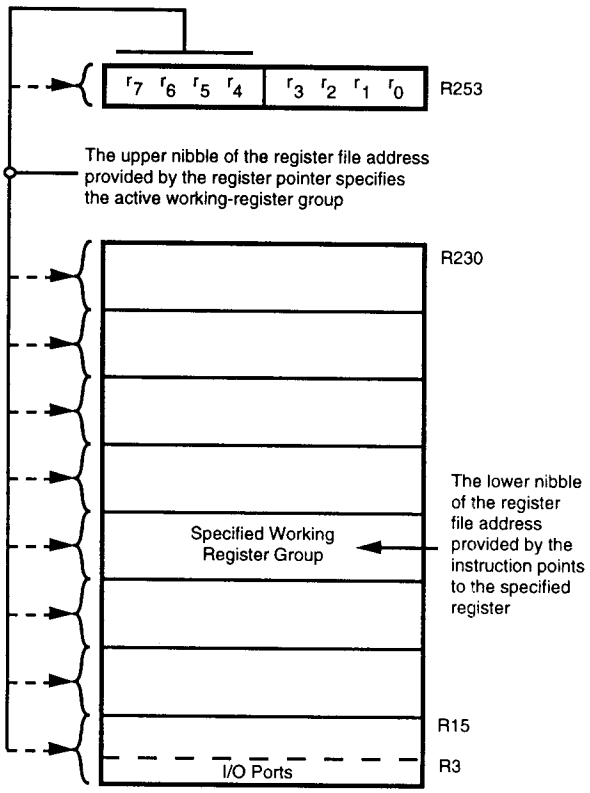


Figure 15. Register Pointer

DIVZR. *Division by Zero* (D0). When set to 1, this indicates an error of division by 0. This bit is read only.

Example:

Upon reset, the status of the MDCON register is 100uuu00b (D7 to D0).

u = Undefined
x = Irrelevant
b = Binary

If multiplication operation is desired, the MDCON register is set to 010xxxxxb.

If the MDCON register is READ during multiplication, it would have a value of 000uuu00b.

Upon completion of multiplication, the result of the MDCON register is 100uuu00b.

If division operation is desired, the MDCON register is set to 001xxxxxb.

During division operation, the register would contain 000uu??b (? - value depends on the DIVIDEND, DIVISOR).

Upon completion of division operation, the MDCON register contains 100uuu??b.

Note that once the multiplication/division operation starts, all data registers (MREG5 through MREG0) are write-protected and so are the writable bits of the MDCON register. The write protection is released once the math unit operation is complete. However, the registers may be read at any time.

A multiplication sequence would look like:

1. Load multiplier and multiplicand.
2. Load MDCON register to start multiply operation.
3. Wait for the DONE bit of the MDCON register to be set to 1 and then read results.

Note that while the multiply/divide operation is in progress, the programmer can use the Z8 to do other things. Also, since the multiplication/division takes a fixed number of cycles, he can start reading the results before the DONE bit is set.

During a division operation, the error flag bits are set at the beginning of the division operation which means the flag bits can be checked by the Z8 while the division operation is being done.

The two general purpose registers can be used as scratch pad registers or as external data memory address pointers during an LDE instruction. MREG0 through MREG5, if not used for multiplication or division, can be used as general purpose registers.

Performance of multiplication. The actual multiplication takes 17 internal clock cycles. It is expected that the chip would run at a 10 MHz internal clock frequency (external clock divided by two). This results in an actual multiplication time (16-bit x 16-bit) of 1.7 µs. If the time to load operands and read results is included:

Number of internal clock cycles to load 5 registers: 30
Number of internal clock cycles to read 4 registers: 24

The total internal clock cycles to perform a multiplication is 71. This results in a net multiplication time of 7.1 µs. Note that this would be the worst case. This assumes that all of the operands are loaded from the external world as opposed to some of the operands being already in place as a result of a previous operation whose destination register is one of the math unit registers.

Performance of division. The actual division needs 20 internal clock cycles. This translates to 2.0 µs for the actual division at 10 MHz (internal clock speed). If the time to load operands and read results is included:

Number of internal clock cycles to load operands: 42
Number of internal clock cycles to read results: 24

The total internal clock cycles to perform a division is 86. This translates to 8.6 µs at 10 MHz.

Counter/Timers

This section describes the enhanced features of the counter/timers (CTC) on the Z86C93. It contains the register mapping of CTC registers and the bit functions of the newly added Timer2 control register.

In a standard Z8, there are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only.

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1), is generated.

Interrupts

The Z86C93 has six different interrupts from nine different sources. The interrupts are maskable and prioritized. The nine sources are divided as follow: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and three in the counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C93 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

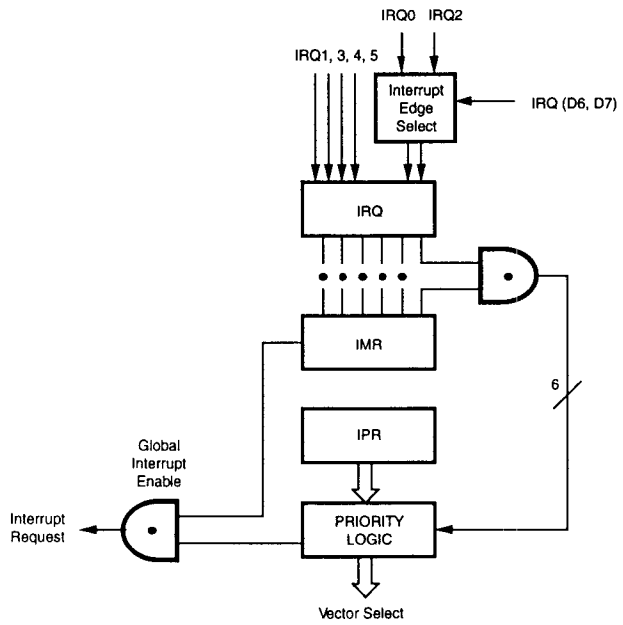


Figure 21. Interrupt Block Diagram

Table 7. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	/DAV 0, P32, T2	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ 1,	P33	2, 3	External (P33), Fall Edge Triggered
IRQ 2	/DAV 2, P31, T_{IN}	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ 3	P30, Serial In	6, 7	External (P30), Fall Edge Triggered
IRQ 4	T0, Serial Out	8, 9	Internal
IRQ 5	TI	10, 11	Internal

Clock

The Z86C93 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The external clock levels are not TTL. The crystal should be AT cut, 1 MHz to 25 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF<CL<100 pF) from each pin to ground (Figure 20).

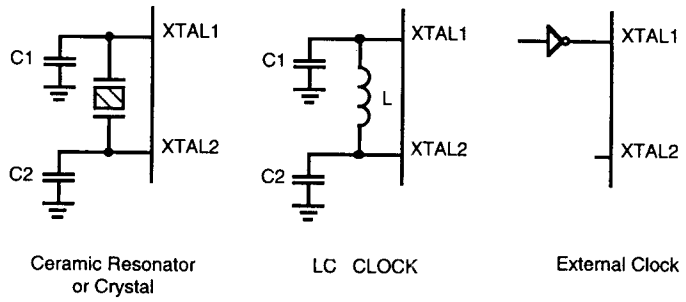


Figure 22. Oscillator Configuration

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	0.8 V_{CC}	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.1xV_{CC}		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7xV_{CC}	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.1xV_{CC}		V	
V_{OH}	Output High Voltge	1.8			V	I_{OH} = -1.0 mA
V_{OH}	Output High Voltge	V_{CC} - 100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +1.0 mA
V_{RH}	Reset Input High Voltage	0.8xV_{CC}	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.1xV_{CC}		V	
I_{IL}	Input Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		µA	V_{RL} = 0V
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Stand By Current (HALT Mode)		12	8	mA	HALT Mode V_{IN}=0V, V_{CC} @ 25 MHz [1]
I_{CC2}	Stand By Current (HALT Mode)		8	1	µA	STOP Mode V_{IN}=0V, V_{CC} [1]
I_{ALL}	Auto Latch Low Current	-10	10	5	µA	

Note:

[1] All inputs driven to 0V, V_{CC} and outputs floating.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltge	2.4			V	I_{OH}=-2.0 mA
V_{OH}	Output High Voltage	V_{CC} -100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +5 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.8		V	
I_{IL}	Input Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	-2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		-80		µA	V_{RL} = 0V
I_{CC}	Supply Current		55	35	mA	@ 33 MHz [1]
			40	25	mA	@ 25 MHz [1]
			30	20	mA	@ 20 MHz [1]
I_{CC1}	Standby Current (HALT Mode)		15	9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 25 MHz [1]
			20	15		HALT Mode V_{IN} = 0V, V_{CC} @ 33 MHz [1]
			12	7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 20 MHz [1]
I_{CC2}	Standby Current (STOP Mode)		10	1	µA	STOP Mode V_{IN} = 0V, V_{CC} [1]
I_{AL}	Auto Latch Current	-16	16	5	µA	

Note:

[1] All inputs driven to 0V, or V_{cc} and outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

			T_A = 0°C to +70°C							
			33 MHz		25 MHz		20 MHz		Typical	
No	Sym	Parameter	Min	Max	Min	Max	Min	Max	V_{cc}=5.0V @ 25°C	Units
1	TdA(AS)	Address Valid To /AS Rise Delay	13		22		26			ns
2	TdAS(A)	/AS Rise To Address Hold Time	20		25		28			ns
3	TdAS(DI)	/AS Rise Data In Req'd Valid Delay		90		130		160		ns
4	TwAS	/AS Low Width	20		28		36			ns
5	TdAZ(DSR)	Address Float To /DS (Read)	0		0		0			ns
6	TwDSR	/DS (Read) Low Width	65		100		130			ns
7	TwDSW	/DS (Write) Low Width	40		65		75			ns
8	TdDSR(DI)	/DS (Read) To Data in Req'd Valid Delay		30		78		100		ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0			ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		34		40			ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36			ns
12	TdR/W(AS)	R/W To /AS Rise Delay	12		26		32			ns
13	TdDS(R/W)	/DS Rise To R/W Valid Delay	12		30		36			ns
14	TdDO(DSW)	Data Out To /DS (Write) Delay	12		34		40			ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40			ns
16	TdA(DI)	Address To Data In Req'd Valid Delay		110		160		200		ns
17	TdAS(DSR)	/AS Rise To /DS (Read) Delay	20		40		48			ns
18	TaDI(DSR)	Data In Set-up Time To /DS Rise Read	16		30		36			ns
19	TdDM(AS)	/DM To /AS Rise Delay	10		22		26			ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay							34*	ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time							34*	ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising							20*	ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling							23*	ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling							29*	ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising							29*	ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling							29*	ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising							29*	ns
28	TsW(XT)	Wait Set-up Time							10*	ns
29	ThW(XT)	Wait Hold Time							15*	ns
30	TwW	Wait Width (One Wait Time)							25*	ns

Notes:
When using extended memory timing add 2 TpC.
Timing numbers given are for minimum TpC.
* Preliminary value to be characterized.

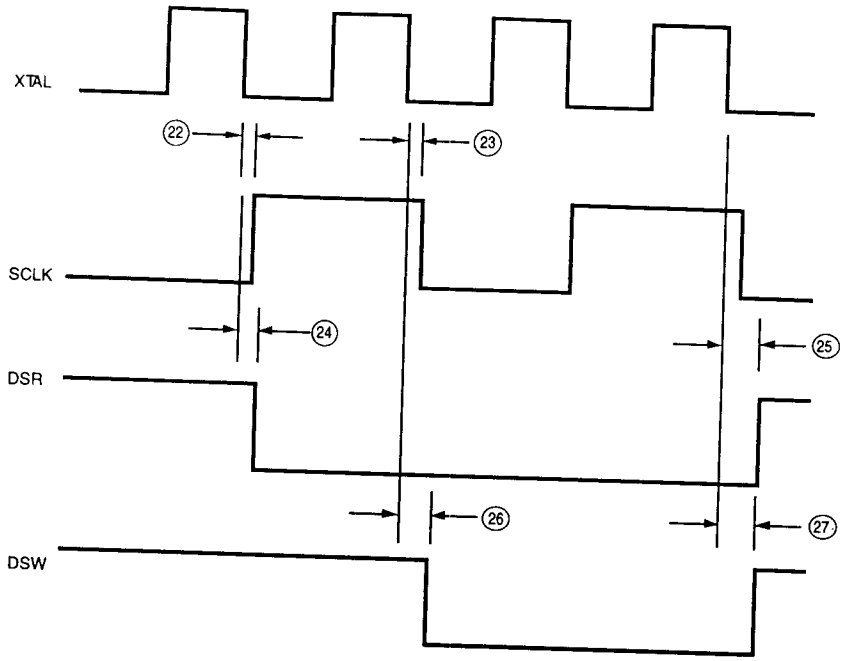


Figure 25. XTAL/SCLK To DSR and DSW Timing

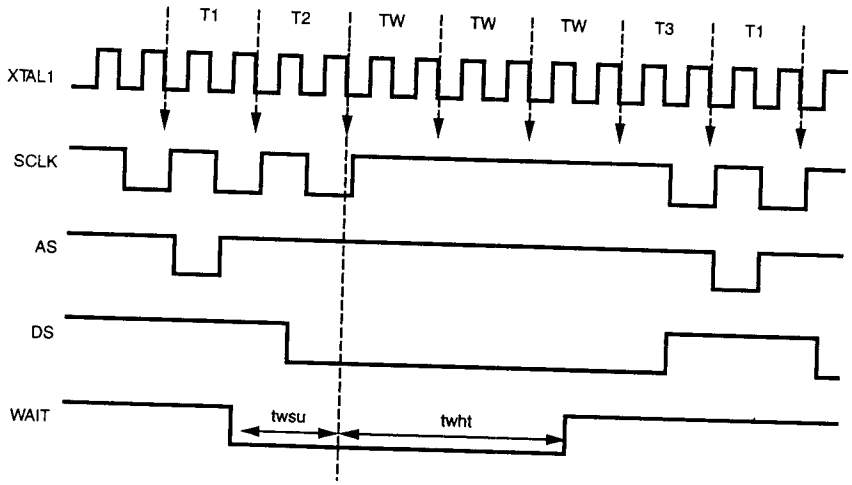


Figure 26. XTAL/SCLK To WAIT Timing (25 MHz Device Only)

AC CHARACTERISTICS
Additional Timing Diagram

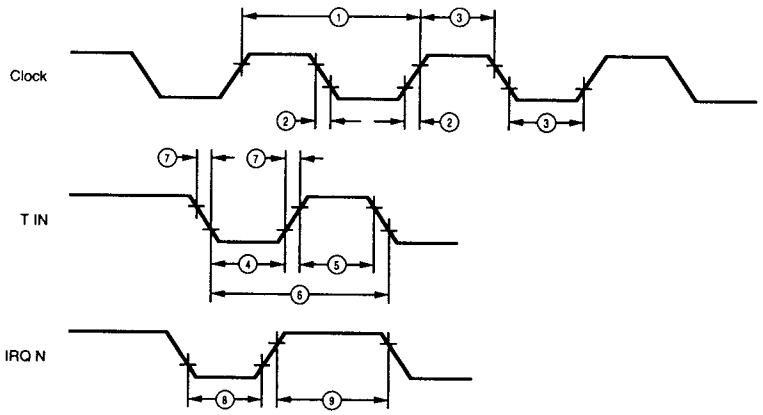


Figure 27. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	T_A = 0°C to +70° C						Units	Notes
			33 MHz		24 MHz		20 MHz			
			Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	30	1000	42	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Imput Rise & Fall Times		5		10		10	ns	[1]
3	TwC	Input Clock Width	10		11		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request via Port 3.
[4] Interrupt request via Port 3 (P31-P33)`.
[5] Interrupt request via Port 30.

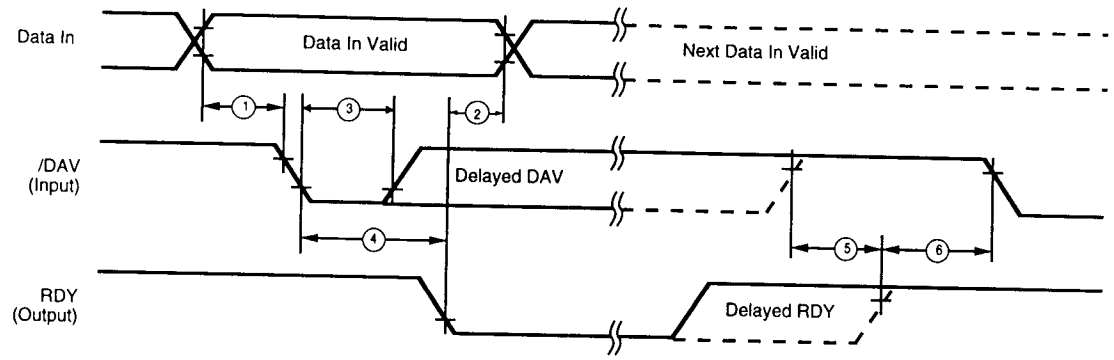


Figure 28. Input Handshake Timing

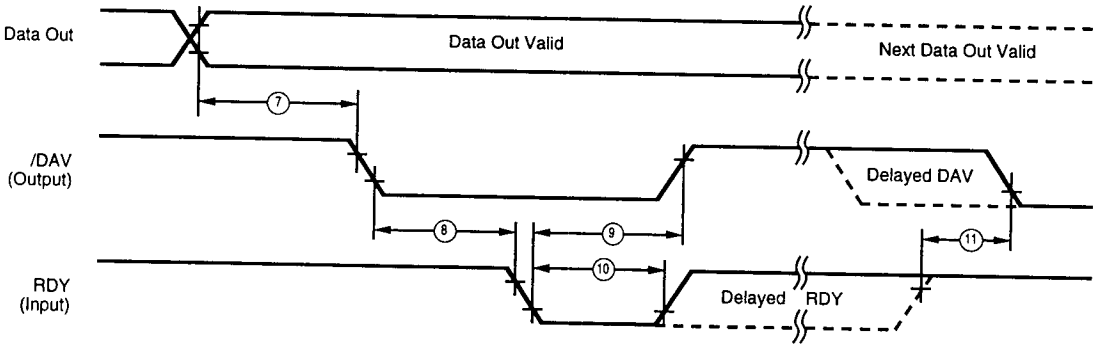


Figure 29. Output Handshake Timing

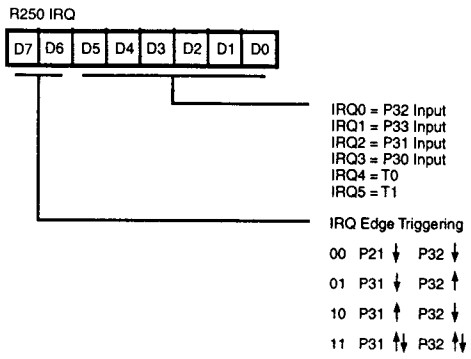


Figure 47. Interrupt Request Register (FAH: Read/Write)

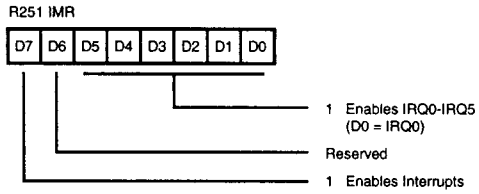


Figure 48. Interrupt Mask Register (FBH: Read/Write)

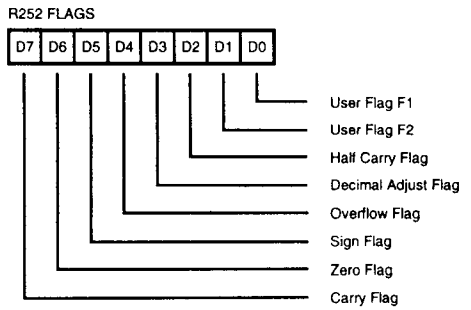


Figure 49. Flag Register (FCH: Read/Write)

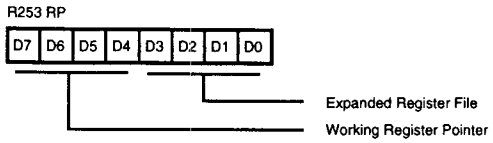


Figure 50. Register Pointer (FDH: Read/Write)

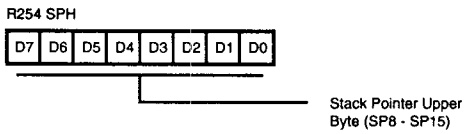


Figure 51. Stack Pointer High (FEH: Read/Write)

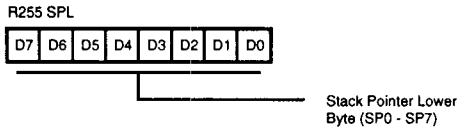


Figure 52. Stack Pointer Low (FFH: Read/Write)

CONDITION CODES

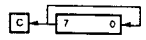
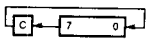
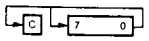
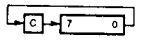
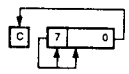
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

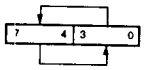
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r		rE r = 0 - F	-	*	*	*	-	-
	R		20						
	IR		21						
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r	Im	rC	-	-	-	-	-	-
	r	R	r8						
	R	r	r9						
			r = 0 - F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

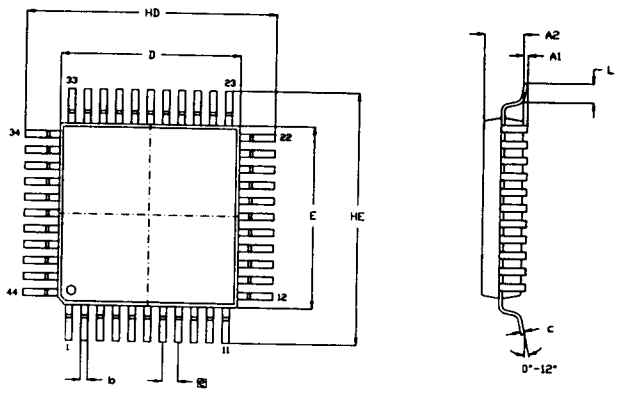
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

PACKAGE INFORMATION (Continued)

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm / .004"

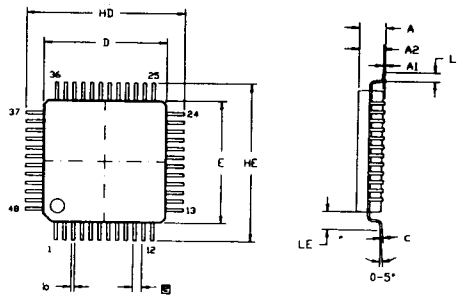
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.05	2.25	.081	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047



44-Pin QFP Package Diagram

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.18	.004	.007
HD	8.60	9.40	.339	.370
D	6.90	7.10	.272	.280
HE	8.60	9.40	.339	.370
E	6.90	7.10	.272	.280
e	0.50 TYP		.020 TYP	
L	0.30	0.70	.012	.028
LE	0.90	1.10	.035	.043

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"



48-Pin VQFP Package Diagram