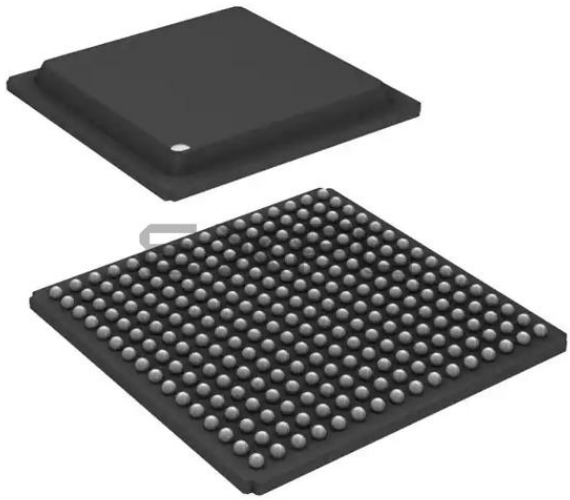

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc852tcvr100a

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	– 40	°C
	$T_{j(max)}$	100	°C

1 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage that high-static voltage or electrical fields cause; however, Freescale recommends taking normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC852T.

Table 3. MPC852T Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	49	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	32	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	41	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	29	
Junction-to-board[4]			$R_{\theta JB}$	24	
Junction-to-case[5]			$R_{\theta JC}$	13	
Junction-to-package top[6]	Natural convection		Ψ_{JT}	3	
	Airflow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal

3 Per JEDEC JESD51-6 with the board horizontal

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter
T_T = thermocouple temperature on top of package
P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

8 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Figure 6 provides the timing for the synchronous output signals.

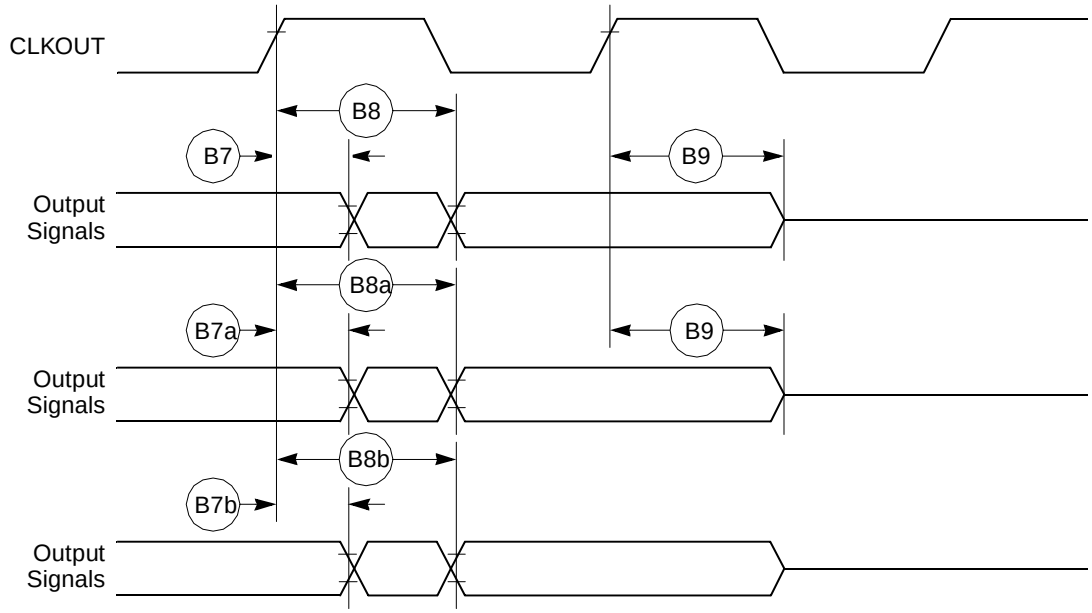

Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

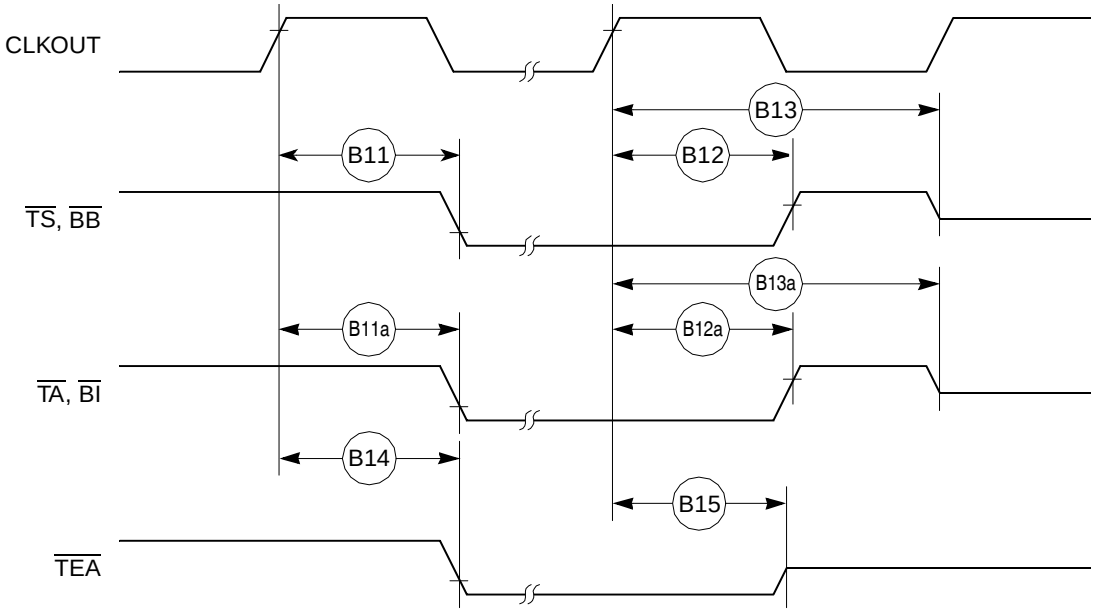

Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

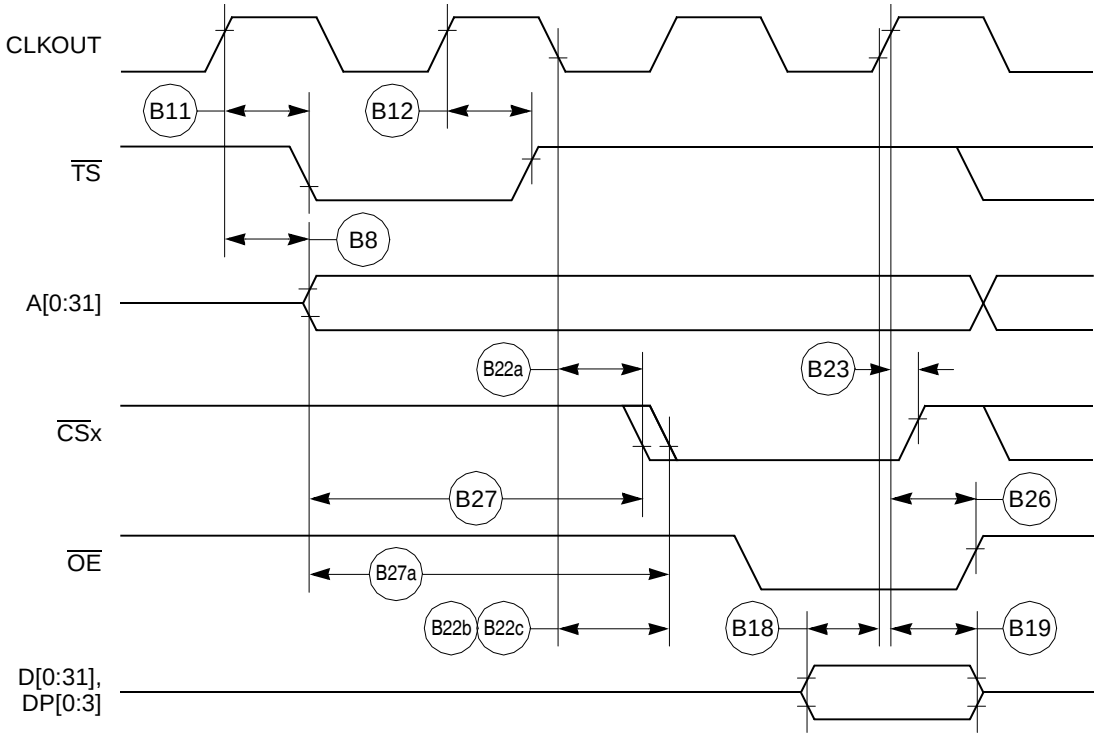

Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 15 through Figure 17 provide the timing for the external bus write that various GPCM factors control.

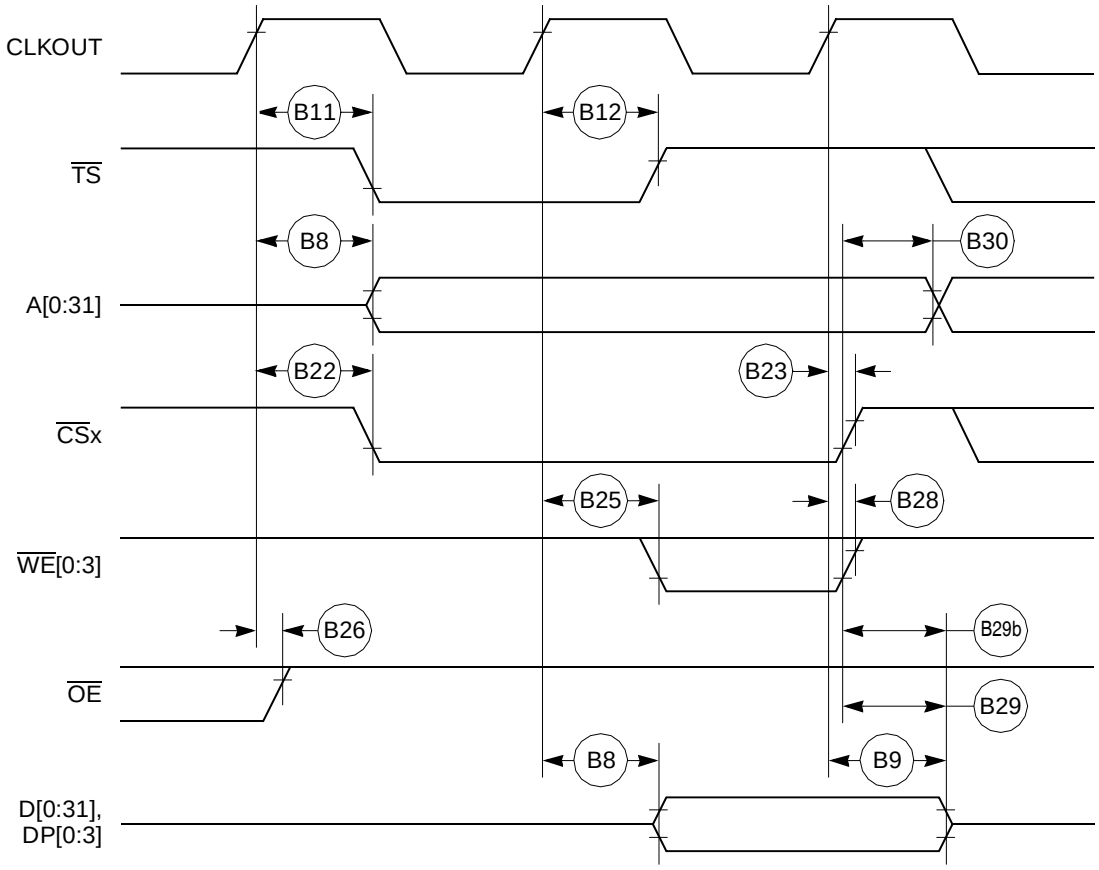

Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

Figure 27 provides the PCMCIA access cycle timing for the external bus write.

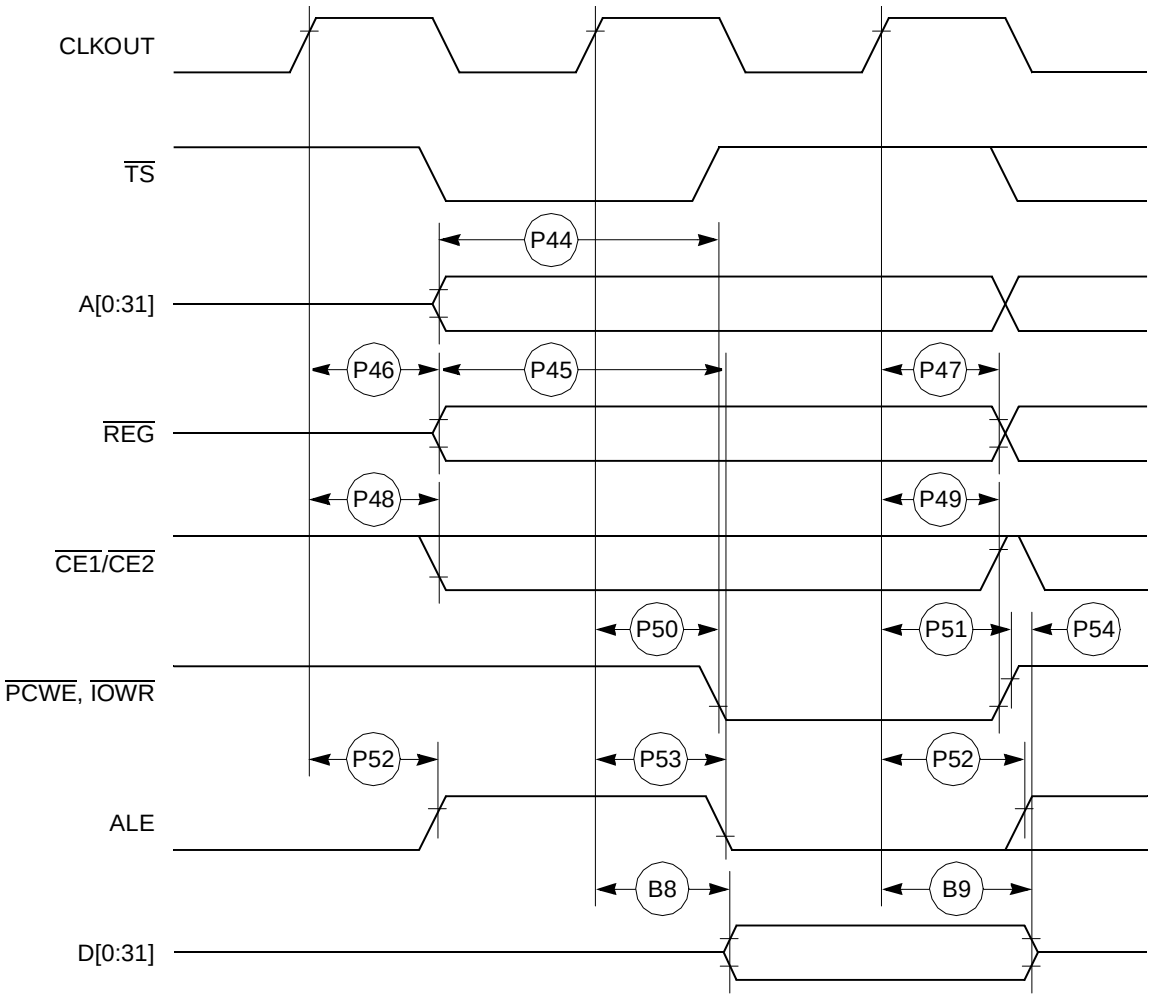

Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA WAIT signals detection timing.

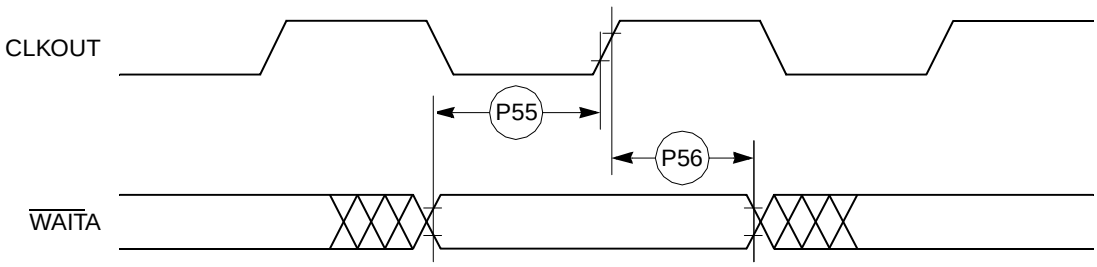

Figure 28. PCMCIA WAIT Signals Detection Timing

14.2 IDMA Controller AC Electrical Specifications

Table 17 provides the IDMA controller timings as shown in Figure 41 through Figure 44.

Table 17. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

1 Applies to high-to-low mode (EDM = 1).

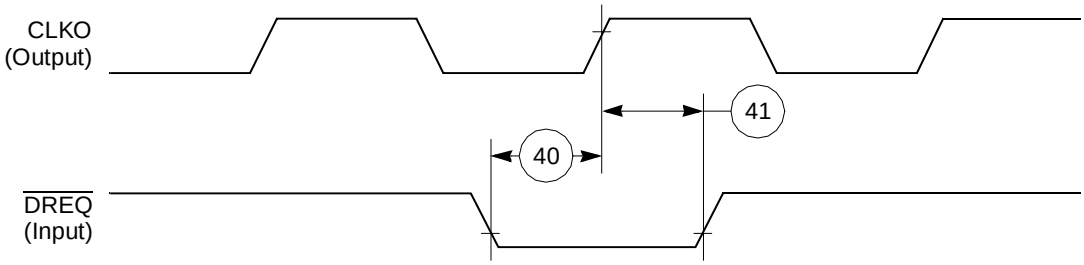

Figure 41. IDMA External Requests Timing Diagram

14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 46.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

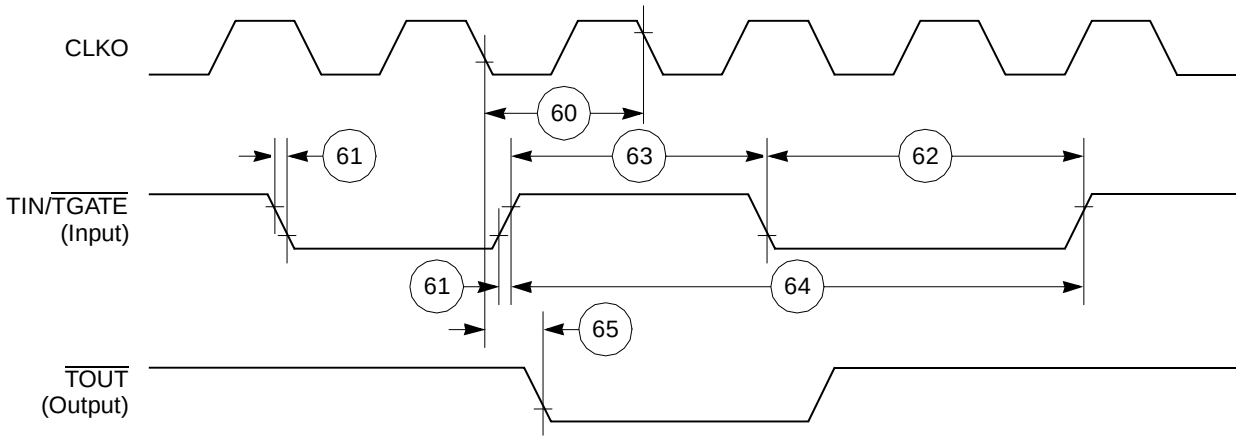

Figure 46. CPM General-Purpose Timers Timing Diagram

14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns

Table 20. NMSI External Clock Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
107	RXD3 hold time from RCLK3 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 47 through Figure 49 show the NMSI timings.

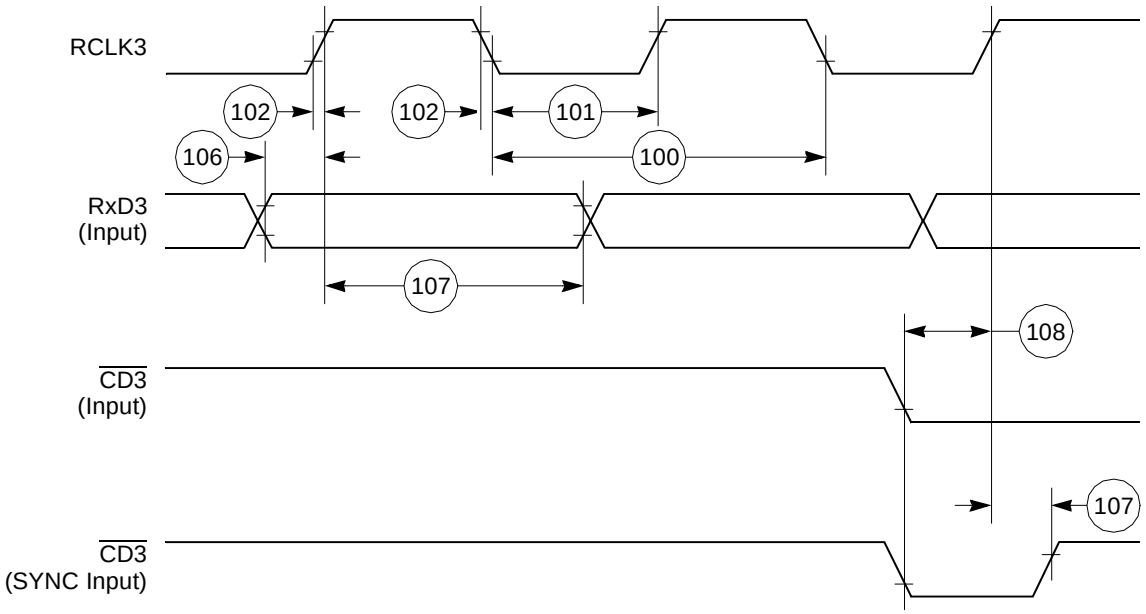

Figure 47. SCC NMSI Receive Timing Diagram

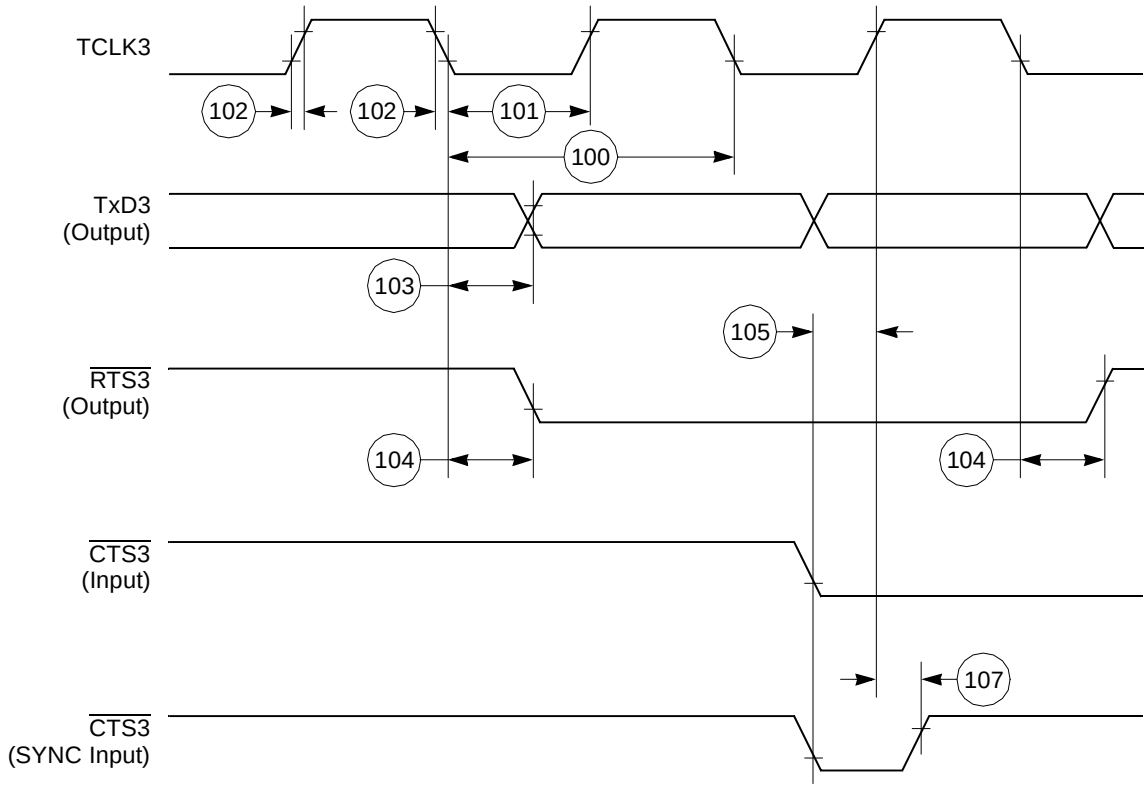

Figure 48. SCC NMSI Transmit Timing Diagram

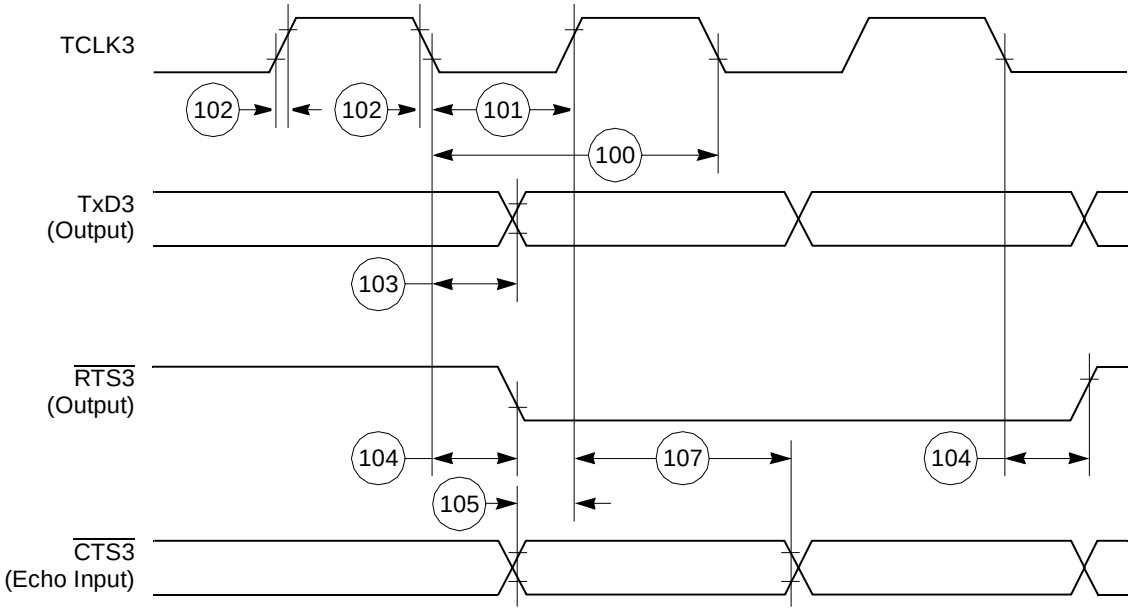

Figure 49. HDLC Bus Timing Diagram

14.6 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 50 through Figure 54.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period[1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

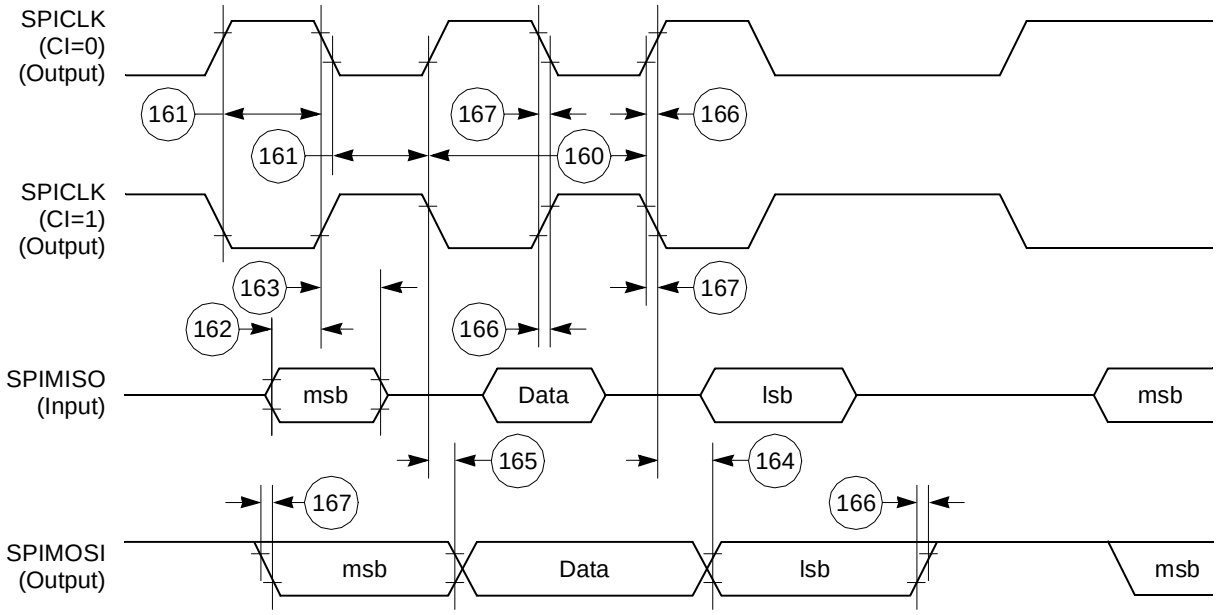

Figure 56. SPI Master (CP = 1) Timing Diagram

14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 57 and Figure 58.

Table 24. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

15.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency –1%.

Table 25 provides information on the MII receive signal timing.

Table 25. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 59 shows MII receive signal timing.

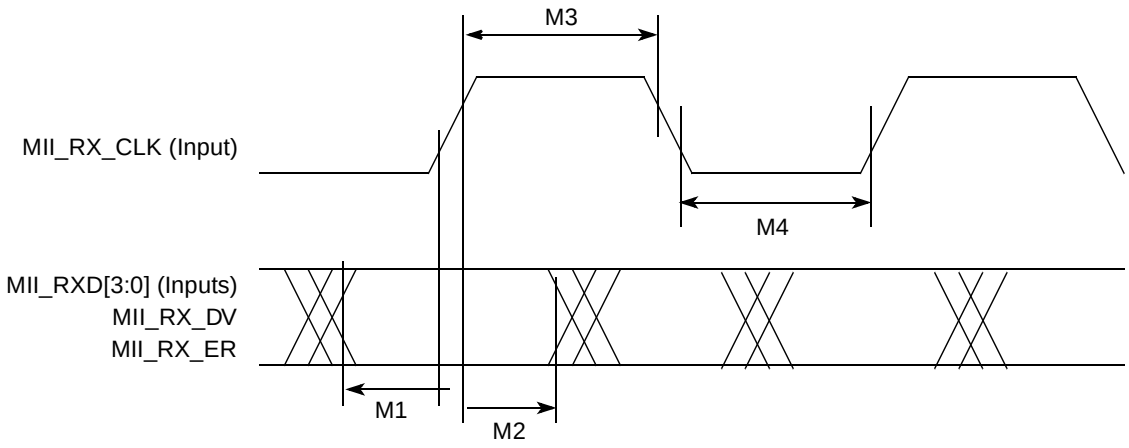

Figure 59. MII Receive Signal Timing Diagram

15.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 28 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 28. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 62 shows the MII serial management channel timing diagram.

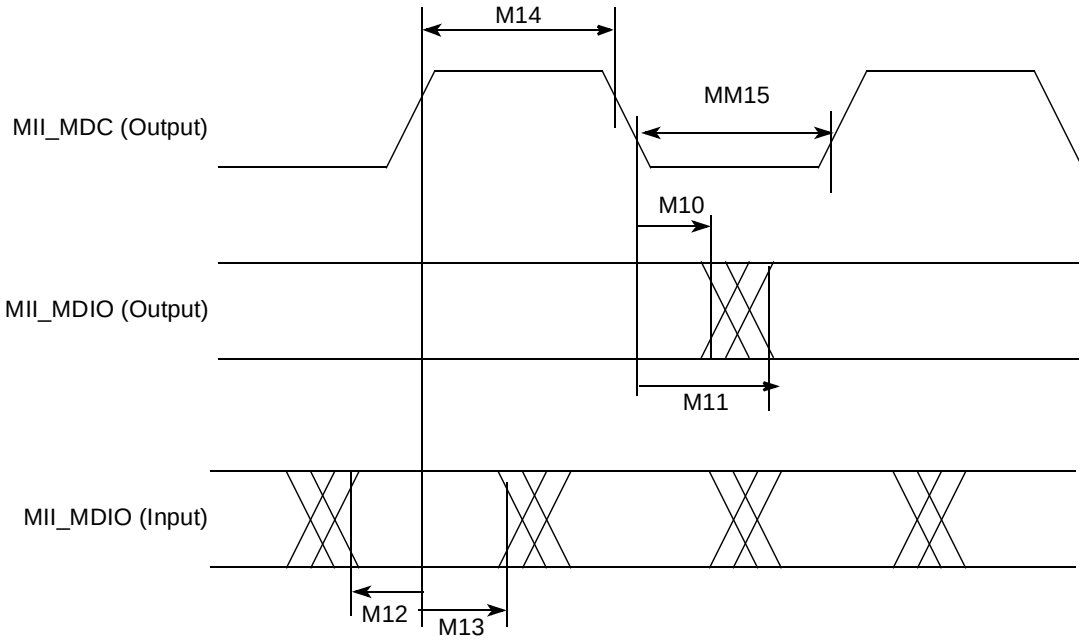

Figure 62. MII Serial Management Channel Timing Diagram

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
FRZ IRQ6	H4	Bidirectional (3.3 V only)
IRQ0	P13	Input (3.3 V only)
IRQ1	M11	Input (3.3 V only)
M_TX_CLK IRQ7	N12	Input (3.3 V only)
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3 V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3 V only)
RSTCONF	K4	Input (3.3 V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output

16.1.2 The non-JEDEC Pinout

Figure 64 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *PowerQUICC™ Family Reference Manual*.

NOTE: This figure shows the top view of the device.

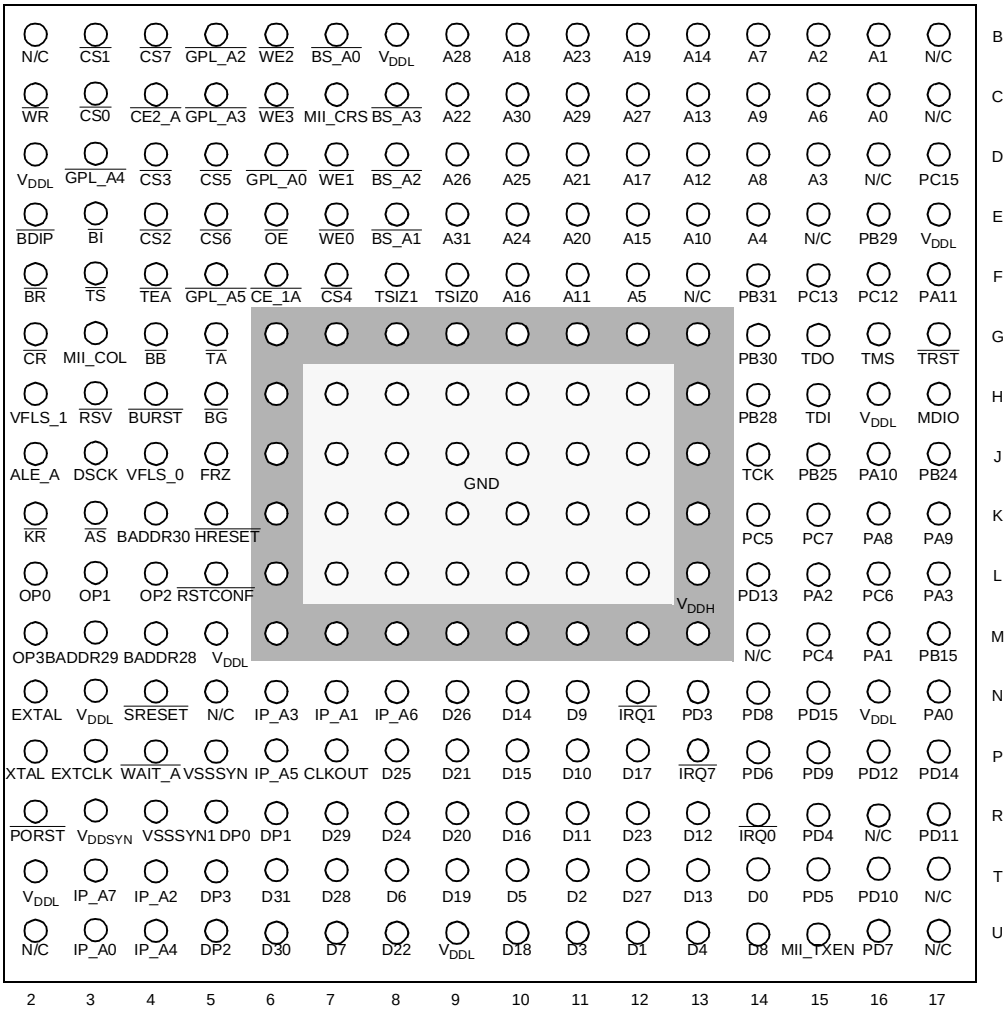

Figure 64. Pinout of PBGA Package—Non-JEDEC

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$, BS_B0, $\overline{IORD}$	E7	Output
$\overline{WE1}$, BS_B1, $\overline{IOWR}$	D7	Output
$\overline{WE2}$, BS_B2, $\overline{PCOE}$	B6	Output
$\overline{WE3}$, BS_B3, $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$, $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$, $\overline{GPL\_A1}$, $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3], $\overline{GPL\_B}$[2:3], $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA, $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)
$\overline{RSTCONF}$	L5	Input (3.3 V only)
$\overline{HRESET}$	K5	Open-drain
$\overline{SRESET}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{CE1\_A}$	F6	Output
$\overline{CE2\_A}$	C4	Output
$\overline{WAIT\_A}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PD12, MII_MDC	P16	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	R17	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	T16	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	P15	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	N14	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	U16	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	P14	Bidirectional (5-V tolerant)
PD5, MII_TXD3	T15	Bidirectional (5-V tolerant)
PD4, MII_TXD2	R15	Bidirectional (5-V tolerant)
PD3, MII_TXD1	N13	Bidirectional (5-V tolerant)
TMS	G16	Input (5-V tolerant)
TDI, DSDI	H15	Input (5-V tolerant)
TCK, DSCK	J14	Input (5-V tolerant)
$\overline{\text{TRST}}$	G17	Input (5-V tolerant)
TDO, DSDO	G15	Output (5-V tolerant)
MII_CRS	C7	Input
MII_MDIO	H17	Bidirectional (5-V tolerant)
MII_TX_EN	U15	Output (5-V tolerant)
MII_COL	G3	Input
V_{SSSYN}	P5	PLL analog GND

17 Document Revision History

Table 32 lists significant changes between revisions of this document.

Table 32. Document Revision History

Revision	Date	Changes
4		• Updated template. • On page 1, updated first paragraph and added a second paragraph. • After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 2) and renumbered the rest of the figures. • In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. • In Figure 4, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. • In Table 17, changed num 46 description to read, "$\overline{TA}$ assertion to rising edge ..." • In Figure 42, changed $\overline{TA}$ to reflect the rising edge of the clock.
3.1	1/18/2005	Document template update.
3.0	11/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Broke the Section 16.1, "Pin Assignments," into 2 smaller sections for the JEDEC and non-JEDEC pinouts.
2.0	12/2003	Put 852T on the 1st page in place of 8245. Figure 62 on page 59 had overbars added on signals CR (pin G2) and WAIT_A (pin P4).
1.8	7/2003	Changed the pinout to be JEDEC Compliant, changed timing parameters B28a through B28d, and B29d to show that TRLX can be 0 or 1.
1.7	5/2003	Changed the SPI Master Timing Specs. 162 and 164
1.6	4/2003	Changed the package drawing in Figure 15-63
1.5	4/2003	Changed 5 Port C pins with interrupt capability to 7 Port C pins. Added the Note: solder sphere composition for MPC852TVR and MPC852TCVR devices is 95.5%Sn 45%Ag 0.5%Cu to Figure 15-63
1.4	2/2003	Changed Table 15-30 Pin Assignments for the PLL Pins V_{SSSYN1}, V_{SSSYN}, V_{DDSYN}
1.3	1/2003	Added subscripts to timing diagrams for B1-B35, to specify memory controller settings for the specific edges.
1.2	1/2003	In Table 15-30, specified EXTCLK as 3.3 V.
1.1	12/2002	Added fast Ethernet controller to the features
1	11/2002	Added values for 80 and 100 MHz
0	10/2002	Initial release