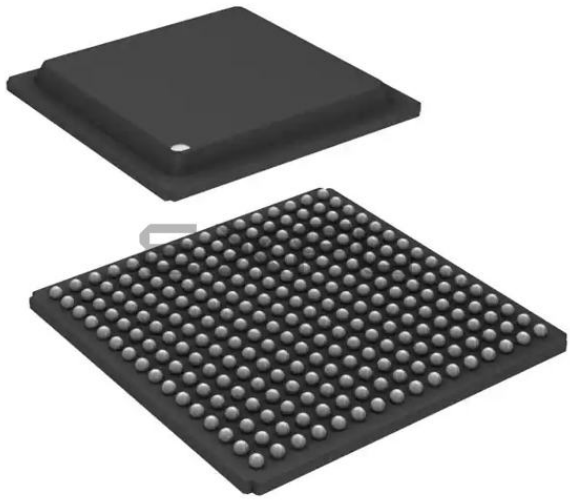

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc852tczt100a

1 Overview

The MPC852T is a 0.18-micron derivative of the MPC860 PowerQUICC™ family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8-V core and a 3.3-V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

2 Features

The MPC852T is comprised of three modules that each use a 32-bit internal bus: an MPC8xx core, system integration unit (SIU), and communication processor module (CPM).

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - 50/66 MHz core frequencies support both 1:1 and 2:1 modes
  - 80/100 MHz core frequencies support 2:1 mode only
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction caches is two-way, set-associative with 128 sets
    - 4-Kbyte data cachesis two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank

  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller-programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet controller (FEC)
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable or disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1™ standard test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Seven port pins with interrupt capability
  - Eighteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest-priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Eight serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability

- Two baud rate generators
  - Independent (can be connected toany SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3® standard optional on SCC3 and SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channel)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

Figure 1 shows the MPC852T block diagram.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical[1]	Maximum[2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V. and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation, and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application that buffer current can cause, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC852T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} to V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO)[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V

where:

T_A = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. Thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature (ºC)

P_D = power dissipation in package

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 and CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3/BS_B[0:3]) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[8]	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[8]	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) Invalid GPCM write access [9] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

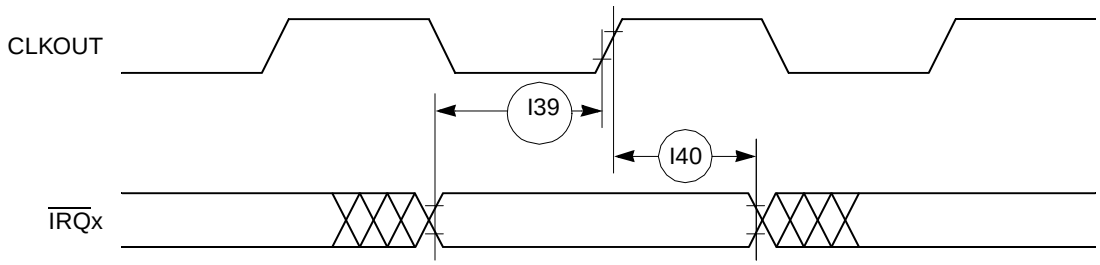

Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

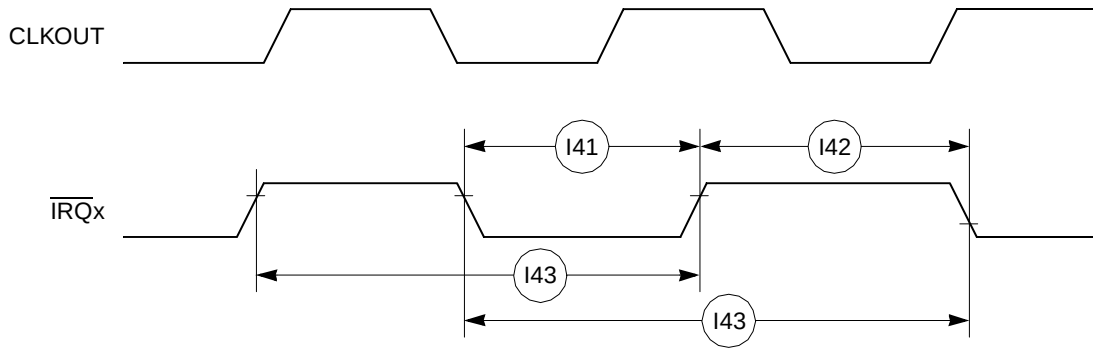

Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Table 13 shows the debug port timing for the MPC852T.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	DSCK cycle time	$3 \times T_{CLOCKOUT}$	—	—
J83	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
J84	DSCK rise and fall times	0.00	3.00	ns
J85	DSDI input data setup time	8.00	—	ns
J86	DSDI data hold time	5.00	—	ns
J87	DSCK low to DSDO data valid	0.00	15.00	ns
J88	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 31 provides the input timing for the debug port clock.

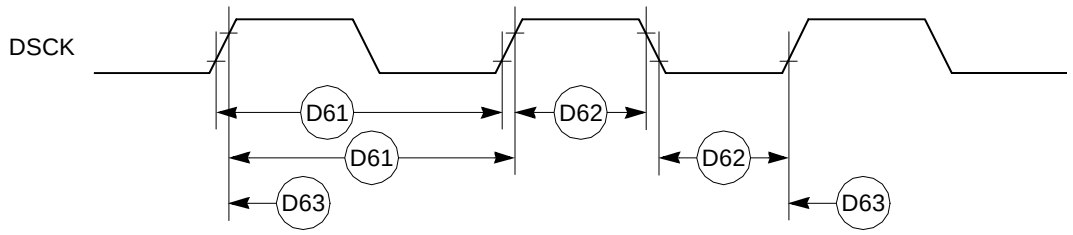

Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.

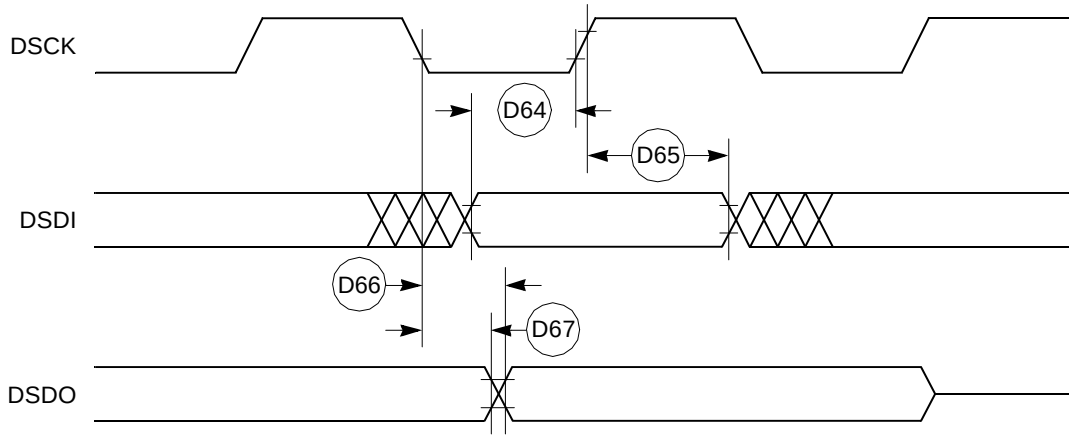

Figure 32. Debug Port Timings

Table 14 shows the reset timing for the MPC852T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge set up time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK set up (MIN = 3.00 × B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

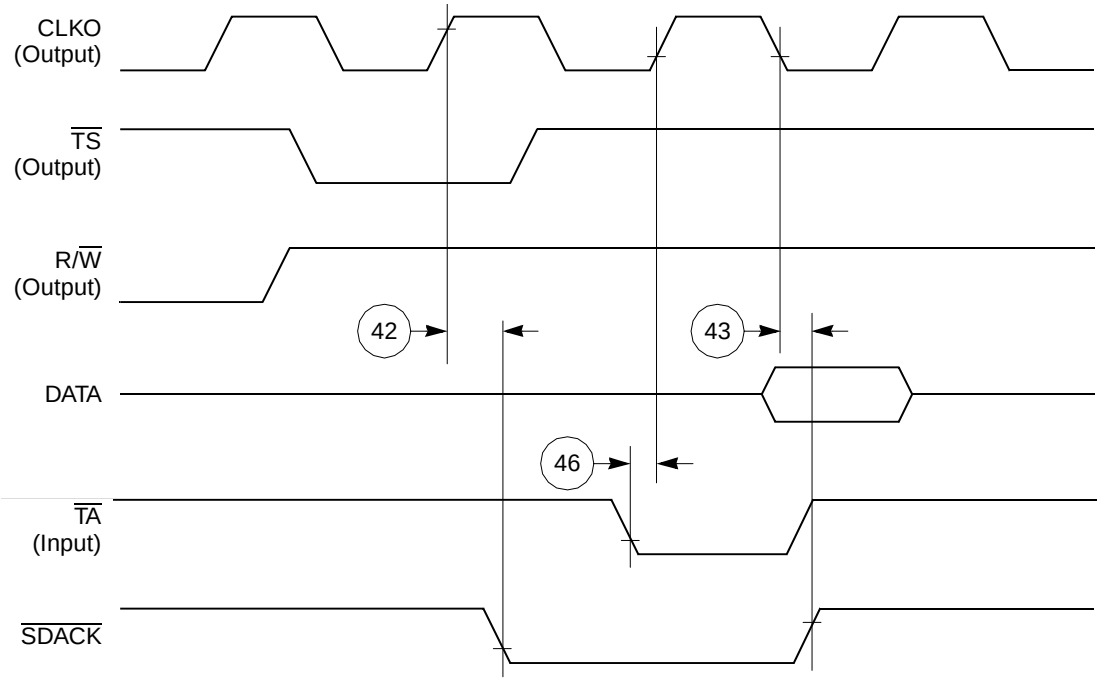

Figure 42. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

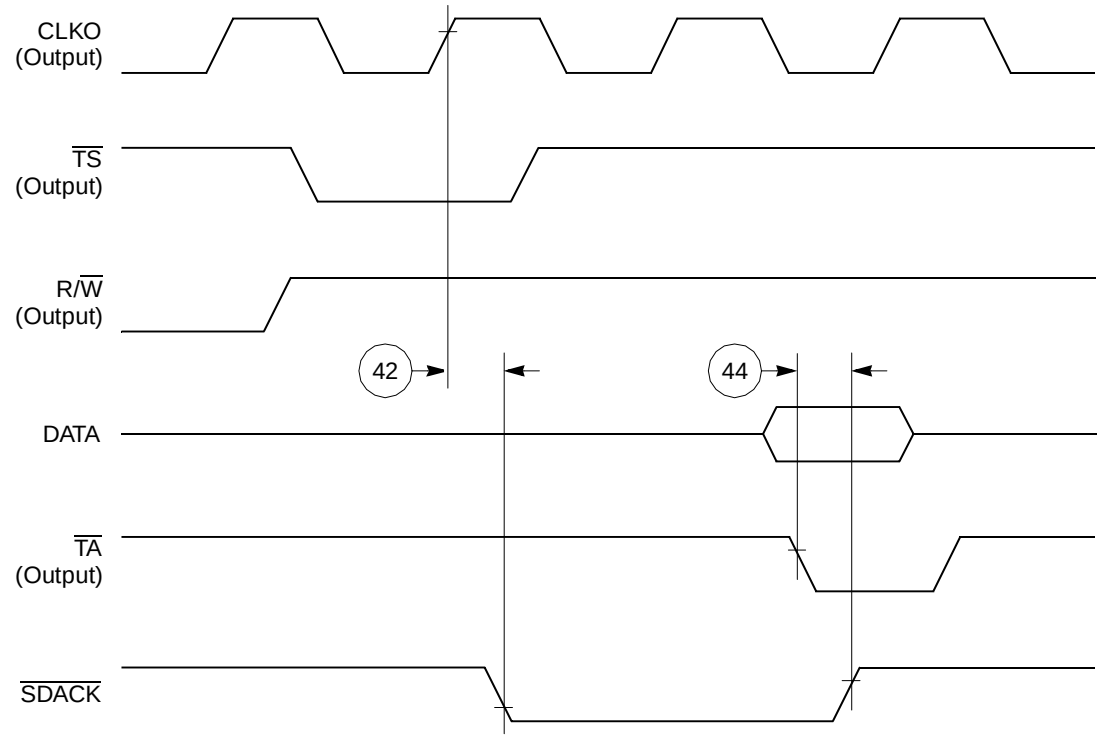

Figure 43. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 46.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

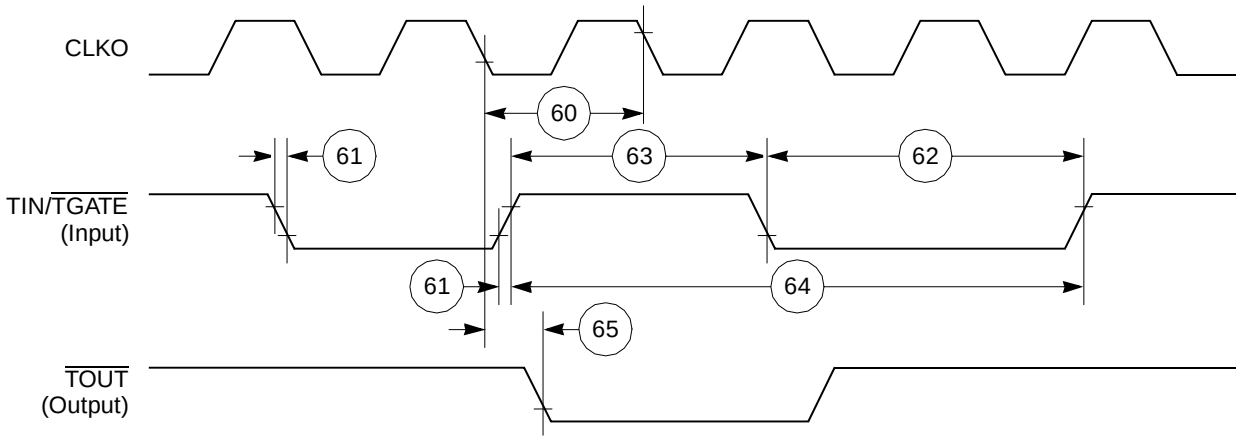

Figure 46. CPM General-Purpose Timers Timing Diagram

14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns

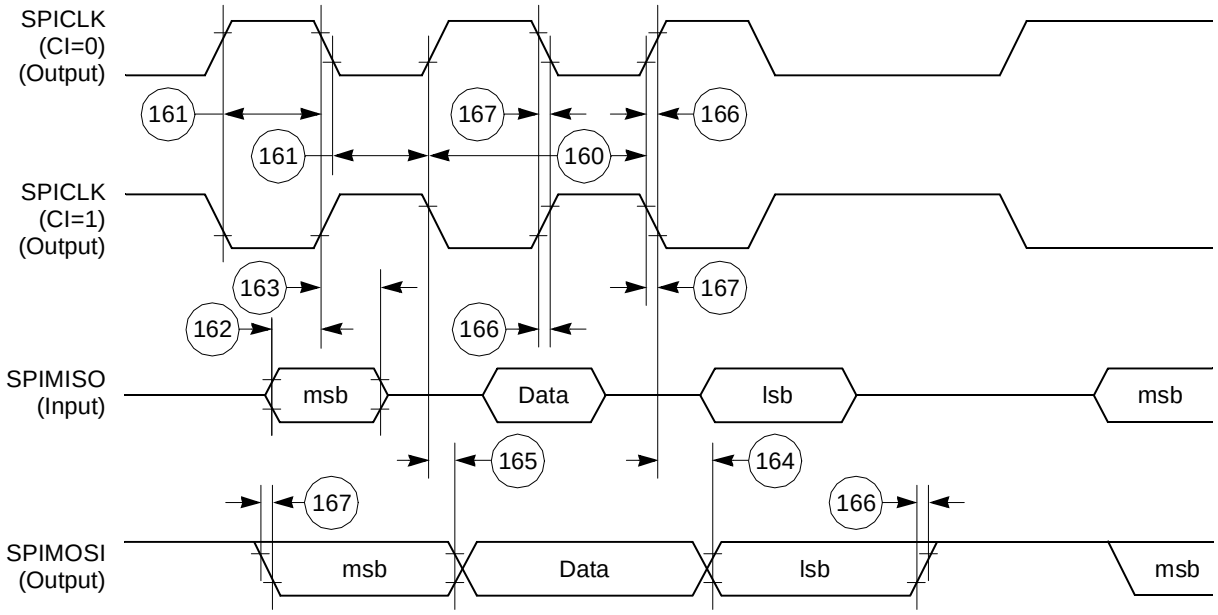

Figure 56. SPI Master (CP = 1) Timing Diagram

14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 57 and Figure 58.

Table 24. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

15.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency –1%.

Table 25 provides information on the MII receive signal timing.

Table 25. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 59 shows MII receive signal timing.

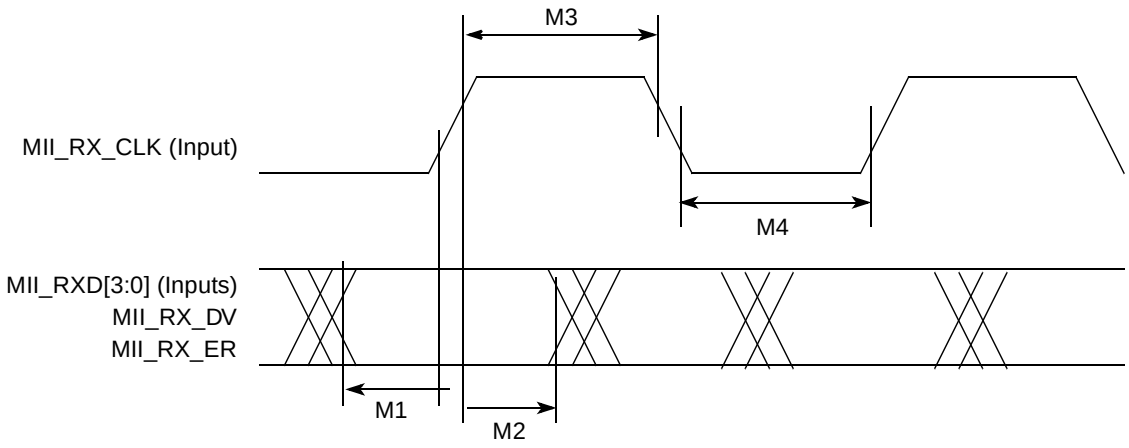

Figure 59. MII Receive Signal Timing Diagram

15.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
FRZ IRQ6	H4	Bidirectional (3.3 V only)
IRQ0	P13	Input (3.3 V only)
IRQ1	M11	Input (3.3 V only)
M_TX_CLK IRQ7	N12	Input (3.3 V only)
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3 V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3 V only)
RSTCONF	K4	Input (3.3 V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MII_CRS	B6	Input

16.1.2 The non-JEDEC Pinout

Figure 64 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *PowerQUICC™ Family Reference Manual*.

NOTE: This figure shows the top view of the device.

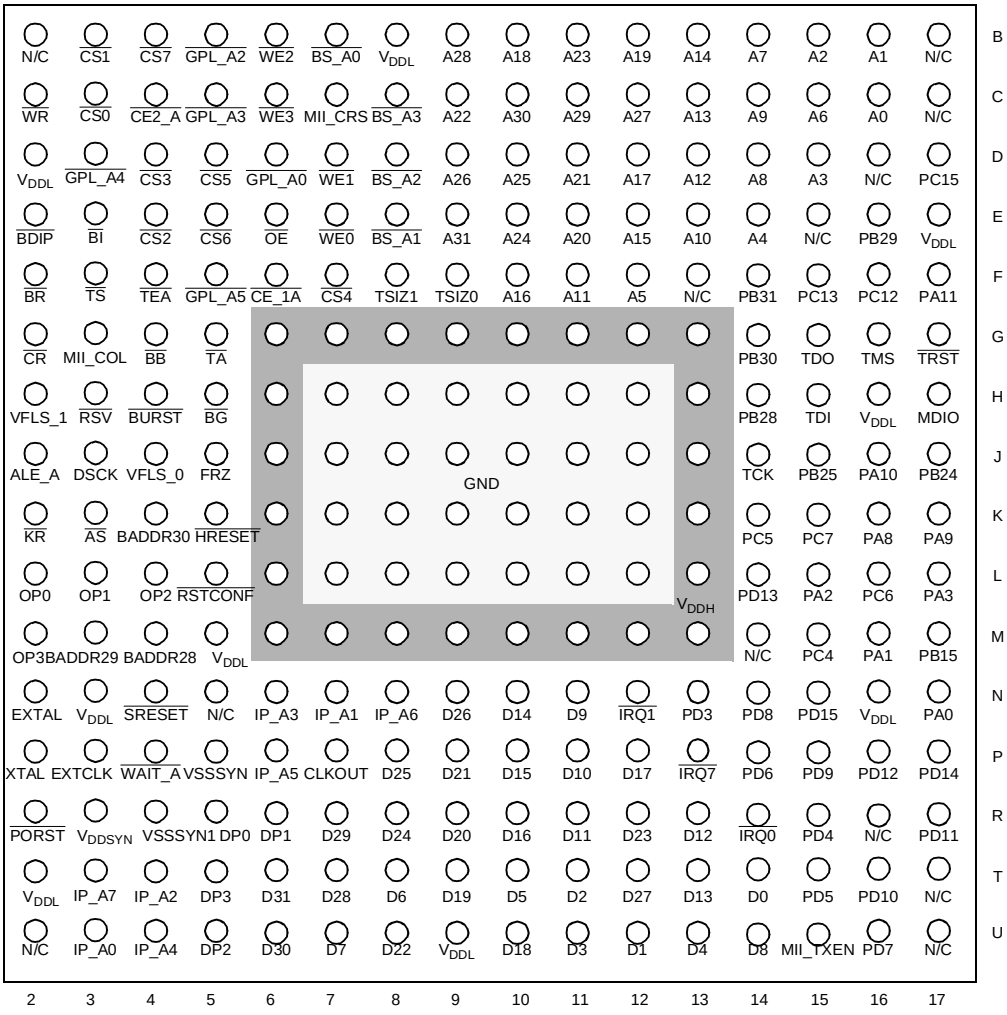

Figure 64. Pinout of PBGA Package—Non-JEDEC

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$, BS_B0, $\overline{IORD}$	E7	Output
$\overline{WE1}$, BS_B1, $\overline{IOWR}$	D7	Output
$\overline{WE2}$, BS_B2, $\overline{PCOE}$	B6	Output
$\overline{WE3}$, BS_B3, $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$, $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$, $\overline{GPL\_A1}$, $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3], $\overline{GPL\_B}$[2:3], $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA, $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)
$\overline{RSTCONF}$	L5	Input (3.3 V only)
$\overline{HRESET}$	K5	Open-drain
$\overline{SRESET}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{CE1\_A}$	F6	Output
$\overline{CE2\_A}$	C4	Output
$\overline{WAIT\_A}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PB31, $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	G14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	J17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	M17	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	D17	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	F15	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	F16	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	K15	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	L16	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	K14	Bidirectional (5-V tolerant)
PC4, $\overline{\text{CD4}}$	M15	Bidirectional (5-V tolerant)
PD15, MII_RXD3	N15	Bidirectional (5-V tolerant)
PD14, MII_RXD2	P17	Bidirectional (5-V tolerant)
PD13, MII_RXD1	L14	Bidirectional (5-V tolerant)

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