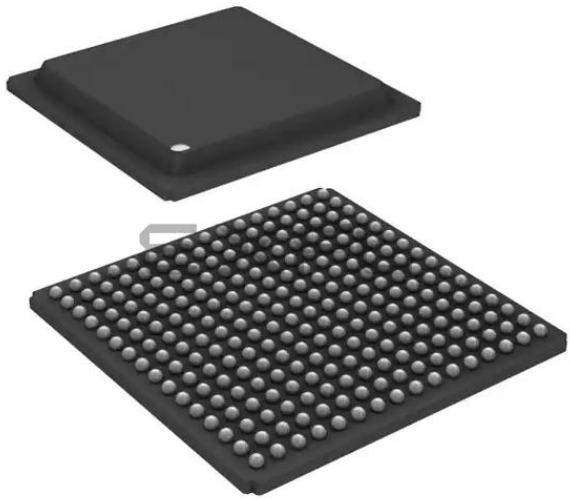


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tcvr100a

- Two baud rate generators
  - Independent (can be connected toany SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3® standard optional on SCC3 and SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channel)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

Figure 1 shows the MPC852T block diagram.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical[1]	Maximum[2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V. and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation, and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application that buffer current can cause, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC852T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} to V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO)[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in Table 6 in the boot code after the reset deasserts.

Table 6. Mandatory Reset Configuration of MPC852T

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4–7] PAPAR[12–15]	0
PADIR (Port A data direction register)	PADIR[4–7] PADIR[12–15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16–23] PBPAR[26–27]	0
PBDIR (Port B data direction register)	PBDIR[14] PBDIR[16–23] PBDIR[26–27]	1
PCPAR (Port C pin assignment register)	PCPAR[8–11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8–11] PCDIR[14]	1

11 Layout Practices

Each V_{DD} pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC866 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})."

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 +.000)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = 0.00 × B1 + 1.00[4])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time)[5] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time)[5] (MIN = 0.00 × B1 + 1.00[6])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time)[7] (MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time)[7] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 and CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3/BS_B[0:3]) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[8]	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)[8]	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) Invalid GPCM write access [9] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Figure 4 is the control timing diagram.

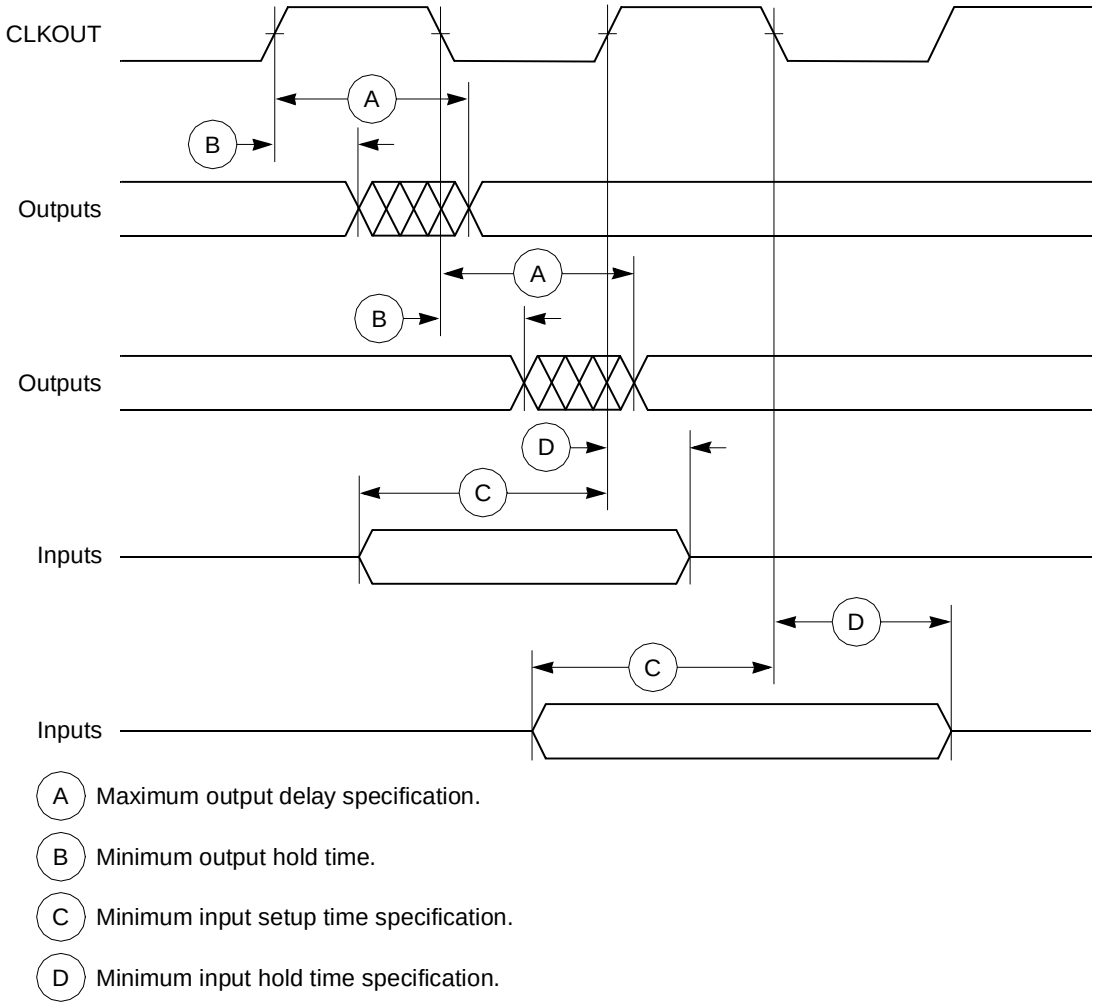


Figure 4. Control Timing

Figure 5 provides the timing for the external clock.

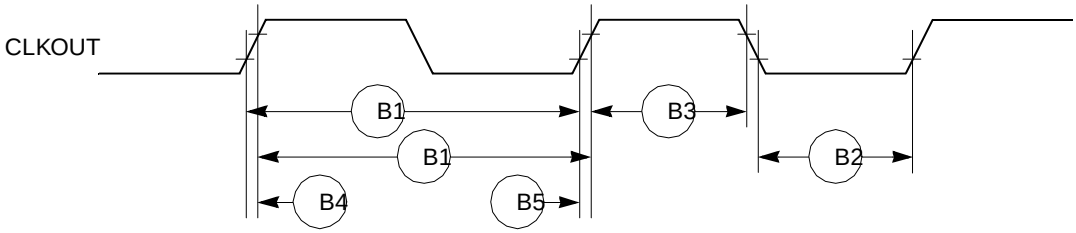


Figure 5. External Clock Timing

Figure 8 provides the timing for the synchronous input signals.

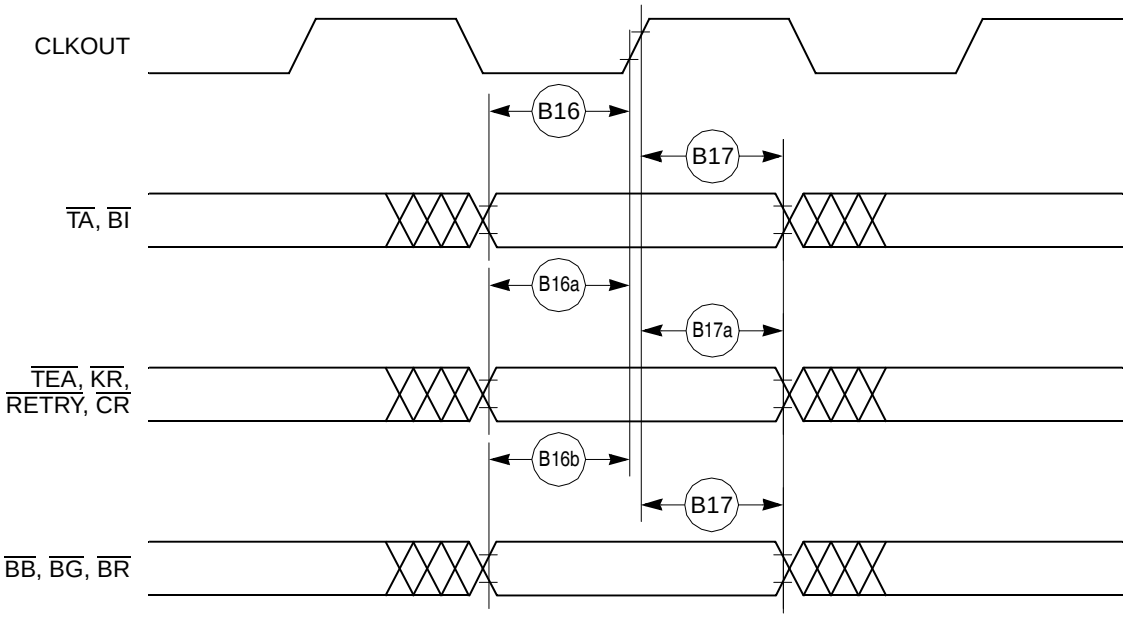


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

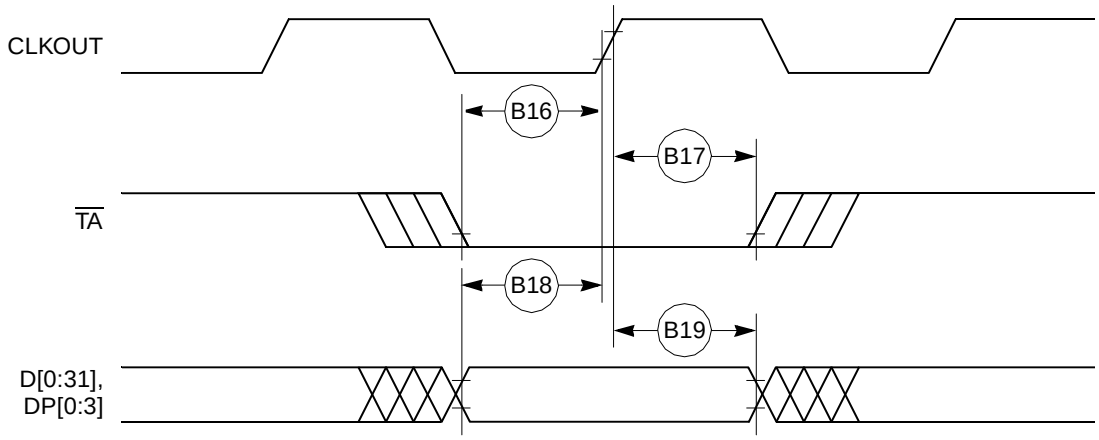


Figure 9. Input Data Timing in Normal Case

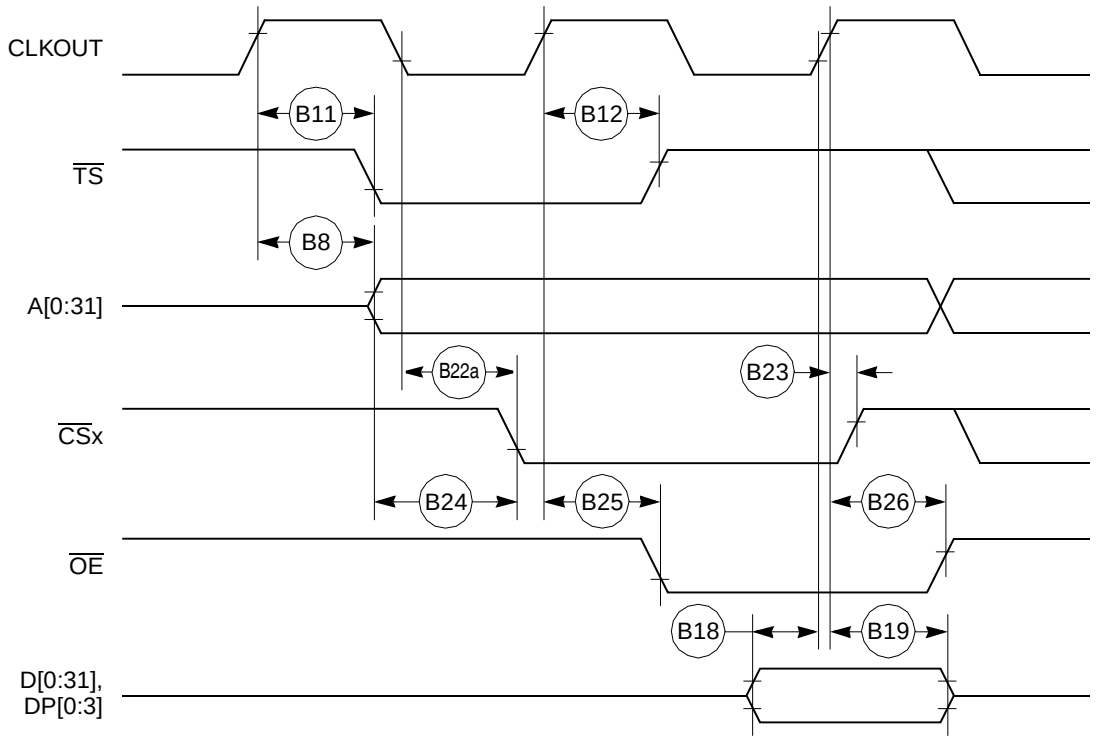


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

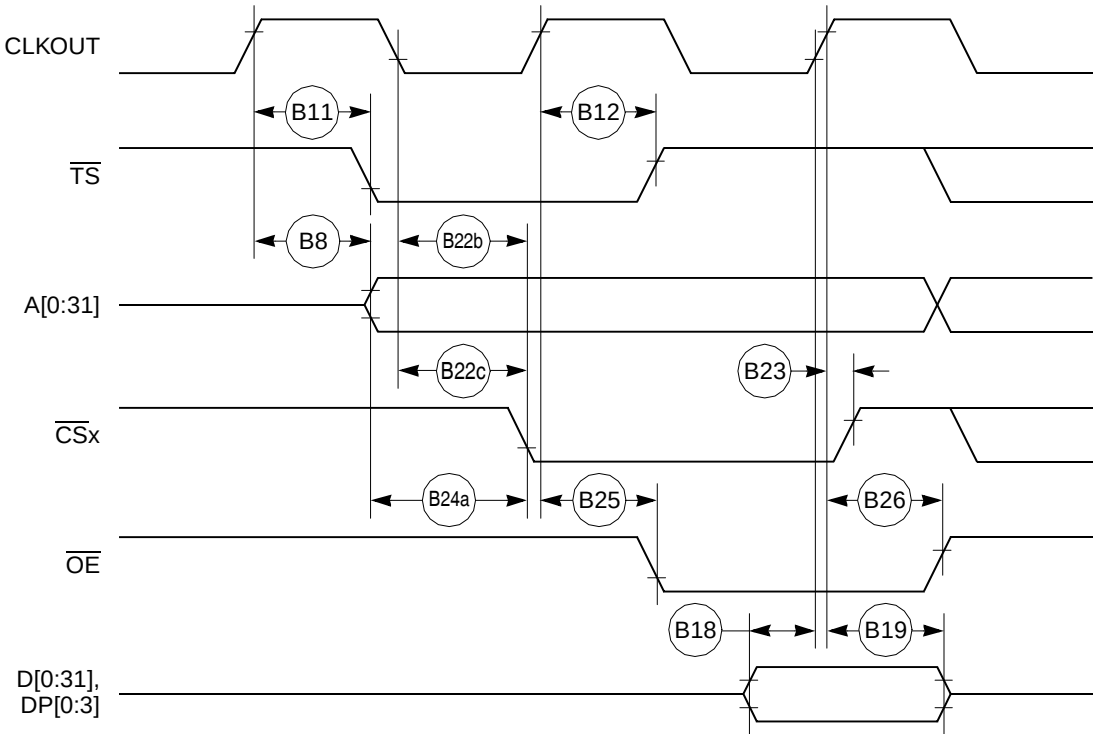


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

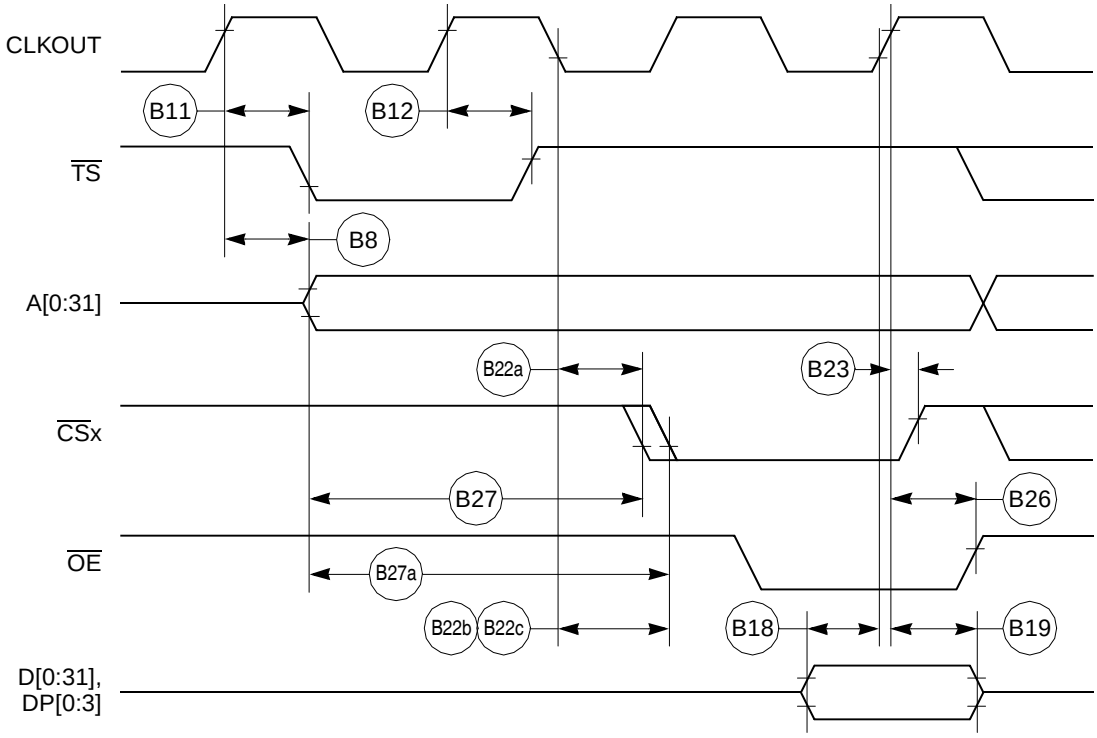


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

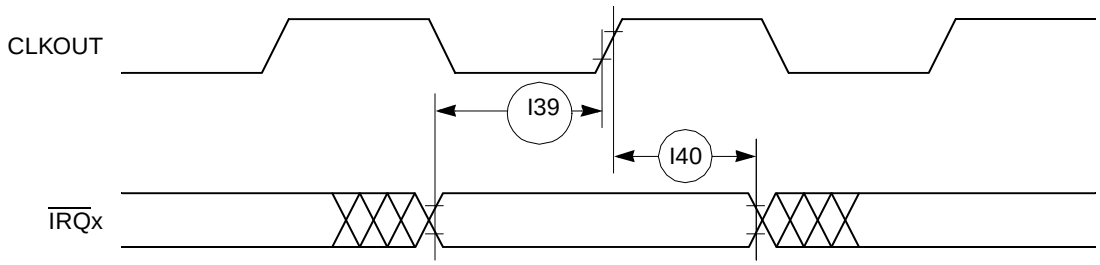


Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

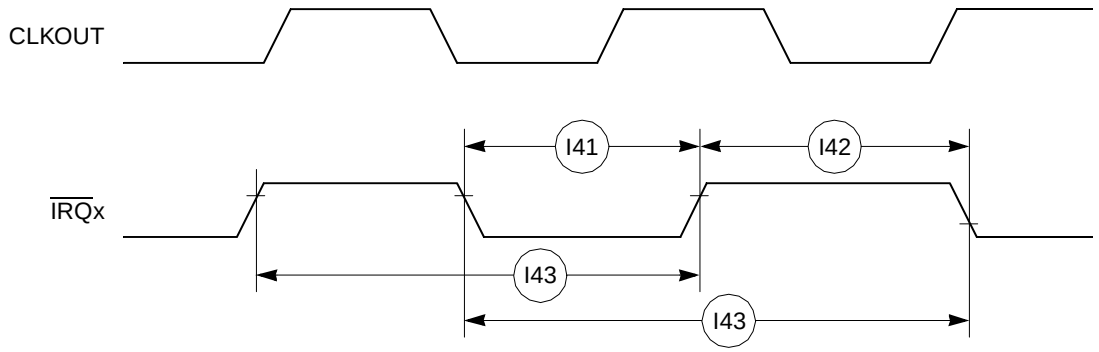


Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Table 14 shows the reset timing for the MPC852T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge set up time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK set up (MIN = 3.00 × B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

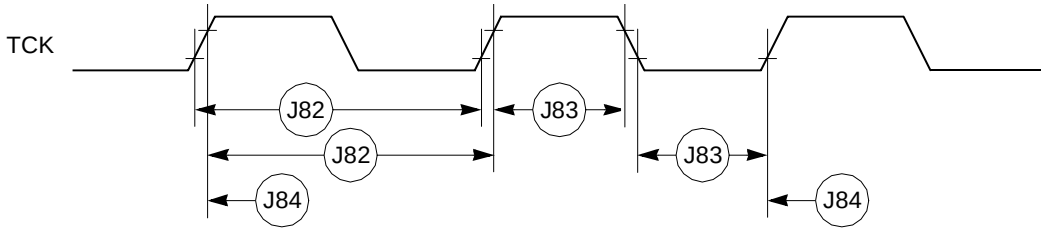


Figure 36. JTAG Test Clock Input Timing

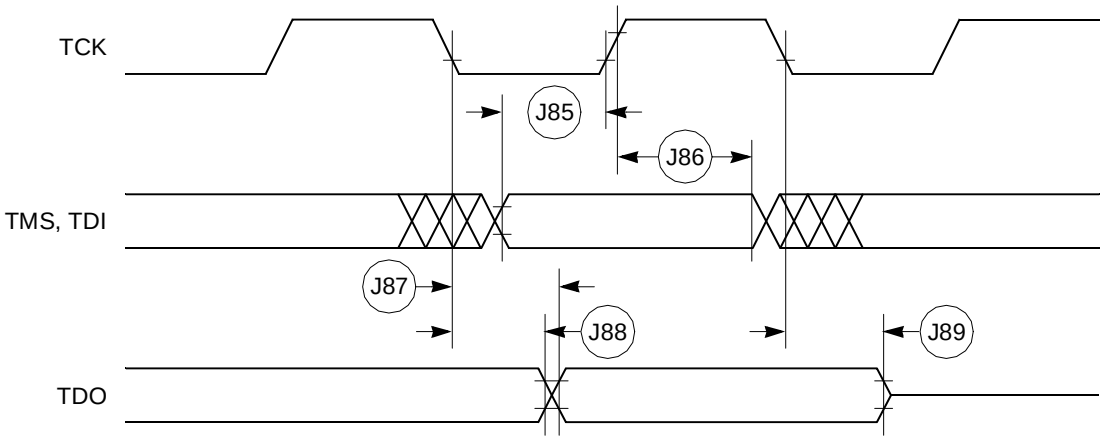


Figure 37. JTAG Test Access Port Timing Diagram

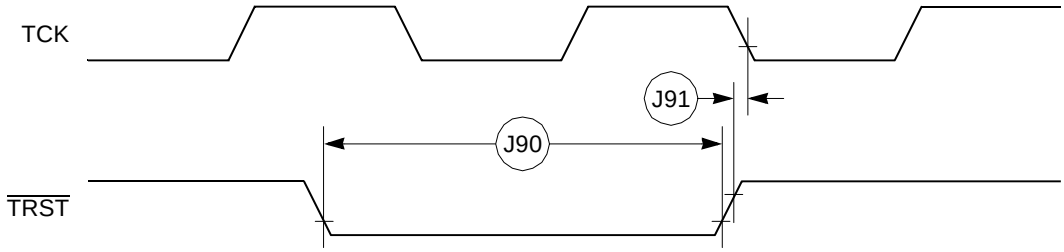


Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

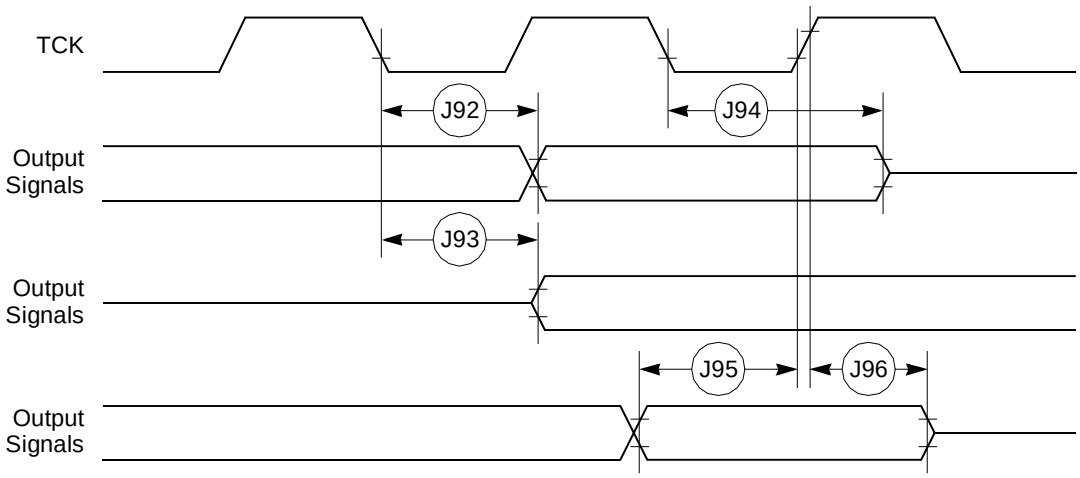


Figure 39. Boundary Scan (JTAG) Timing Diagram

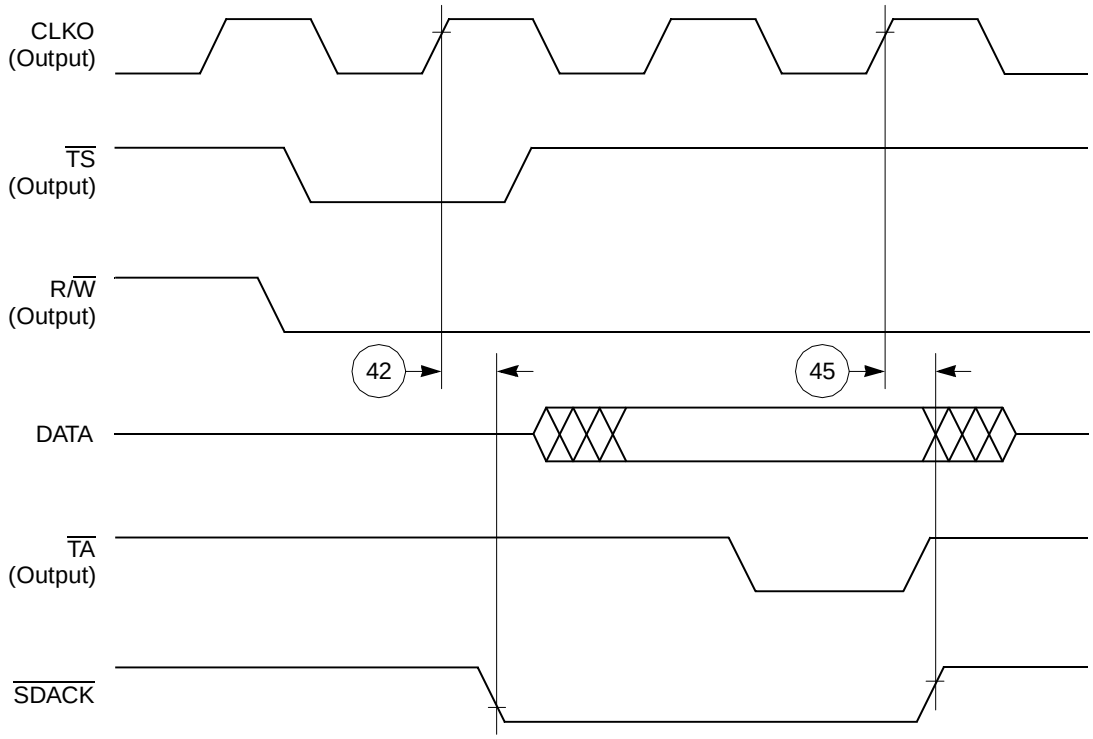


Figure 44. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

14.3 Baud Rate Generator AC Electrical Specifications

Table 18 provides the baud rate generator timings as shown in Figure 45.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

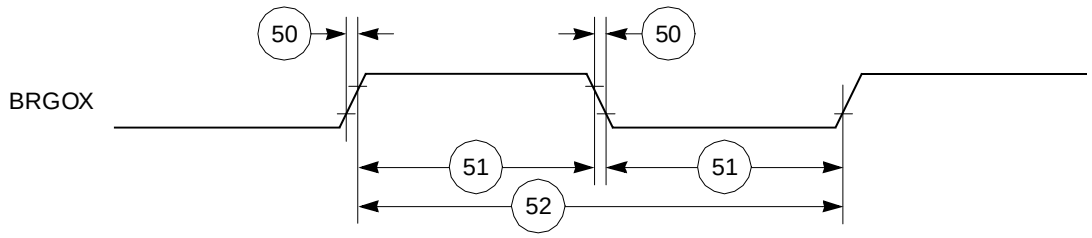


Figure 45. Baud Rate Generator Timing Diagram

14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 46.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

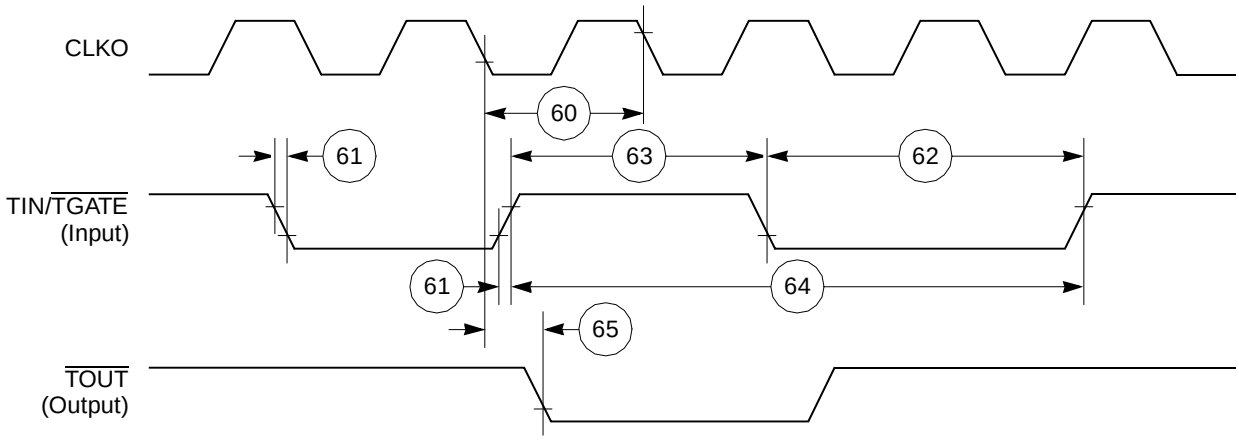


Figure 46. CPM General-Purpose Timers Timing Diagram

14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high[1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK + 5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns

Table 20. NMSI External Clock Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
107	RXD3 hold time from RCLK3 rising edge[2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

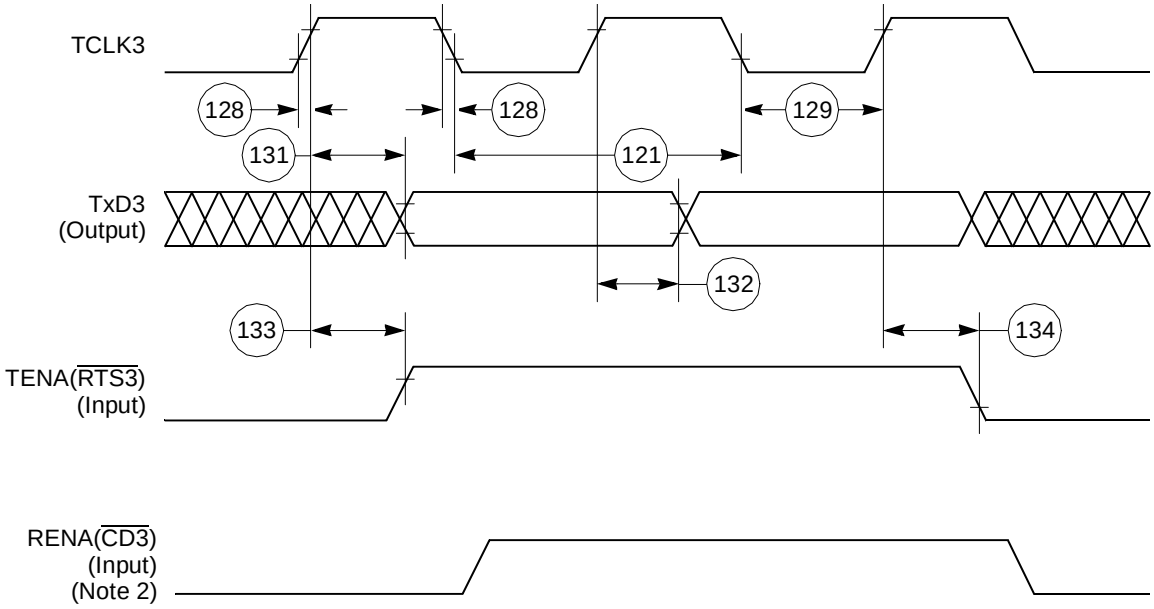
Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency[1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge[2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.



Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 52. Ethernet Transmit Timing Diagram

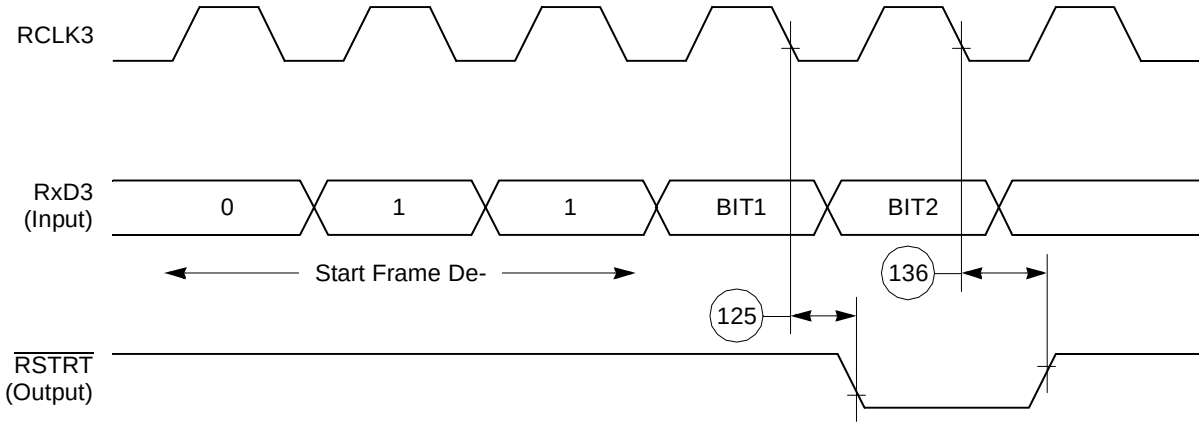


Figure 53. CAM Interface Receive Start Timing Diagram

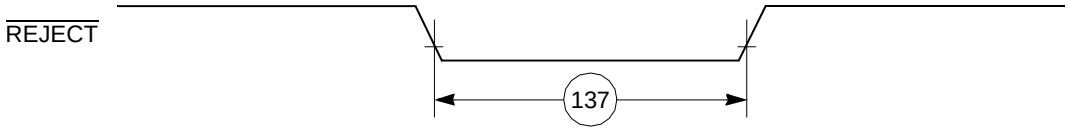


Figure 54. CAM Interface REJECT Timing Diagram

Table 31 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

Table 31. Pin Assignments—Non-JEDEC

Name	Pin Number	Type
A[0:31]	C16, B16, B15, D15, E14, F12, C15, B14, D14, C14, E13, F11, D13, C13, B13, E12, F10, D12, B10, B12, E11, D11, C9, B11, E10, D10, D9, C12, B9, C11, C10, E9	Bidirectional Three-state (3.3 V only)
TSIZ0, $\overline{\text{REG}}$	F9	Bidirectional Three-state (3.3 V only)
TSIZ1	F8	Bidirectional Three-state (3.3 V only)
RD/$\overline{\text{WR}}$	C2	Bidirectional Three-state (3.3 V only)
$\overline{\text{BURST}}$	H4	Bidirectional Three-state (3.3 V only)
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	E2	Output
$\overline{\text{TS}}$	F3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TA}}$	G5	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TEA}}$	F4	Open-drain
$\overline{\text{BI}}$	E3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	H3	Bidirectional Three-state (3.3 V only)
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$ $\overline{\text{RETRY}}$, SPKROUT	K2	Bidirectional Three-state (3.3 V only)
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	G2	Input (3.3 V only)
D[0:31]	T14, U12, T11, U11, U13, T10, T8, U7, U14, N11, P11, R11, R13, T13, N10, P10, R10, P12, U10, T9, R9, P9, U8, R12, R8, P8, N9, T12, T7, R7, U6, T6	Bidirectional Three-state (3.3 V only)
DP0, $\overline{\text{IRQ3}}$	R5	Bidirectional Three-state (3.3 V only)
DP1, $\overline{\text{IRQ4}}$	R6	Bidirectional Three-state (3.3 V only)
DP2, $\overline{\text{IRQ5}}$	U5	Bidirectional Three-state (3.3 V only)
DP3, $\overline{\text{IRQ6}}$	T5	Bidirectional Three-state (3.3 V only)
$\overline{\text{BR}}$	F2	Bidirectional (3.3 V only)
$\overline{\text{BG}}$	H5	Bidirectional (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IP_A1	N7	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2, MODCK1, $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30, $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11, RXD3	F17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	K17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	K16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA3, CLK5, BRGO3, TIN3	L17	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	L15	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	M16	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	N17	Bidirectional (5-V tolerant)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PB31, $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	G14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	J17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	M17	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	D17	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	F15	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	F16	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	K15	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	L16	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	K14	Bidirectional (5-V tolerant)
PC4, $\overline{\text{CD4}}$	M15	Bidirectional (5-V tolerant)
PD15, MII_RXD3	N15	Bidirectional (5-V tolerant)
PD14, MII_RXD2	P17	Bidirectional (5-V tolerant)
PD13, MII_RXD1	L14	Bidirectional (5-V tolerant)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
V_{SSSYN1}	R4	PLL analog GND
V_{DDSYN}	R3	PLL analog V_{DD}
GND	H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12	Power
V_{DDL}	B8, D2, E17, H16, M5, N3, T2, N16, U9	Power
V_{DDH}	G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13	Power
N/C	B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17	No connect