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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc852tcvr50a

- Two baud rate generators
  — Independent (can be connected toany SCC3/4 or SMC1)
  — Allows changes during operation
  — Autobaud support option
- Two SCCs (serial communication controllers)
  — Ethernet/IEEE 802.3® standard optional on SCC3 and SCC4, supporting full 10-Mbps operation
  — HDLC/SDLC
  — HDLC bus (implements an HDLC-based local area network (LAN))
  — Universal asynchronous receiver transmitter (UART)
  — Totally transparent (bit streams)
  — Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channel)
  — UART
- One SPI (serial peripheral interface)
  — Supports master and slave modes
  — Supports multimaster operation on the same bus
- PCMCIA interface
  — Master (socket) interface, release 2.1 compliant
  — Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  — Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  — Supports conditions: = ≠ < >
  — Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

Figure 1 shows the MPC852T block diagram.

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

8 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/ BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B37	UPWAIT valid to CLKOUT falling edge[10] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid[10] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge[11] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50MHz, use 9.80ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC852T is selected to work with external bus arbiter.

4 For part speeds above 50MHz, use 2ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50MHz, use 2ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 This formula applies to bus operation up to 50 MHz.

9 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

10 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

11 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

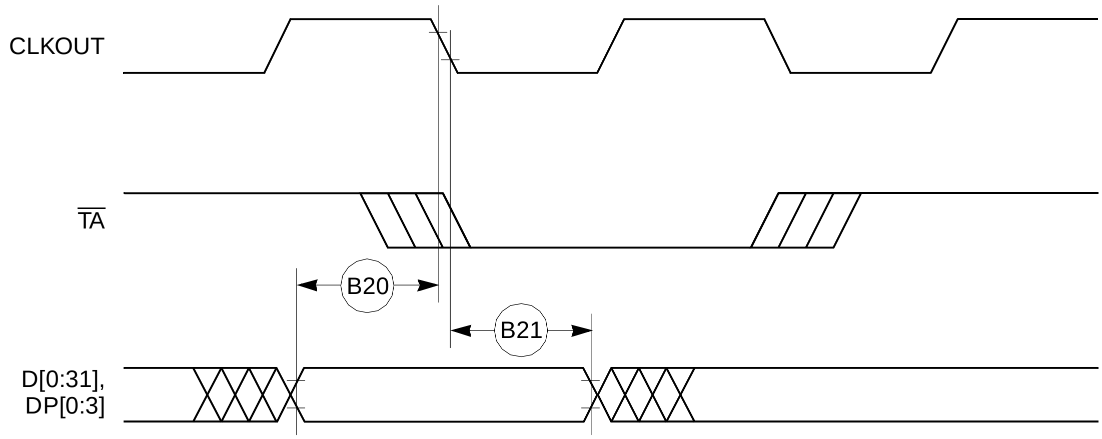

Figure 10. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read that various GPCM factors control.

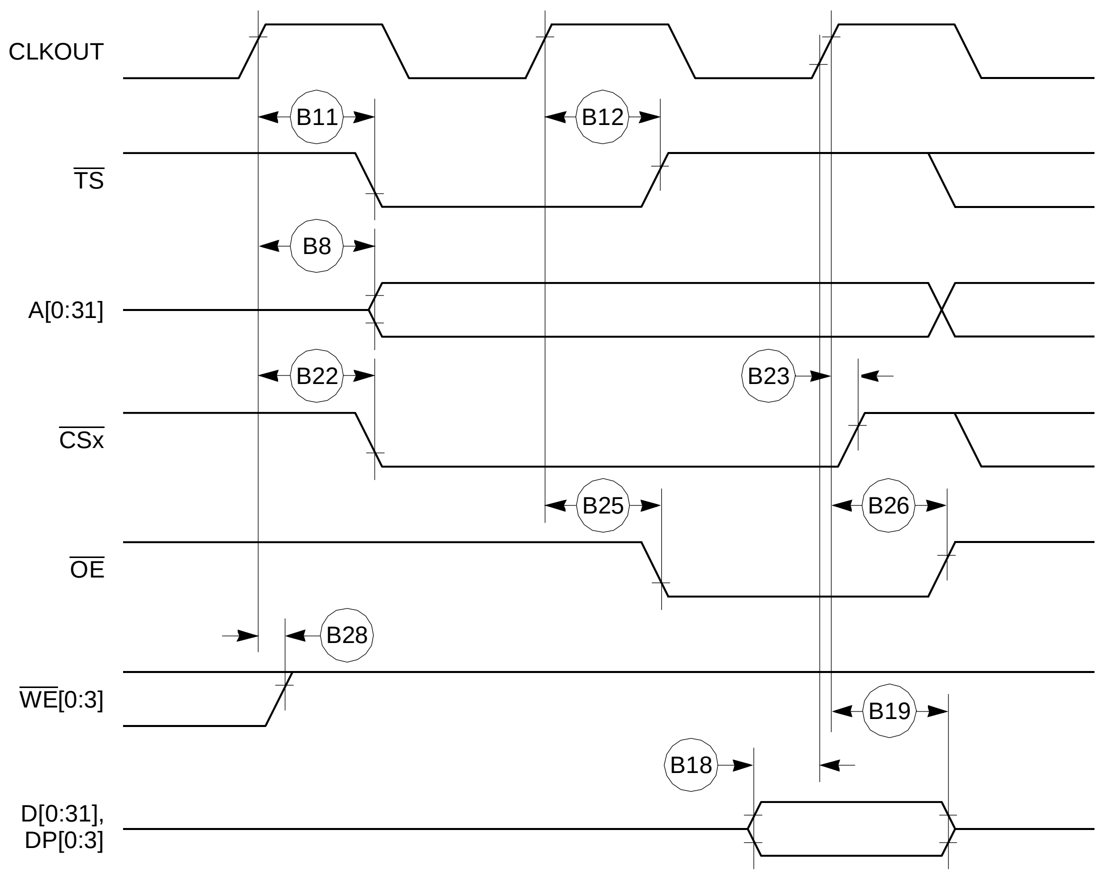

Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

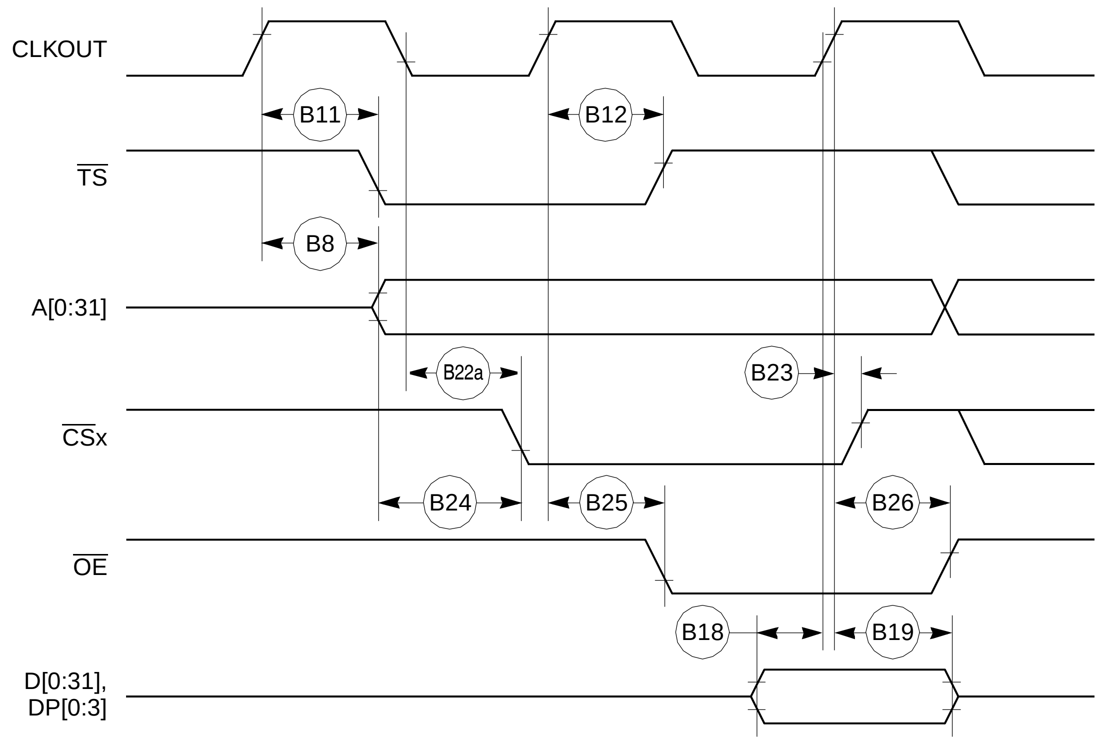

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

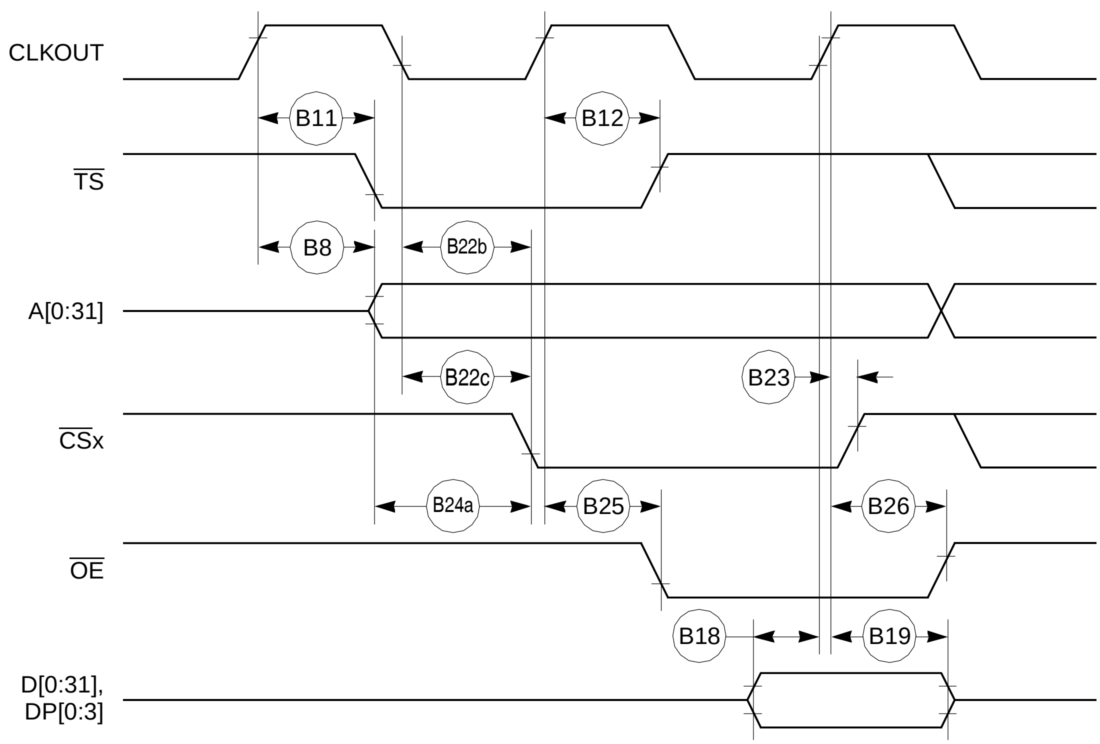

Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Table 10 provides interrupt timing for the MPC852T.

Table 10. Interrupt Timing

Num	Characteristic[1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT. The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

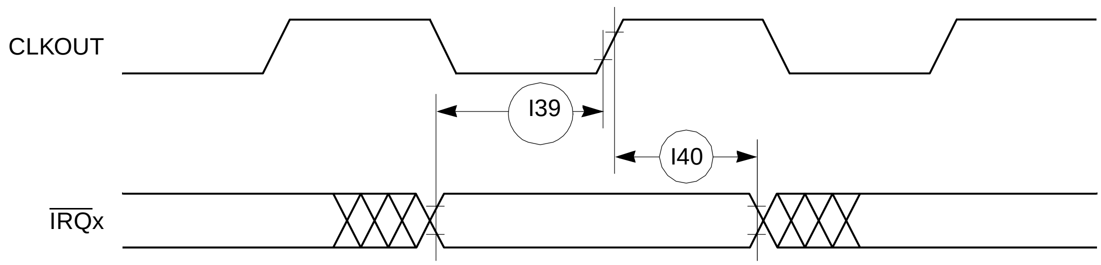

Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

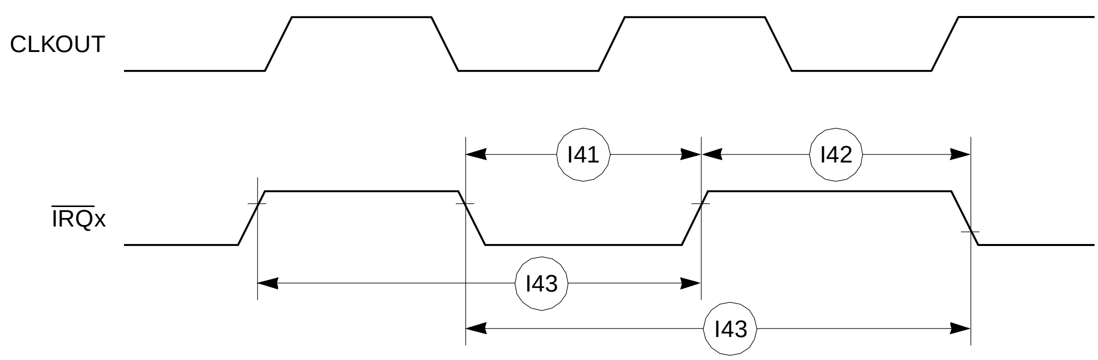

Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

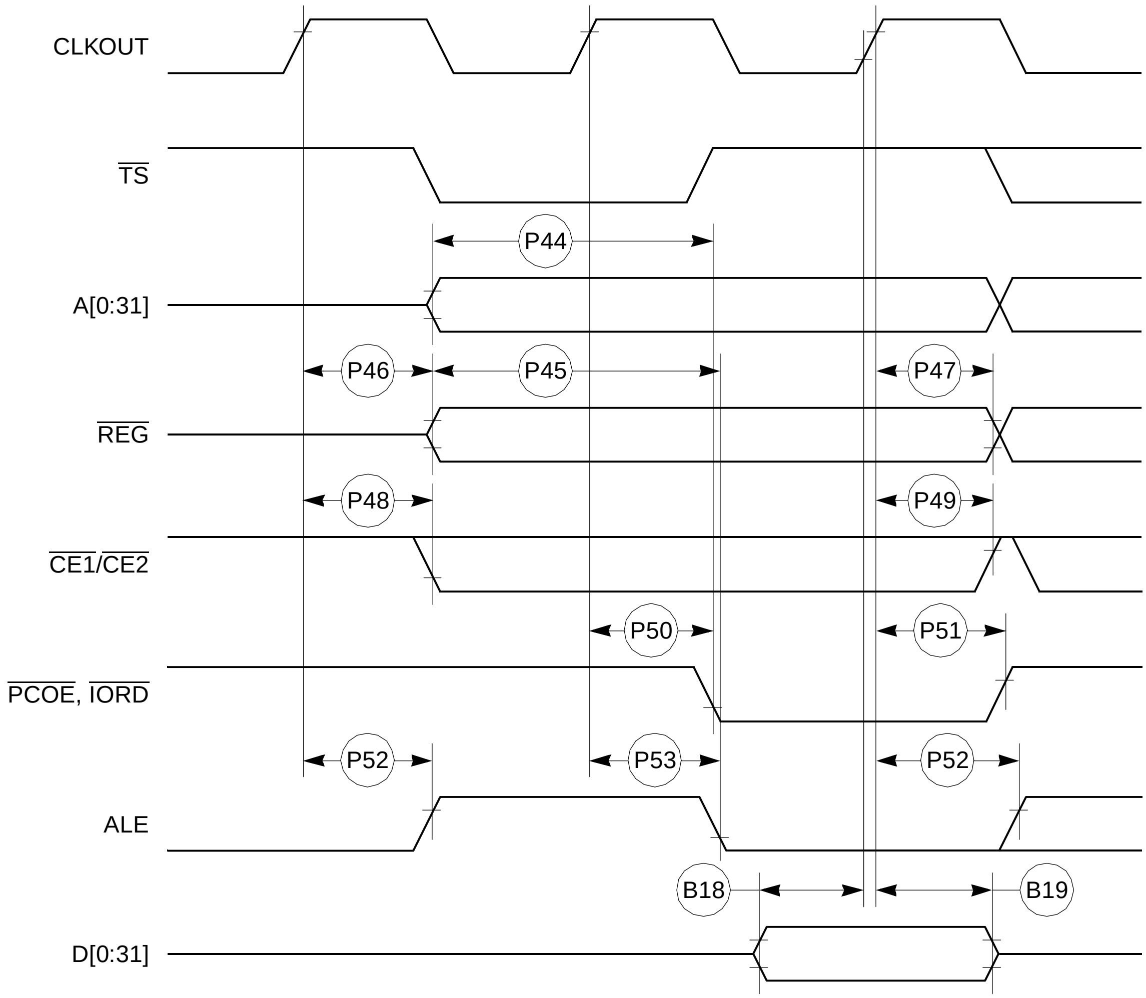

Figure 26. PCMCIA Access Cycles Timing External Bus Read

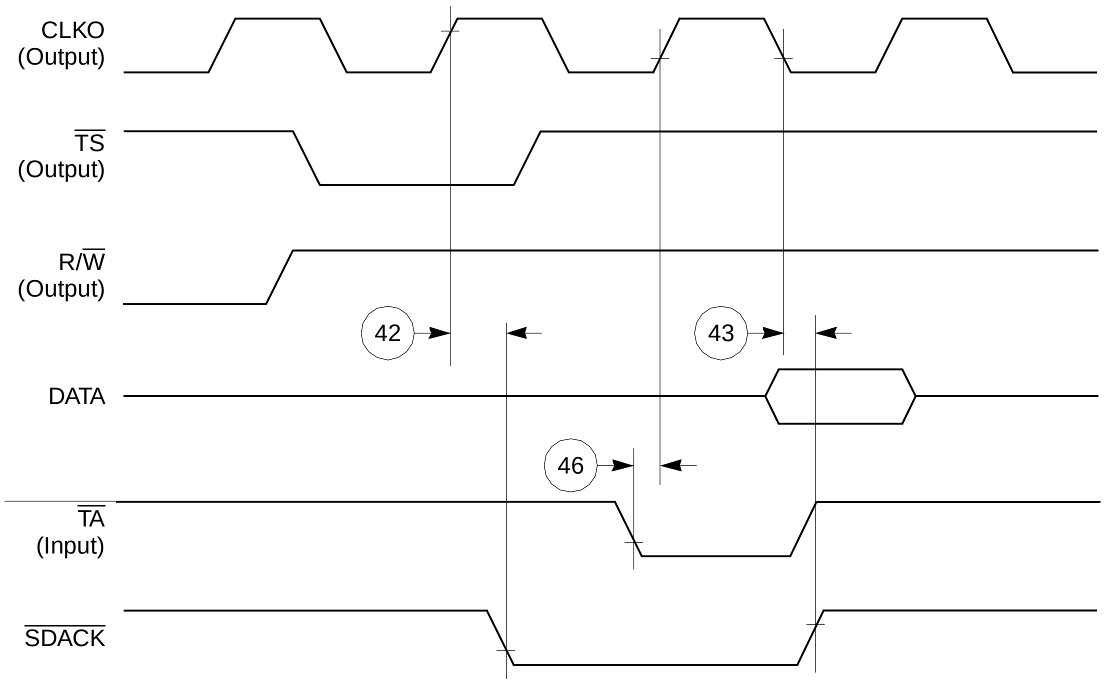

Figure 42. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

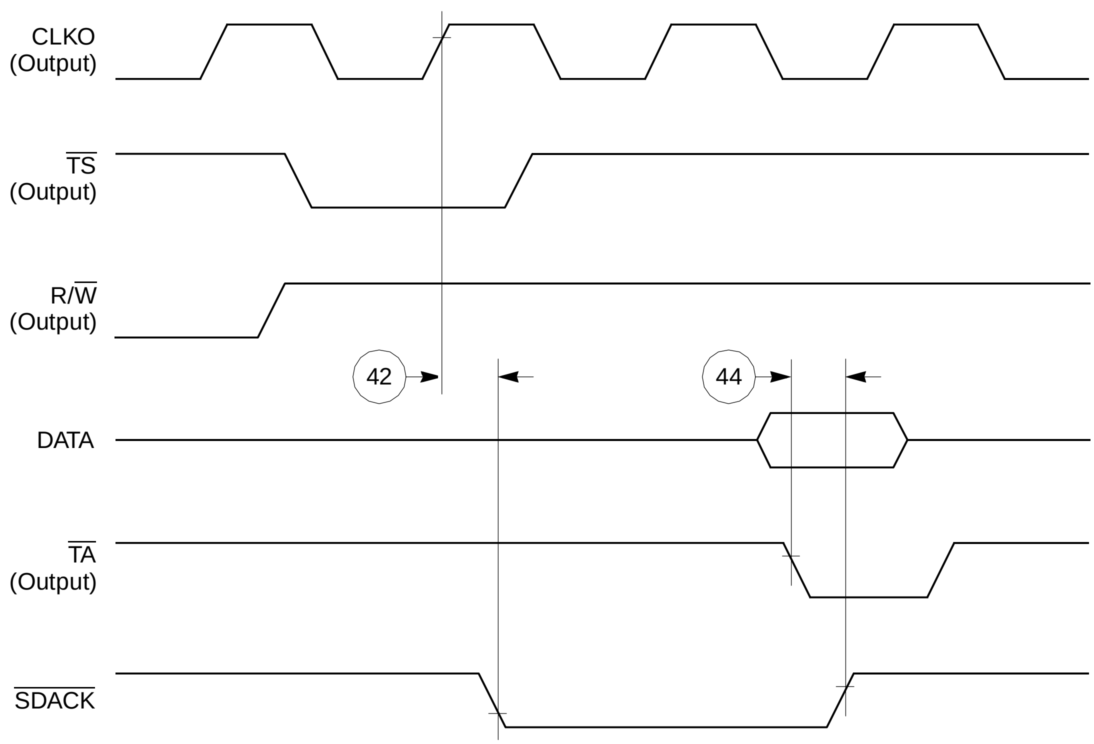

Figure 43. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

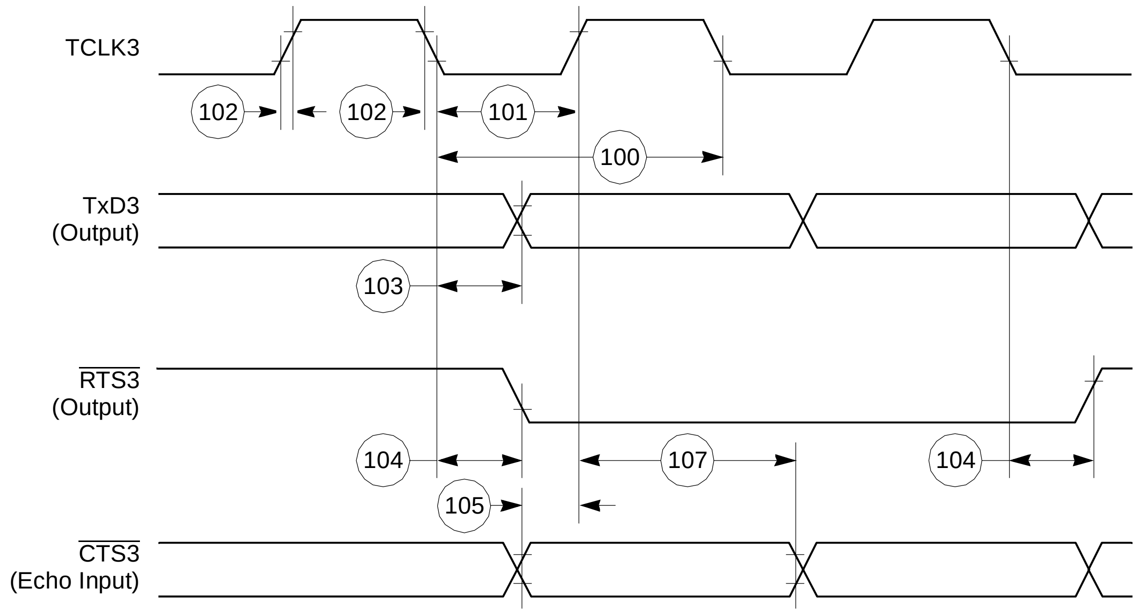

Figure 49. HDLC Bus Timing Diagram

14.6 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 50 through Figure 54.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period[1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

Table 26 provides information about the MII transmit signal timing,.

Table 26. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	—
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 60 shows the MII transmit signal timing diagram.

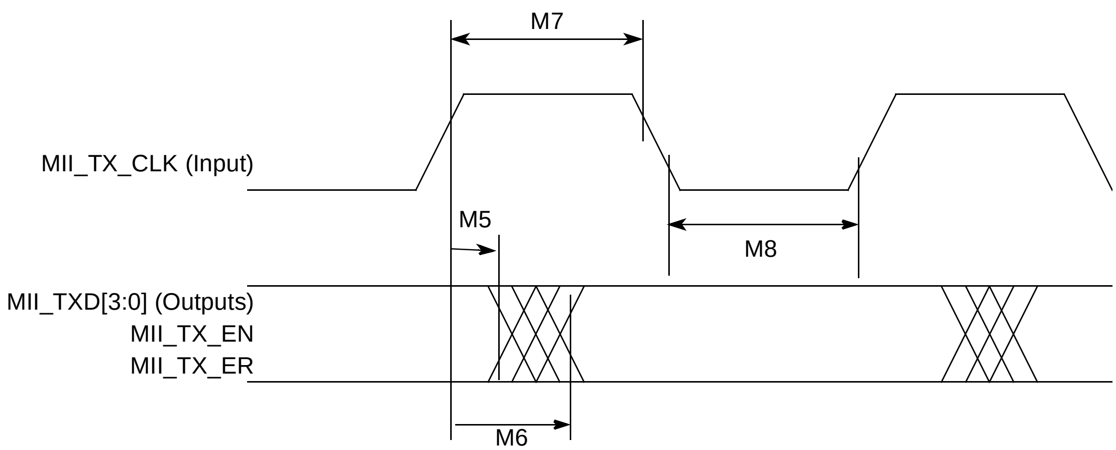

Figure 60. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 27 provides information about the MII async inputs signal timing.

Table 27. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 61 shows the MII asynchronous inputs signal timing diagram.

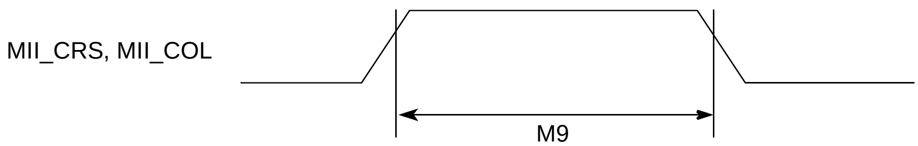

Figure 61. MII Async Inputs Timing Diagram

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
EXTAL	M1	Analog Input (1.8 V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8 V only)
ALE_A	H1	Output
$\overline{\text{CE1\_A}}$	E5	Output
$\overline{\text{CE2\_A}}$	B3	Output
$\overline{\text{WAIT\_A}}$	N3	Input (3.3 V only)
IP_A0	T2	Input (3.3 V only)
IP_A1	M6	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	R3	Input (3.3 V only)
IP_A3	M5	Input (3.3 V only)
IP_A4	T3	Input (3.3 V only)
IP_A5	N5	Input (3.3 V only)
IP_A6	M7	Input (3.3 V only)
IP_A7	R2	Input (3.3 V only)
DSCK	H2	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	H3, G1	Bidirectional (3.3 V only)
OP0	K1	Bidirectional (3.3 V only)
OP1	K2	Output
OP2, MODCK1, $\overline{\text{STS}}$	K3	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	L1	Bidirectional (3.3 V only)
BADDR[28:29]	L3, L2	Output
BADDR30, $\overline{\text{REG}}$	J3	Output
$\overline{\text{AS}}$	J2	Input (3.3 V only)
PA11, RXD3	E16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	H15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	J15	Bidirectional (Optional: Open-drain) (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PA3, CLK5, BRGO3, TIN3	K16	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	K14	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	L15	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	M16	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	F13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	G13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	H16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	L16	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	C16	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	E14	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	E15	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	J14	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	K15	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	J13	Bidirectional (5-V tolerant)

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PC4, $\overline{\text{CD4}}$	L14	Bidirectional (5-V tolerant)
PD15, MII_RXD3	M14	Bidirectional (5-V tolerant)
PD14, MII_RXD2	N16	Bidirectional (5-V tolerant)
PD13, MII_RXD1	K13	Bidirectional (5-V tolerant)
PD12, MII_MDC	N15	Bidirectional (5-V tolerant)
PD11, RXD3, MII_TX_ER	P16	Bidirectional (5-V tolerant)
PD10, TXD3, MII_RXD0	R15	Bidirectional (5-V tolerant)
PD9, RXD4, MII_TXD0	N14	Bidirectional (5-V tolerant)
PD8, TXD4, MII_RX_CLK	M13	Bidirectional (5-V tolerant)
PD7, $\overline{\text{RTS3}}$, MII_RX_ER	T15	Bidirectional (5-V tolerant)
PD6, $\overline{\text{RTS4}}$, MII_RX_DV	N13	Bidirectional (5-V tolerant)
PD5, MII_TXD3	R14	Bidirectional (5-V tolerant)
PD4, MII_TXD2	P14	Bidirectional (5-V tolerant)
PD3, MII_TXD1	M12	Bidirectional (5-V tolerant)
TMS	F15	Input (5-V tolerant)
TDI, DSDI	G14	Input (5-V tolerant)
TCK, DSCK	H13	Input (5-V tolerant)
$\overline{\text{TRST}}$	F16	Input (5-V tolerant)
TDO, DSDO	F14	Output (5-V tolerant)
MII_CRS	B6	Input

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
MII_MDIO	G16	Bidirectional (5-V tolerant)
MII_TXEN	T14	Output (5-V tolerant)
MII_COL	F2	Input
V_{SSSYN}	N4	PLL analog GND
V_{SSSYN1}	P3	PLL analog GND
V_{DDSYN}	P2	PLL analog V_{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
V_{DDL}	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
V_{DDH}	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No connect

Table 31 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

Table 31. Pin Assignments—Non-JEDEC

Name	Pin Number	Type
A[0:31]	C16, B16, B15, D15, E14, F12, C15, B14, D14, C14, E13, F11, D13, C13, B13, E12, F10, D12, B10, B12, E11, D11, C9, B11, E10, D10, D9, C12, B9, C11, C10, E9	Bidirectional Three-state (3.3 V only)
TSIZ0, $\overline{\text{REG}}$	F9	Bidirectional Three-state (3.3 V only)
TSIZ1	F8	Bidirectional Three-state (3.3 V only)
RD/$\overline{\text{WR}}$	C2	Bidirectional Three-state (3.3 V only)
$\overline{\text{BURST}}$	H4	Bidirectional Three-state (3.3 V only)
$\overline{\text{BDIP}}$, $\overline{\text{GPL\_B5}}$	E2	Output
$\overline{\text{TS}}$	F3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TA}}$	G5	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TEA}}$	F4	Open-drain
$\overline{\text{BI}}$	E3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$	H3	Bidirectional Three-state (3.3 V only)
$\overline{\text{IRQ4}}$, $\overline{\text{KR}}$ $\overline{\text{RETRY}}$, SPKROUT	K2	Bidirectional Three-state (3.3 V only)
$\overline{\text{CR}}$, $\overline{\text{IRQ3}}$	G2	Input (3.3 V only)
D[0:31]	T14, U12, T11, U11, U13, T10, T8, U7, U14, N11, P11, R11, R13, T13, N10, P10, R10, P12, U10, T9, R9, P9, U8, R12, R8, P8, N9, T12, T7, R7, U6, T6	Bidirectional Three-state (3.3 V only)
DP0, $\overline{\text{IRQ3}}$	R5	Bidirectional Three-state (3.3 V only)
DP1, $\overline{\text{IRQ4}}$	R6	Bidirectional Three-state (3.3 V only)
DP2, $\overline{\text{IRQ5}}$	U5	Bidirectional Three-state (3.3 V only)
DP3, $\overline{\text{IRQ6}}$	T5	Bidirectional Three-state (3.3 V only)
$\overline{\text{BR}}$	F2	Bidirectional (3.3 V only)
$\overline{\text{BG}}$	H5	Bidirectional (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{\text{BB}}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{\text{IRQ6}}$	J5	Bidirectional (3.3 V only)
$\overline{\text{IRQ0}}$	R14	Input (3.3 V only)
$\overline{\text{IRQ1}}$	N12	Input (3.3 V only)
$\overline{\text{IRQ7}}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{\text{CS}}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{\text{CS6}}$	E5	Output
$\overline{\text{CS7}}$	B4	Output
$\overline{\text{WE0}}$, BS_B0, $\overline{\text{IORD}}$	E7	Output
$\overline{\text{WE1}}$, BS_B1, $\overline{\text{IOWR}}$	D7	Output
$\overline{\text{WE2}}$, BS_B2, $\overline{\text{PCOE}}$	B6	Output
$\overline{\text{WE3}}$, BS_B3, $\overline{\text{PCWE}}$	C6	Output
$\overline{\text{BS\_A}}$[0:3]	B7, E8, D8, C8	Output
$\overline{\text{GPL\_A0}}$, $\overline{\text{GPL\_B0}}$	D6	Output
$\overline{\text{OE}}$, $\overline{\text{GPL\_A1}}$, $\overline{\text{GPL\_B1}}$	E6	Output
$\overline{\text{GPL\_A}}$[2:3], $\overline{\text{GPL\_B}}$[2:3], $\overline{\text{CS}}$[2–3]	B5, C5	Output
UPWAITA, $\overline{\text{GPL\_A4}}$	D3	Bidirectional (3.3 V only)
$\overline{\text{GPL\_A5}}$	F5	Output
$\overline{\text{PORESET}}$	R2	Input (3.3 V only)
$\overline{\text{RSTCONF}}$	L5	Input (3.3 V only)
$\overline{\text{HRESET}}$	K5	Open-drain
$\overline{\text{SRESET}}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{\text{CE1\_A}}$	F6	Output
$\overline{\text{CE2\_A}}$	C4	Output
$\overline{\text{WAIT\_A}}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IP_A1	N7	Input (3.3 V only)
IP_A2, $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1], VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2, MODCK1, $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3, MODCK2, DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30, $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11, RXD3	F17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA10, TXD3	J16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA9, RXD4	K17	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA8, TXD4	K16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PA3, CLK5, BRGO3, TIN3	L17	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	L15	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	M16	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	N17	Bidirectional (5-V tolerant)

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