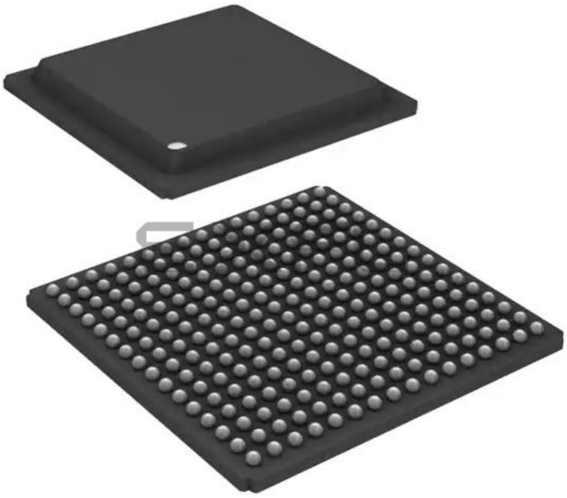

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc852tcvr66a

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	– 40	°C
	$T_{j(max)}$	100	°C

[1] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage that high-static voltage or electrical fields cause; however, Freescale recommends taking normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC852T.

Table 3. MPC852T Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient[1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$[2]	49	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	32	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$[3]	41	
		Four-layer board (2s2p)	$R_{\theta JMA}$[3]	29	
Junction-to-board[4]			$R_{\theta JB}$	24	
Junction-to-case[5]			$R_{\theta JC}$	13	
Junction-to-package top[6]	Natural convection		Ψ_{JT}	3	
	Airflow (200 ft/min)		Ψ_{JT}	2	

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal

[3] Per JEDEC JESD51-6 with the board horizontal

[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical[1]	Maximum[2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V. and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation, and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application that buffer current can cause, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC852T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} to V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{TRST}$, TMS, MII_TXEN, MII_MDIO)[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

8 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in Table 6 in the boot code after the reset deasserts.

Table 6. Mandatory Reset Configuration of MPC852T

Register/Configuration	Field	Value (Binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	X1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	X1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4–7] PAPAR[12–15]	0
PADIR (Port A data direction register)	PADIR[4–7] PADIR[12–15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16–23] PBPAR[26–27]	0
PBDIR (Port B data direction register)	PBDIR[14] PBDIR[16–23] PBDIR[26–27]	1
PCPAR (Port C pin assignment register)	PCPAR[8–11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8–11] PCDIR[14]	1

11 Layout Practices

Each V_{DD} pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC866 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})."

12 Bus Signal Timing

The maximum bus speed that the MPC852T supports is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core	40	50	40	66.67
Bus	40	50	40	66.67

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core	40	50	40	66.67	40	80	40	100
Bus 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC852T at 33, 40, 50, and 66 MHz.

The timing for the MPC852T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT) See Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew—If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK[1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30b	WE(0:3)/BS_B[0:3] negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. CS negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B30c	WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. CS negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	WE(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, CS negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to CS valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to CS valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to CS valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to CS valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to CS valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to BS valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns

Figure 4 is the control timing diagram.

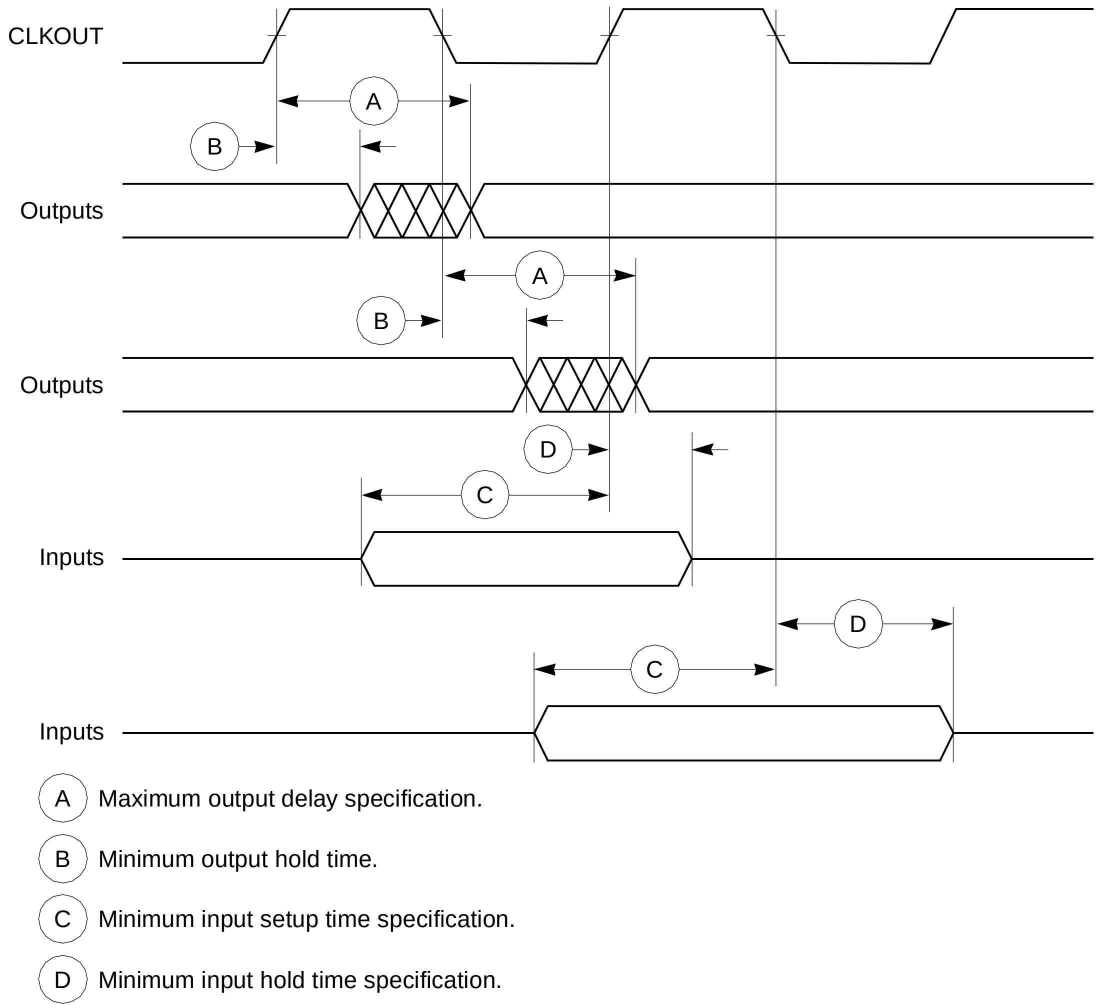

Figure 4. Control Timing

Figure 5 provides the timing for the external clock.

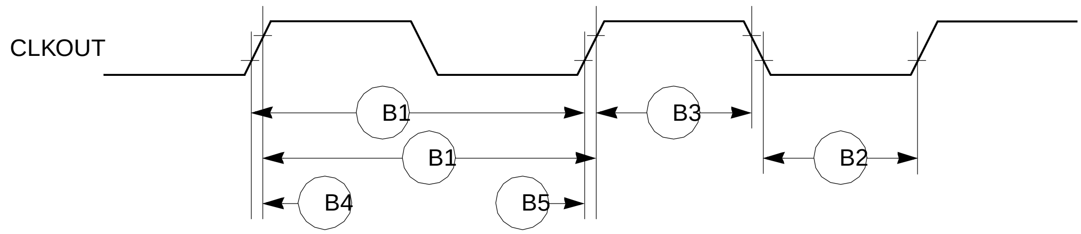

Figure 5. External Clock Timing

Table 13 shows the debug port timing for the MPC852T.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	DSCK cycle time	$3 \times T_{CLOCKOUT}$	—	—
J83	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$	—	—
J84	DSCK rise and fall times	0.00	3.00	ns
J85	DSDI input data setup time	8.00	—	ns
J86	DSDI data hold time	5.00	—	ns
J87	DSCK low to DSDO data valid	0.00	15.00	ns
J88	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 31 provides the input timing for the debug port clock.

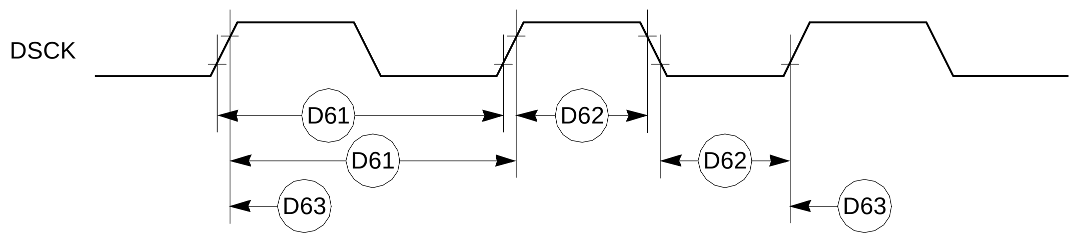

Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.

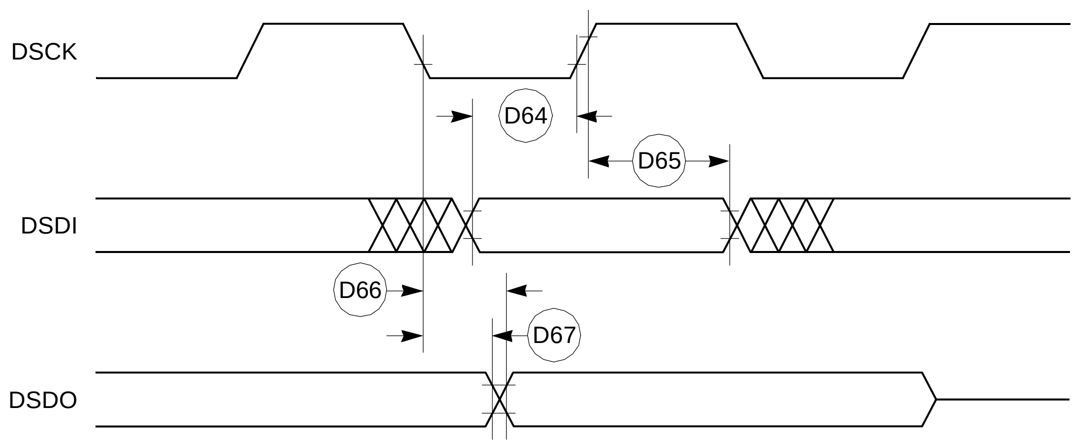

Figure 32. Debug Port Timings

Figure 33 shows the reset timing for the data bus configuration.

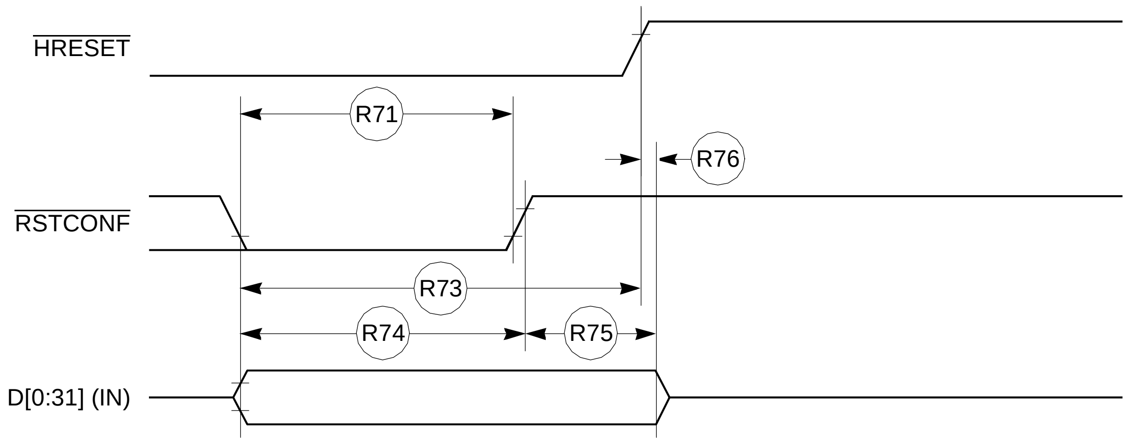

Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.

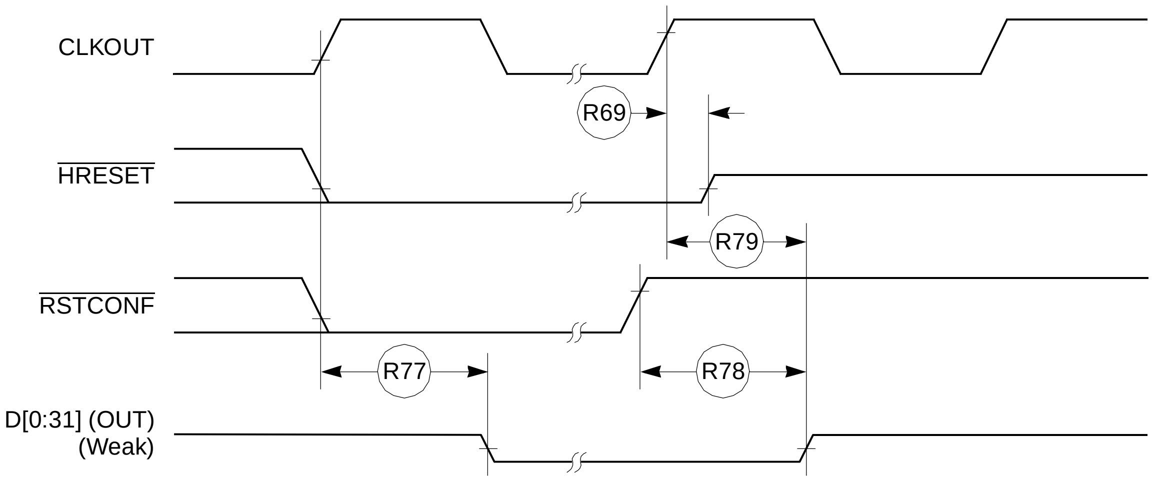

Figure 34. Reset Timing—Data Bus Weak Drive During Configuration

Figure 35 provides the reset timing for the debug port configuration.

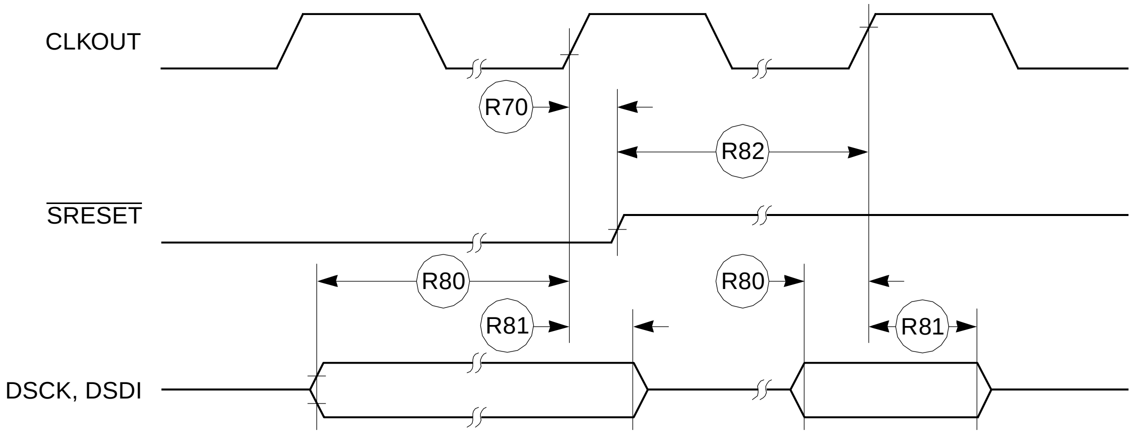

Figure 35. Reset Timing—Debug Port Configuration

13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 36 through Figure 39.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

14 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC852T.

14.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 40 shows the port C interrupt detection timing.

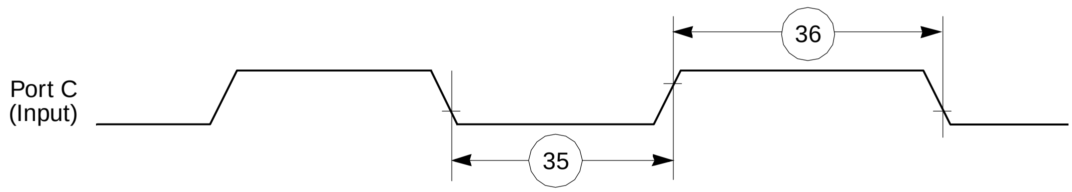

Figure 40. Port C Interrupt Detection Timing

Figure 47 through Figure 49 show the NMSI timings.

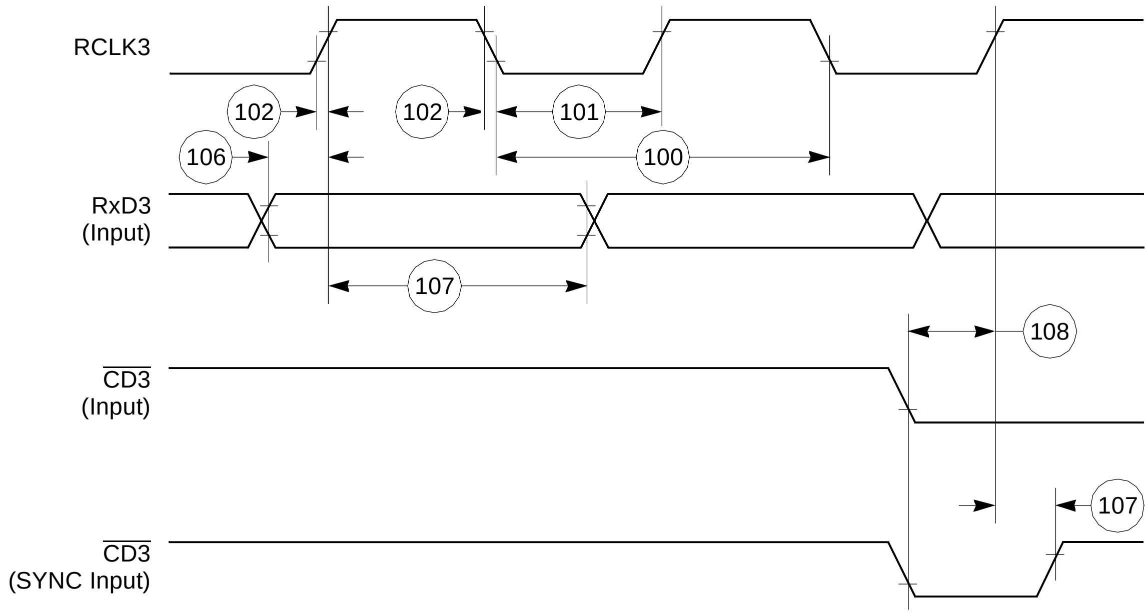

Figure 47. SCC NMSI Receive Timing Diagram

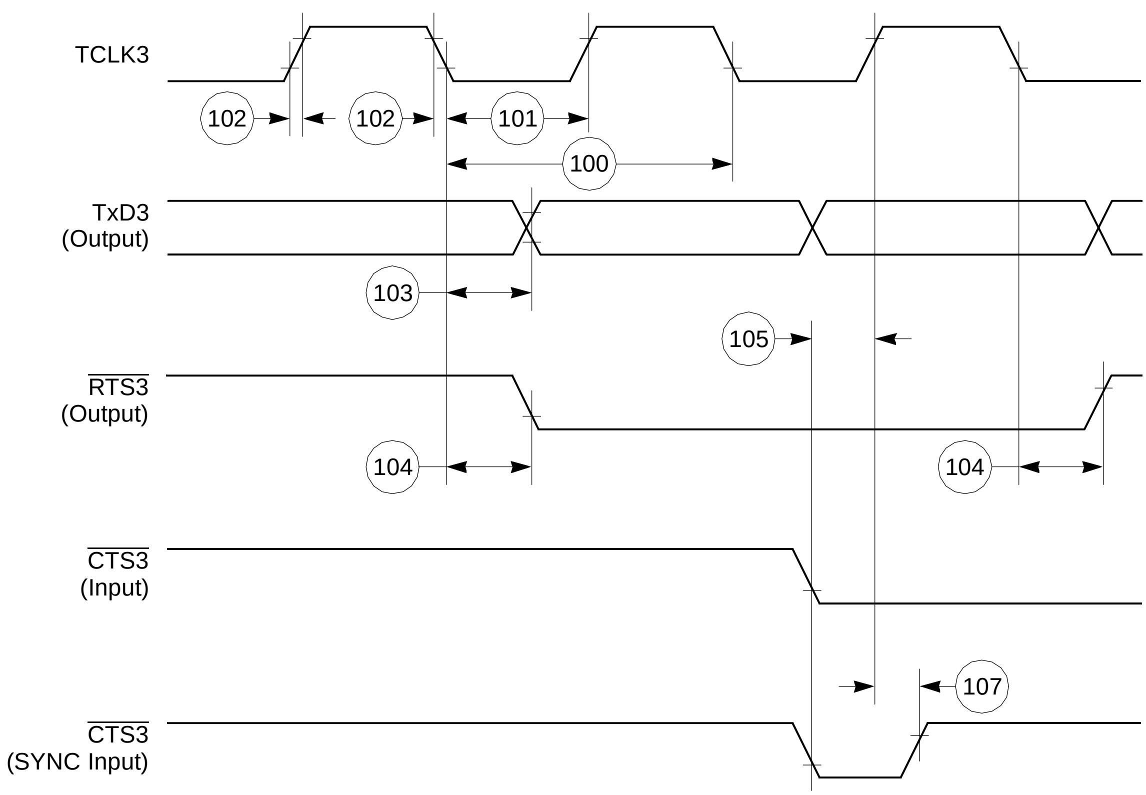

Figure 48. SCC NMSI Transmit Timing Diagram

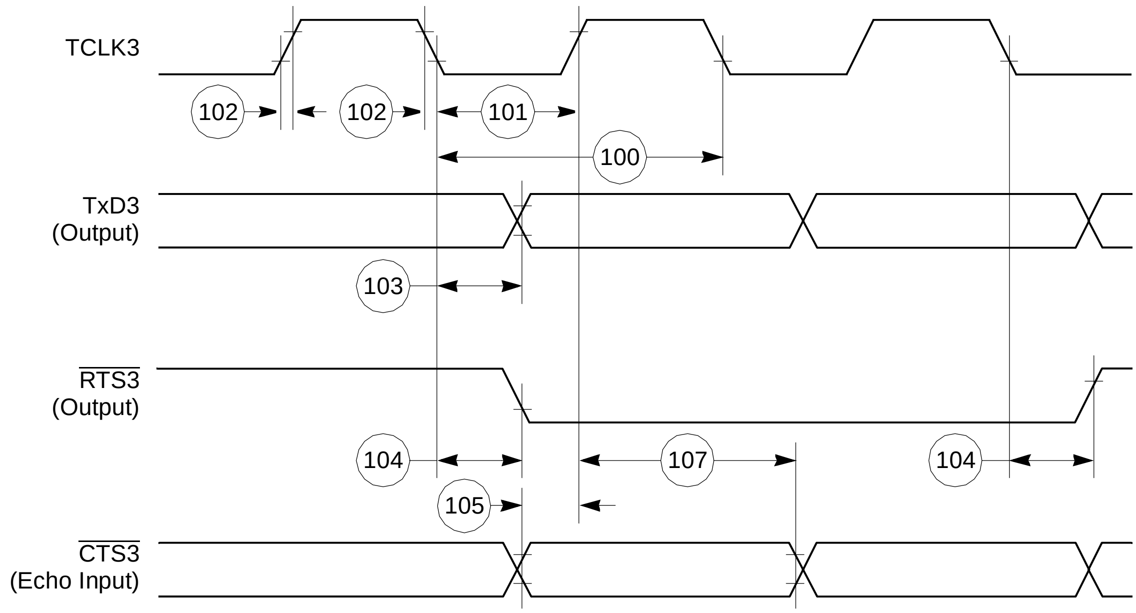

Figure 49. HDLC Bus Timing Diagram

14.6 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 50 through Figure 54.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period[1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
FRZ IRQ6	H4	Bidirectional (3.3 V only)
IRQ0	P13	Input (3.3 V only)
IRQ1	M11	Input (3.3 V only)
M_TX_CLK IRQ7	N12	Input (3.3 V only)
CS[0:5]	B2, A2, D3, C3, E6, C4	Output
CS6	D4	Output
CS7	A3	Output
WE0 BS_B0 IORD	D6	Output
WE1 BS_B1 IOWR	C6	Output
WE2 BS_B2 PCOE	A5	Output
WE3 BS_B3 PCWE	B5	Output
BS_A[0:3]	A6, D7, C7, B7	Output
GPL_A0 GPL_B0	C5	Output
OE GPL_A1 GPL_B1	D5	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	A4, B4	Output
UPWAITA GPL_A4	C2	Bidirectional (3.3 V only)
GPL_A5	E4	Output
PORESET	P1	Input (3.3 V only)
RSTCONF	K4	Input (3.3 V only)
HRESET	J4	Open-drain
SRESET	M3	Open-drain
XTAL	N1	Analog Output

Table 30. Pin Assignments—JEDEC Standard (continued)

Name	Pin Number	Type
PA3, CLK5, BRGO3, TIN3	K16	Bidirectional (5-V tolerant)
PA2, CLK6, $\overline{\text{TOUT3}}$	K14	Bidirectional (5-V tolerant)
PA1, CLK7, BRGO4, TIN4	L15	Bidirectional (5-V tolerant)
PA0, CLK8, $\overline{\text{TOUT4}}$	M16	Bidirectional (5-V tolerant)
PB31, $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB30, SPICLK	F13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB29, SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB28, SPIMISO, BRGO4	G13	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB25, SMTXD1	H14	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB24, SMRXD1	H16	Bidirectional (Optional: Open-drain) (5-V tolerant)
PB15, BRGO3	L16	Bidirectional (5-V tolerant)
PC15, $\overline{\text{DREQ0}}$	C16	Bidirectional (5-V tolerant)
PC13, $\overline{\text{RTS3}}$	E14	Bidirectional (5-V tolerant)
PC12, $\overline{\text{RTS4}}$	E15	Bidirectional (5-V tolerant)
PC7, $\overline{\text{CTS3}}$	J14	Bidirectional (5-V tolerant)
PC6, $\overline{\text{CD3}}$	K15	Bidirectional (5-V tolerant)
PC5, $\overline{\text{CTS4}}$, SDACK1	J13	Bidirectional (5-V tolerant)

16.1.2 The non-JEDEC Pinout

Figure 64 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *PowerQUICC™ Family Reference Manual*.

NOTE: This figure shows the top view of the device.

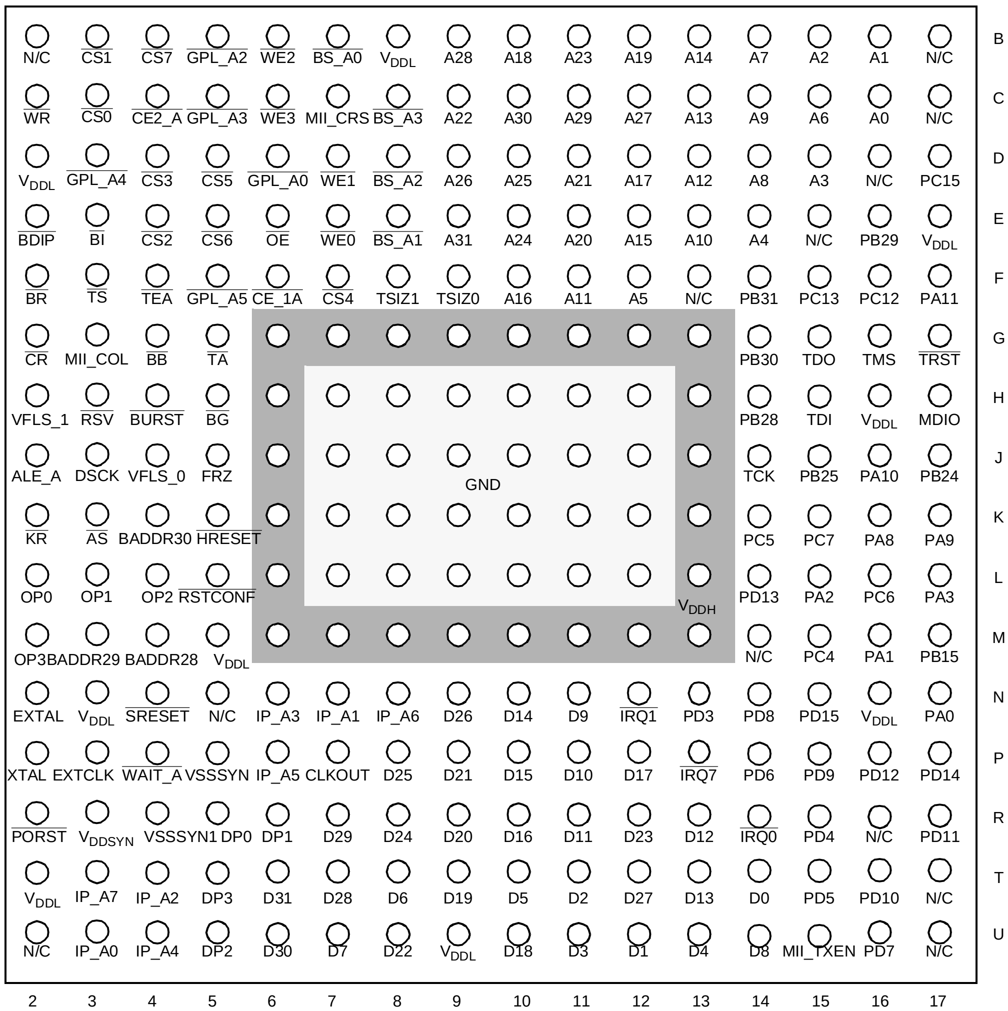

Figure 64. Pinout of PBGA Package—Non-JEDEC

Table 31. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{BB}$	G4	Bidirectional Active Pull-up (3.3 V only)
FRZ, $\overline{IRQ6}$	J5	Bidirectional (3.3 V only)
$\overline{IRQ0}$	R14	Input (3.3 V only)
$\overline{IRQ1}$	N12	Input (3.3 V only)
$\overline{IRQ7}$, M_TX_CLK	P13	Input (3.3 V only)
$\overline{CS}$[0:5]	C3, B3, E4, D4, F7, D5	Output
$\overline{CS6}$	E5	Output
$\overline{CS7}$	B4	Output
$\overline{WE0}$, BS_B0, $\overline{IORD}$	E7	Output
$\overline{WE1}$, BS_B1, $\overline{IOWR}$	D7	Output
$\overline{WE2}$, BS_B2, $\overline{PCOE}$	B6	Output
$\overline{WE3}$, BS_B3, $\overline{PCWE}$	C6	Output
$\overline{BS\_A}$[0:3]	B7, E8, D8, C8	Output
$\overline{GPL\_A0}$, $\overline{GPL\_B0}$	D6	Output
$\overline{OE}$, $\overline{GPL\_A1}$, $\overline{GPL\_B1}$	E6	Output
$\overline{GPL\_A}$[2:3], $\overline{GPL\_B}$[2:3], $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA, $\overline{GPL\_A4}$	D3	Bidirectional (3.3 V only)
$\overline{GPL\_A5}$	F5	Output
$\overline{PORESET}$	R2	Input (3.3 V only)
$\overline{RSTCONF}$	L5	Input (3.3 V only)
$\overline{HRESET}$	K5	Open-drain
$\overline{SRESET}$	N4	Open-drain
XTAL	P2	Analog output
EXTAL	N2	Analog input (3.3 V only)
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{CE1\_A}$	F6	Output
$\overline{CE2\_A}$	C4	Output
$\overline{WAIT\_A}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)

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